Non-Hermitian Physics-Inspired Voltage-Controlled Oscillators with Resistive Tuning

Weidong Cao^a, Hua Wang^b, and Xuan Zhang^a

^aWashington University in St. Louis, Saint Louis, MO, USA; ^bETH Zürich, Zürich, Switzerland

Abstract—This paper presents a non-Hermitian physics-inspired voltage-controlled oscillator (VCO) topology, which is termed parity-time-symmetric topology. The VCO consists of two coupled inductor-capacitor (LC) cores with a balanced gain and loss profile. Due to the interplay between the gain/loss and their coupling, an extra degree of freedom is enabled via resistive tuning, which can enhance the frequency tuning range (FTR) beyond the bounds of conventional capacitive or inductive tuning. A silicon prototype is implemented in a standard 130 nm bulk CMOS process with a core area of 0.15mm². Experimental results show that it achieves a $3.1 \times$ FTR improvement and 30% phase noise reduction of the baseline VCO with the same amount of capacitive tuning ability.

Index Terms—Non-Hermitian physics, voltage-controlled oscillator, PT-symmetry, resistive tuning, frequency tuning range.

I. INTRODUCTION

Inductor-capacitor (LC) voltage-controlled oscillators (VCOs) are the key building blocks in many communication systems [1]–[3]. Such local oscillators need to cover a wide frequency tuning range (FTR) and maintain good phase noise (PN) performance. Existing methods mainly rely on aggressive inductive tuning (e.g., negative inductance/switched-inductors) [4], [5] or capacitive tuning (e.g., varactors/switched-capacitors) [6] to reach a wide FTR. However, they often suffer from degenerated PN performance due to the excessive noise sources introduced by the tuning mechanisms. Some techniques have been proposed to tackle the stringent design trade-off between FTR and PN. For example, multi-core and multi-mode VCOs implemented with two or more coupled LC cores can reduce PN and extend the FTR, but bear the cost of excessive design complexity in VCO cores [7], [8]. On the other hand, leveraging multiple separated LC VCOs can extend the FTR, but induces large area overhead and high multiplexing complexity [9]. Therefore, developing more effective approaches to improving the FTR without hurting the PN performance is highly desirable.

Toward the goal, a gain-loss coupled dual-core VCO topology based on non-Hermitian physics is shown in this paper, which is originally proposed in our prior work [10]. From the perspective of non-Hermitian physics, the eigenfrequency of a physical system built upon two coupled units with a balanced gain and loss distribution can evolve in a wide range by tuning the gain/loss contrast [10], [11]. Inspired by this physical principle, we build this gain-loss coupled dual-core VCO. It not only inherits the superior PN performance from the coupled structure of multi-core VCOs but also achieves an enlarged FTR beyond the bounds of conventional capacitive/inductive tuning with extra resistive tuning. The proposed topology can be combined with existing optimization approaches to further advance VCO performance. Section II introduces the theoretical model of non-Hermitian quantum physical systems



Fig. 1. (a) Illustration of an open non-Hermitian quantum system that can be modeled as a gain (G) or a loss (L) unit. (b) Illustration of a non-Hermitian quantum system with a coupled gain and loss profile. $\omega_{1,2}$ is the resonant frequency of the unit. -g and l represents gain and loss amount respectively.

composed of two coupled units with a balanced gain and loss profile. Circuit design and analysis are presented in Section III. Comprehensive measurement results are shown in Section IV before the conclusion in Section V.

II. BACKGROUND

A. Non-Hermitian Quantum Mechanics

In quantum mechanics, an open system can be generally modeled as a gain (or loss) unit with a resonant frequency as shown in Fig. 1(a). Such systems are described by non-Hermitian Hamiltonians which preserve complex eigenvalues, i.e., $\omega_1 - ig$ or $\omega_2 + il$. However, non-Hermitian quantum systems built upon two coupled units, one with gain and the other one with loss as shown in Fig. 1(b), possess purely real eigenfrequencies in certain regimes as derived below. Note that such systems are also specifically termed parity-time-symmetric (PT-symmetric) systems [10]. The system dynamics in Fig. 1(b) is expressed as

$$\frac{d}{dt} \begin{bmatrix} a_{\rm G} \\ a_{\rm L} \end{bmatrix} = \begin{bmatrix} i\omega_1 + g & \kappa \\ \kappa & i\omega_2 - l \end{bmatrix} \cdot \begin{bmatrix} a_{\rm G} \\ a_{\rm L} \end{bmatrix}, \qquad (1)$$

where the subscript G (or L) refers to the gain (or loss) unit and $a_{G,L}$ is the field amplitude defined such that $|a_{G,L}|^2$ represents the energy stored in each unit. g (or l) presents the gain (or loss) of the unit. κ indicates the coupling strength between the two units and $\omega_{1,2}$ represents the resonant frequency of each unit. To find the eigenfrequencies, we let $a_{G,L} \propto \exp^{i\omega t}$ and obtain the characteristic equation as

$$(i(\omega_1 - \omega) + g) \cdot (i(\omega_2 - \omega) - l) + \kappa^2 = 0.$$
⁽²⁾

For a balanced system where the gain is equal to the loss, i.e., g=l, the solutions are then given by the following expression:

$$\omega = \omega_0 \pm \sqrt{\kappa^2 - g^2}, \, \omega_0 = (\omega_1 + \omega_2)/2. \tag{3}$$

Eq. (3) shows that when the coupling strength κ is stronger than a threshold determined by the gain-loss contrast g, i.e., $\kappa > g = l$,



Fig. 2. Structure comparisons between (a) conventional single-core VCOs, (b) multi-core VCOs, and (c) proposed VCOs. (d) Numerical comparisons of frequency tuning between the three types of VCOs.

the system has a pair of real eigenfrequencies. Particularly, these eigenfrequencies could evolve with gain-loss contrast in a wide range as long as $g = l \in (0, \kappa)$. This simple analysis suggests that the interplay between gain/loss and their coupling provides a new degree of tuning freedom, i.e., gain/loss tuning freedom, to modulate the behaviors of a system. In the next section, we discuss how this physical principle (i.e., PT-symmetric topology) can be applied to design VCOs.

B. Non-Hermitian Quantum Mechanics for VCO Design

Before introducing the proposed VCO topology, Fig. 2 first re-examines conventional single-core and multi-core VCOs. A single-core VCO can be simplified into an active LC resonator shown in Fig. 2(a). It consists of a gain (-R) and an LC core with an intrinsic loss (R_0). A multi-core VCO (e.g., dual-core) is built upon two coupled single-core VCOs with a fixed coupling strength κ , each of which is simplified into an active LC resonator. For both VCOs, at the start-up phase, the gain is set to be slightly higher than the inherent loss to produce an oscillation with exponentially-growing amplitude. As the amplitude grows, the gain saturates and equates the loss in the large-signal domain due to nonlinearity. The oscillation then becomes stable, and the frequency (i.e., ω_S/ω_M in Fig. 2(a)/(b)) can only be adjusted via ω_0 by tuning the core's capacitance or inductance. In particular, the multi-core VCO has two frequency modes as shown by ω_M in Fig. 2(b).



Fig. 3. The circuit schematic of the proposed VCO.

This re-examination shows that in the conventional VCOs. the gain-loss distribution plays only a trivial role in the transient behavior of oscillators, i.e., the gain is used to compensate for the undesired loss to establish the start-up condition for the exponential growth of oscillation amplitude. Fortunately, based on the non-Hermitian quantum mechanics introduced before, the loss is useful if the gain-loss distribution in a system is properly manipulated. Inspired by this physical principle, our method explores the interplay between the gain/loss distribution and their coupling to enhance the frequency tuning bandwidth of VCOs. Fig. 2(c) exhibits the simplified topology of the proposed VCO. It is built upon two coupled LC cores, one active with a negative resistance -q and the other one dissipative with an equal amount of loss l, and the two cores have the same capacitance and inductance. The proposed VCO exhibits two frequency modes as shown by $\omega_{\rm P}$ in Fig. 2(c) and an extra resistive tuning freedom (i.e., g) that is orthogonal with the typical capacitive/inductive tuning freedoms of ω_0 . Fig. 2(d) numerically compares the frequency tuning of these three types of VCOs. Both the single-core VCO and multi-core VCO have only individual frequency points (i.e., blue circle and red asterisks), which are independent of g. However, the proposed VCO has a very wide FTR enabled by g. The comparison shows that the proposed VCO with the resistive tuning freedom can achieve a wider FTR than conventional VCOs given the same capacitive/inductive tuning ability preserved by ω_0 .

III. GAIN-LOSS COUPLED DUAL-CORE VCO TOPOLOGY

A. Circuit Design

Fig. 3 shows the proposed VCO circuit. The gain side has a tunable gain rate generated by cross-coupled differential pairs (XDPs) and an inherent loss rate R_{G0} , leading to the total gain of $-R_G = (-1/G_m)||R_{G0}; G_m = (g_{mn} + g_{mp})/2$, where g_{mn} and g_{mp} are the small signal transconductance of NMOS and PMOS XDP. The loss side has an intrinsic loss rate R_{L0} and a variable loss rate R_{L1} , giving the total loss of $R_L = R_{L0}||R_{L1}$. To make loss adjustable, a variable resistor based on stacked transistors is parallelly connected to the loss side. The subset in Fig. 3 shows the schematic of the variable resistor R_{L1} . All the gates of MOSFETs are connected together. By tuning the gate voltage V_{BIASL} , the resistance can be continuously adjusted in a wide range. The capacitor C_G (C_L) in each LC core is composed of a parasitic capacitance C_{G0} (C_{L0}), a fixed Metal-Insulator-Metal

(MIM) capacitor C_{G1} (C_{L1}) with high-quality factor (high-Q) and an adjustable varactor C_{G2} (C_{L2}). The varactor takes up a small proportion of the total capacitance and is mainly used to compensate for the fabrication mismatch of the fixed MIM capacitors on each side. The coupling capacitance (C_C) is realized by two equal MIM capacitors (C_{C1} and C_{C2}) which are serially connected through an on-chip switch (SW). The inductance (L_G/L_L) in both cores comes from the high-Q symmetrical parallel inductor (symindp) of the technology. A center tap connection is provided such that both cores share the same common mode voltage by connecting the center taps of the inductors. The balanced condition is satisfied by setting $R_G \approx R_L = R$, $L_G \approx L_L = L$, and $C_G \approx C_L = C$.

B. Phase Noise Analysis

We perform a qualitative analysis on the phase noise (PN) of the proposed VCO. It is well-established in the classic VCO theory that a multi-core VCO built upon a coupled structure can lead to PN reduction as compared to a single-core VCO. By taking a two-core VCO as an example, the improved PN can be intuitively understood as that the equivalent current noise of each LC core experiences twice the capacitance, and therefore its PN contribution is reduced by 6 dB. Two noise contributions from the two cores are uncorrelated and can be summed up, ideally leading to a 3 dB reduction of the total PN. Generally, for an N-core VCO built upon a coupled structure, its PN is lower than a single-core VCO by $10\log_{10}N$ dB. Thanks to the coupled structure, the proposed VCO topology also inherits the PN advantage of conventional multi-core VCOs. On the other hand, the gain-loss tuning physically realized by active devices, although it does not generate more inherent losses, does contribute additional noise to the system. However, this is not a big issue as the unique gain-loss tuning also increases the carrier amplitude which suppresses the effect of noise. It can be shown as follows. For the proposed VCO, the gain not only compensates the inherent loss in the active core but also offsets the tunable loss in the coupled lossy core. Assuming the ratio between the tunable gain $-G_m$ generated by XDPs and the inherent loss R_0 is β ($\beta > 1$), the PN of the active core in our proposed VCO can be obtained based on the well-known PN model of single-core VCOs as below:

$$\mathcal{L}_{\mathbf{P}}(\Delta\omega) = 10\log_{10}\left((1+\beta m) \cdot \frac{4kTR_{0}}{(\beta^{2}V_{\text{osc}})^{2}} \cdot \left(\frac{\omega}{2Q_{S}\Delta\omega}\right)^{2}\right)$$

$$= \underbrace{10\log_{10}\left((1+m) \cdot \frac{4kTR_{0}}{(V_{\text{osc}})^{2}} \cdot \left(\frac{\omega}{2Q_{S}\Delta\omega}\right)^{2}\right)}_{\mathcal{L}_{S}(\Delta\omega)}$$

$$-\underbrace{10\log_{10}\left(\frac{\beta^{4}(1+m)}{(1+\beta m)}\right)}_{>0} < \mathcal{L}_{S}(\Delta\omega), \qquad (4)$$

where k is the Boltzmann constant; T is the absolute temperature; R_0 is the inherent resonator loss; m (m > 1) is a constant noise factor of active elements; V_{osc} is the amplitude of the carrier; Q_S is the quality factor of the LC core; $\mathcal{L}_S(\Delta \omega)$ is PN of a conventional single-core VCO. Compared to the PN of conventional single-core VCOs, both the noise factor m of active devices and the amplitude



Fig. 4. Die micrograph of the proposed VCO.



Fig. 5. Frequency tuning of the two VCOs. (a), The baseline VCO. (b), The proposed VCO. Theory: theoretical predictions; Exp: experimental results.

 $V_{\rm osc}$ of carrier increase in the PN formula of the active core of the proposed VCO. But the carrier amplitude increases to $\beta^2 \times$ of the conventional one because the current flowing into the core is quadratically proportional to the gain when XDPs operate in the saturation region. Therefore, the proposed VCO topology shows better PN performance than conventional single-core VCOs.

IV. EXPERIMENTAL EVALUATIONS

To experimentally verify the advantages of the proposed VCO, a prototype design is implemented in a standard 130 nm bulk CMOS process with a core area of 0.15 mm² as shown in Fig. 4. The two LC cores can be coupled (decoupled) by turning on (off) the switch SW. A single-core VCO, i.e., the active LC core in our design, is used as the baseline to directly compare with ours on the same monolithic chip. The baseline only has capacitive tuning freedom. Additionally, since it inherently comes from our proposed VCO with the same non-ideal parasitic effects, thereby serving as a fair candidate for comparison to show the enhanced performance solely due to the contribution of the extra resistive tuning freedom.

Fig. 5 shows the frequency tuning curves of the two VCOs. The baseline yielded a 0.20 GHz ($3.03 \sim 3.23$ GHz, 6.4% FTR) bandwidth tuning as demonstrated in Fig. 5(a) by adjusting the control voltage of varactors. Such a tuning range corresponds to a capacitive tuning ability of [1.30, 1.50] pF. We then set the core capacitance to be 1.35 pF and 1.45 pF respectively. Fig. 5(b) exhibits the tuning curves corresponding to each capacitance value. At C = 1.35 pF (C = 1.45 pF), the proposed VCO achieves a tuning bandwidth of [2.77, 3.20] GHz ([2.63, 2.98] GHz) with the extra resistive tuning freedom. The results show that even with a slightly reduced amount of the capacitive tuning ability, the proposed VCO can realize a wider bandwidth tuning of 0.57 GHz ($2.63 \sim 3.20$ GHz, 20.2% FTR) by including the resistive tuning freedom, enabling a $3.1 \times$ FTR of the baseline. Note that this prototype only a small range of capacitive tuning ability (i.e., [1.30, 1.50] pF) is

TABLE I							
COMPARISONS BETWEEN THE PROPOSED VCO AND STATE-OF-THE-ART VCO	Os						

Reference	JSSC '13 [6]	TCAS-I '12 [4]	ISSCC '19 [12]	ISSCC '19 [7]	JSSC '17 [8]	This work
VCO types	Single-core	Single-core	Single-core	Dual-core	Quad-core	Dual-core
Optimization technique	Suppression of	Switched-coupled inductor,	Narrowband	Aggressive	Multi-core	No
	flicker noise	aggressive capacitive tuning	resonance at $2f_{osc}$	capacitive tuning		optimization
Technology	65 nm CMOS	90 nm CMOS	22 nm FDSOI	65 nm CMOS	55 nm BiCMOS	130 nm CMOS
Power supply (V)	1.2	1.2	0.15	0.65	1.2	1.2
Power (mW)	0.72	1.06	$0.91 \sim 1.22$	$17.5 \sim 21.6$	50	$2 \sim 4.31$
Area (mm ²)	0.0806	0.5	0.272	0.08	0.6	0.15
Tuning bandwidth (GHz)	$3.0 \sim 3.6$	$1.13 \sim 1.9$	$4.15 \sim 4.97$	$25 \sim 38$	$17.4 \sim 20.3$	$2.63 \sim 3.20$
FTR (%)	18.2%	50.8%	18%	41.2%	15.3%	20.2%
Resistive tuning	X	×	X	X	X	1
PN (dBc/Hz) (Average)	-112@1MHz	-117.2@1MHz	-141@10MHz	-116@3MHz	-106.5@1MHz	-120.3@1MHz
FoM (dB) ^a (Average)	183@1MHz	177.3@1MHz	193@10MHz	183@3MHz	187.5@1MHz	184@1MHz
FoM _T (dB) ^b (Average)	188.2@1MHz	191@1MHz	198@10MHz	195@3MHz	191@1MHz	190.1@1MHz

^a FoM = $|PN| + 20\log_{10}(f_{osc}/\Delta f) - 10\log_{10}(P_{DC}/1mW)$.

^b $\text{FoM}_{\text{T}} = \text{FoM} + 20\log_{10}(\text{FTR}/10\%).$



Fig. 6. PN comparisons of two VCOs across different oscillation frequencies.

included in this prototype, thereby achieving an FTR of 20%. By slightly increasing the capacitive tuning ability, the proposed VCO can readily realize a wider FTR.

We then show the PN of both VCOs. Particularly, we measure the PN at three frequency points for each VCO in its tuning bandwidth. For the proposed VCO, we choose such frequencies to be 2.84 GHz (low), 3.04 GHz (medium), and 3.22 GHz (high). While for the baseline VCO, we choose them to be 3.05 GHz (low), 3.12 GHz (medium), and 3.22 GHz (high). Fig. 6 shows the measured PN at 1 MHz offset frequency for the two VCOs. We observed that the PN of the proposed VCO is generally 1.5 dB better than the baseline across the different oscillation frequencies. Due to the parasitics of the switch connecting the two LC cores, the PN improvement is not as much as the ideal case discussed in Section III-B. However, these observations generally match well with the previous qualitative characterizations. Our results show that manipulating the gain-loss profile and their coupling provides a new method to extend the frequency tuning dimension beyond conventional capacitive/inductive tuning without compromising the PN performance for VCO design.

Additionally, we compare the proposed VCO with other

conventional VCOs, i.e., single-core VCOs, two-core VCOs, and quad-core VCOs that employ different tuning manners or coupling structures, as summarized in Table I. These conventional VCOs exploit different optimization techniques, such as aggressive capacitive tuning to reach wide FTR (TCAS-I '12 [4]), narrow band resonance at $2f_{osc}$ to boost PN performance (ISSCC '19 [12])), and multi cores to enhance PN performance (JSSC '17 [8]). However, our proposed VCO only includes a resistive tuning into design without any other optimization techniques. The comparison still shows its comparable FTR, PN, and figure-of-merit (FoM) with these prior arts. In summary, the resistive tuning of our proposed VCO topology is orthogonal with other capacitive/inductive tuning dimensions to enhance the performance of VCOs with diverse conventional topologies and optimization techniques.

V. CONCLUSION

A non-Hermitian physics-inspired topology of VCO is shown in this paper. The new topology enhances the FTR of existing VCOs with extra resistive tuning freedom. A prototype is implemented in a standard 130 nm CMOS process to demonstrate its advantages. The comparisons show that the resistive tuning of our proposed VCO topology is orthogonal with other capacitive/inductive tuning dimensions to enhance the performance of VCOs with diverse conventional topologies and optimization techniques. Future explorations can be performed by cascading multiple such VCOs in a one-dimensional chain similar to the one shown in prior work [13], which may also achieve topological oscillators.

REFERENCES

- F. Lv, X. Zheng, F. Zhao, J. Wang, S. Yue, Z. Wang, W. Cao, Y. He, C. Zhang, H. Jiang, and Z. Wang, "A power scalable 2-10FIX ME!!!!Gb/s PI-based clock data recovery for multilane applications," *Microelectronics Journal*, vol. 82, pp. 36–45, 2018.
- [2] N. Zhou, L. Wu, Z. Wang, X. Zheng, W. Cao, C. Zhang, F. Li, and Z. Wang, "A 28-Gb/s transmitter with 3-tap FFE and T-coil enhanced terminal in 65-nm CMOS technology," in 2016 14th IEEE International New Circuits and Systems Conference (NEWCAS), 2016, pp. 1–4.
- [3] W. Cao, Z. Wang, D. Li, X. Zheng, K. Huang, S. Yuan, F. Li, and Z. Wang, "A 40Gb/s 27mW 3-tap closed-loop decision feedback equalizer in 65nm CMOS," in 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS). IEEE, 2015, pp. 1–4.
- [4] A. I. et al, "A 1-mW 1.13–1.9 GHz CMOS LC VCO Using Shunt-Connected Switched-Coupled Inductors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 6, pp. 1145–1155, 2012.

- [5] Tanabe, Akira et al, "A 5–20GHz tunable LC-VCO using variable bridge inductor," in 2010 Symposium on VLSI Circuits, 2010, pp. 47–48.
- [6] F. Pepe, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "Suppression of Flicker Noise Up-Conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz Band," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2375–2389, 2013.
- [7] A. Bhat and N. Krishnapura, "26.3 A 25-to-38GHz, 195dB FoM_T LC QVCO in 65nm LP CMOS Using a 4-Port Dual-Mode Resonator for 5G Radios," in 2019 IEEE International Solid- State Circuits Conference - (ISSCC), 2019, pp. 412–414.
- [8] L. Iotti, A. Mazzanti, and F. Svelto, "Insights Into Phase-Noise Scaling in Switch-Coupled Multi-Core LC VCOs for E-Band Adaptive Modulation Links," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 7, pp. 1703–1718, 2017.
- [9] W. Deng, H. Jia, R. Wu, S. Sun, C. Li, Z. Wang, and B. Chi, "An 8.2-to-21.5 ghz dual-core quad-mode orthogonal-coupled vco with concurrently dual-output using parallel 8-shaped resonator," in 2021 IEEE Custom Integrated Circuits Conference (CICC), 2021, pp. 1–2.
- [10] W. Cao, C. Wang, W. Chen, S. Hu, H. Wang, L. Yang, and X. Zhang, "Fully integrated parity–time-symmetric electronics," *Nature nanotechnology*, vol. 17, no. 3, pp. 262–268, 2022.
- [11] Ş. K. Özdemir, S. Rotter, F. Nori, and L. Yang, "Parity-time symmetry and exceptional points in photonics," *Nature Materials*, vol. 18, no. 8, pp. 783–798, Aug 2019.
- [12] O. El-Aassar and G. M. Rebeiz, "26.5 A 0.1-to-0.2V Transformer-Based Switched-Mode Folded DCO in 22nm FDSOI With Active Step-Down Impedance Achieving 197dBc/Hz Peak FoM and 40MHz/V Frequency Pushing," in 2019 IEEE International Solid- State Circuits Conference -(ISSCC), 2019, pp. 416–418.
- [13] Y. Liu, W. Cao, W. Chen, H. Wang, L. Yang, and X. Zhang, "Fully integrated topological electronics," *Scientific reports*, vol. 12, no. 1, p. 13410, 2022.