

# Design Space Exploration of Dense and Sparse Mapping Schemes for RRAM Architectures

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**Abstract**—The impact of device and circuit-level effects in mixed-signal Resistive Random Access Memory (RRAM) accelerators typically manifest as performance degradation of Deep Learning (DL) algorithms, but the degree of impact varies based on algorithmic features. These include network architecture, capacity, weight distribution, and the type of inter-layer connections. Techniques are continuously emerging to efficiently train sparse neural networks, which may have activation sparsity, quantization, and memristive noise. In this paper, we present an extended Design Space Exploration (DSE) methodology to quantify the benefits and limitations of dense and sparse mapping schemes for a variety of network architectures. While sparsity of connectivity promotes less power consumption and is often optimized for extracting localized features, its performance on tiled RRAM arrays may be more susceptible to noise due to *under-parameterization*, when compared to dense mapping schemes. Moreover, we present a case study quantifying and formalizing the trade-offs of typical non-idealities introduced into 1-Transistor-1-Resistor (1T1R) tiled memristive architectures and the size of modular crossbar tiles using the CIFAR-10 dataset.

**Index Terms**—Memristor, RRAM, In-Memory Computing (IMC), Deep Learning, Design Space Exploration

## I. INTRODUCTION

HYBRID mixed-signal RRAM IMC systems are being used to efficiently perform inference of linear and unrolled convolutional layers in DL systems [1]–[5]. In recent years, a number of different dense and sparse mapping schemes have been proposed to reduce the required number of devices to perform inference of pre-trained Artificial Neural Networks (ANNs) [6]. However, the efficacy of different dense and sparse mapping schemes is not well understood with respect to different circuit and device parameters, typical non-idealities, and network architectures.

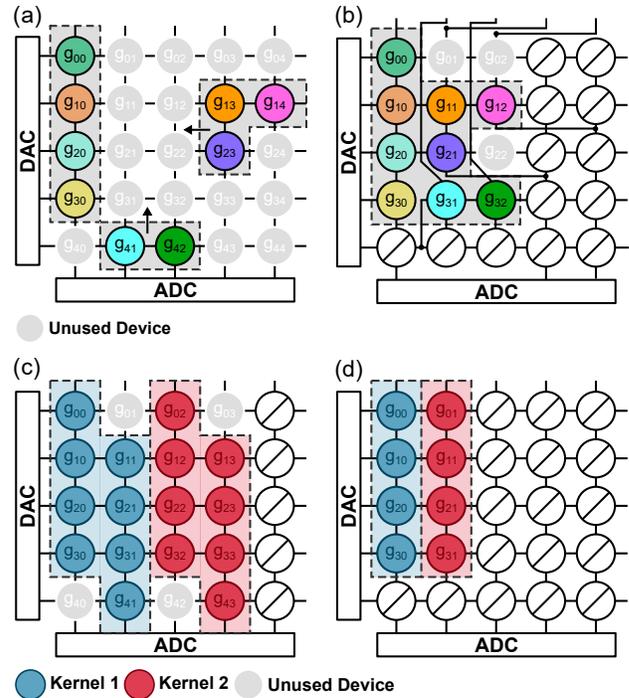


Fig. 1. Overview of four popular dense and sparse mapping schemes for RRAM architectures. When adopting a differential weight mapping scheme, (a-b) crossbar interconnects can be reconfigured to reduce the required number of devices and to reduce sparsity [7]. (c-d) For convolutional layers, kernels can either be mapped in a (c) staggered (sparse) or (d) dense arrangement, at the cost of increased read/write operations.

While various hardware-aware training routines [8]–[11] and generic search methodologies [12], [13] can be used to mitigate performance degradation when mapping pre-trained ANN architectures onto RRAM architectures, they are cumbersome, dependent on a pre-determined set of circuit and device parameters, and are not interpretable. Recently, Quantization-Aware Training (QAT) has demonstrated the

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ability to improve the performance of, and to robustly reduce the error of IMC implementations of pre-trained ANNs using RRAM devices with discrete conductance states [14]–[16]. However, it remains difficult to quantify performance trade-offs and limitations of dense and sparse mapping schemes without simulating them. In this paper, we present an extended DSE methodology to explore the efficacy of dense and sparse mapping schemes for RRAM architectures. Our methodology is able to explore the efficacy of dense and sparse mapping schemes for RRAM architectures without the requirement to simulate multiple dense and sparse schemes. Using our methodology, we quantify the benefits and limitations of dense and sparse mapping schemes for four popular Convolutional Neural Network (CNN) architectures.

## II. RELATED WORK

Related work in literature has attempted to quantify the various performance trade-offs in designing and implementing RRAM architectures with respect to many different device and circuit parameters. *Xu et al.* [17] studied RRAM architecture design, and primarily focused on the choices of different peripherals to achieve the best trade-off among performance, energy, and area. *Niu et al.* [18] performed a comprehensive analysis of issues related to reliability, energy consumption, area overhead, and performance. *Xu et al.* [19] investigated and discussed trade-offs involving voltage drop, write latency, and data patterns. *Matthew et al.* [20] presented a DSE framework to quantify trade-offs with respect to array sizes, write time and write energy. Recently, customizable simulation frameworks have been developed and used to simulate inference and/or training routines of RRAM architectures [21]–[24].

## III. PRELIMINARIES

### A. RRAM Crossbars

Modular crossbar tiles, comprised of smaller sized crossbar architectures with RRAM devices arranged in dual-column or dual-tile configurations, can be used to encode quantized analog weight-representations. By encoding  $M$  Word Line (WL) inputs as voltages, Vector-Matrix Multiplications (VMMs) can be performed in  $\mathcal{O}(1)$  [3], where analog dot products are realized along each of  $N$  Bit Lines (BLs), by exploiting Ohm’s law, i.e.,  $I_N = \sum_{i=0}^M V_N G_{N,M}$ .

### B. Conventional and Sparse Mapping Schemes

In Fig. 1, four popular conventional sparse (a,c) and dense (b,d) weight mapping schemes are depicted. For arbitrary crossbars adopting a differential weight mapping scheme, as depicted in Fig. 1 (b), interconnects can be rerouted at the cost of increased time complexity to reduce the required number of devices [7]. Specifically when mapping convolutional layers, as depicted in Fig. 1 (d), kernels can be mapped in a dense arrangement, at the cost of increased read/write operations.

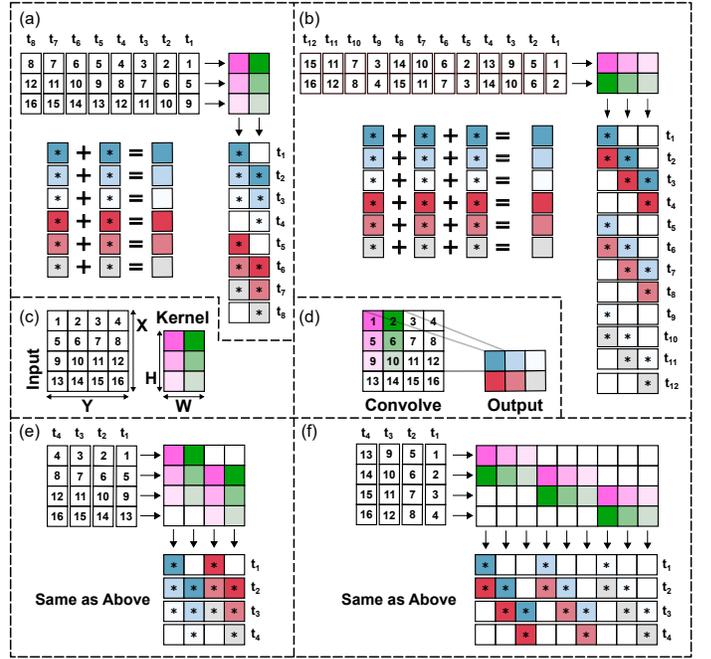


Fig. 2. Dense kernel mapping computation flows for (a) vertically and (b) horizontally orientated kernels. (c-d) Labels for inputs, kernels, and outputs. Sparse (staggered) kernel mapping computation flows for (e) vertically and (f) horizontally orientated kernels.

### C. Sparsity of Traditional ANNs

It has been shown empirically that ANNs can tolerate high levels of sparsity, and this property has been leveraged to enable the deployment of state-of-the-art models in severely resource constrained environments, with no significant performance degradation [25], [26]. Sparsity is most commonly introduced using L1-regularization and Dropout layers. By increasing network sparsity, an appropriately optimized array can reduce the required number of RRAM devices, as well as the overhead of Digital-to-Analog Converters (DACs), Analog-to-Digital Converters (ADCs), and peripheral circuitry.

## IV. PROPOSED DSE METHODOLOGY

We confine our proposed DSE search space to the following dimensions: the weight mapping scheme, I/O bit-width, tile size, maximum input encoding voltage, device/circuit non-idealities (see Section IV.B for further detail), mini-batch size, and regularization method(s). These can be categorized as network, mapping, or device/circuit related. Our proposed DSE methodology criteria consists of the following steps:

- ① For each bit-width and network architecture to investigate, QAT is performed using a pre-determined dataset.
- ② Ranges of each dimension (for dimensions which are not fixed to a singular value) are determined.
- ③ Using Simulation Program with Integrated Circuit Emphasis (SPICE)-based circuit simulation tools, or RRAM-based DL simulation frameworks, the test or validation set accuracy for the pre-determined dataset is determined using either (a) Bayesian Optimization, or (b) a grid-search, exploring the search space. Eqs. (1) –

(3) are used to determine the number of required devices, tiles, and computational steps, for each configuration, after simulating one mapping scheme. ④ Contour plots are generated to explore the efficacy of different network parameters, and device/circuit parameters, using the test or validation set accuracy as the objective function. ⑤ A score is determined for each configuration, weighting the number of required devices, tiles, and the test and/or validation set accuracy. ⑥ Scores are manually compared.

When the scheme depicted in Fig 1(b) was used, we assumed that convolutional kernels were mapped densely. Space requirements for convolutional and linear layers of the dense mapping schemes depicted in Fig 1(b) can be determined using routing algorithms, where the size of modular crossbar tiles and location of zero weights are known [7]. Space requirements for convolutional layers of sparse and dense mapping schemes depicted in Fig 1(c) and Fig 1(d) can be determined without being physically laid out and simulated using (1) and (2), respectively, where  $H$ ,  $W$ ,  $X$ , and  $Y$  are defined in Fig 2.  $D$  denotes dilation,  $K$  denotes the number of kernels, and  $S$  denotes the stride. For 1d-convolutional layers,  $W = 1$ .

$$D_{\text{req\_sparse}} = \frac{K^2 XW[(X + 2P - D(H - 1) - 1)]}{S + 1} \quad (1)$$

$$D_{\text{req\_dense}} = KHW \quad (2)$$

The required number of computational steps in Fig 1(d) can be determined using (3)

$$C_{\text{diff\_sparse}} = \frac{X + 2P - D(H - 1) - 1}{S + 1}. \quad (3)$$

## V. A CASE STUDY

In this Section, we present a case study investigating the performance of different 1T1R RRAM architectures used to perform inference of linear and unrolled convolutional layers within popular CNN architectures using the CIFAR-10 dataset. For all implementations, a dual-column differential weight representation scheme was adopted.

### A. Network Architectures and QAT

To ensure a sufficiently large design space was explored, we investigated the performance of four popular network architectures. A batch size of 256 and 257 training epochs were used for all implementations, with the RMSProp optimizer and a learning rate of 0.001512, which demonstrated significant performance empirically. To investigate the effect of network sparsity, for all implementations, the L1 weight-decay was set to  $5e-4$ . The Xilinx Brevitas [27] library was used in conjunction with the PyTorch [28] Machine Learning (ML) library to train all baseline network architectures. The weight sparsity and test set accuracy of each baseline implementation is presented in Table I.

### B. Device Non-Idealities

In all simulations, the following device non-idealities were accounted for: device-to-device variability, a finite number

TABLE I  
THE PERFORMANCE AND SPARSITY OF EACH BASELINE NETWORK ARCHITECTURE.

Architecture	Bit-Width	Zero Weight Values	Test Accuracy (%)
VGG-16 [30]	4	189,020/15,239,872 (1.24%)	86.24
	6	237,869/15,239,872 (1.56%)	87.96
	8	240,454/15,239,872 (1.58%)	87.88
ResNeXt29 2x64d [31]	4	109,100/9,103,552 (1.20%)	85.70
	6	341,462/9,103,552 (3.75%)	85.89
	8	190,482/9,103,552 (2.09%)	84.21
MobileNetV2 [32]	4	74,318/2,261,824 (3.29%)	87.57
	6	95,521/2,261,824 (4.22%)	88.48
	8	123,501/2,261,824 (5.46%)	88.48
GoogLeNet [33]	4	570,755/6,142,528 (9.29%)	55.19
	6	102,490/6,142,528 (1.67%)	86.17
	8	266,513/6,142,528 (4.32%)	86.72

of conductance states, and stuck  $R_{\text{ON}}$  and  $R_{\text{OFF}}$  devices (including those that have failed to electroform). We note that, while only three non-ideal device characteristics were investigated, more could easily be added, such as conductance drift and endurance and retention characteristics [29].

### C. Modular Crossbar Tile Size

For all implementations, modular symmetric crossbar tiles were used to mitigate the effects of non-ideal device and circuit characteristics. We investigated the following modular crossbar tile sizes:  $(32 \times 32)$ ,  $(64 \times 64)$ ,  $(128 \times 128)$ , and  $(256 \times 256)$ .

### D. Results

To apply our DSE methodology, we determined the optimal batch size and tile shape (of symmetric tiles) for inference, as depicted in Fig. 3. In addition, we reported the best of a normalized device-read/write-accuracy weighted score, alongside: the required number of devices, required number of read/write operations, and the test set accuracy. For each architecture and bit-width, the optimal batch and tile sizes were determined with respect to the test set accuracy. The performance of these configurations are presented in Table II. To simulate RRAM architectures, the MemTorch [21] simulation framework was used. The following fixed parameters were used to reduce the dimensionality of the explored design space:  $R_{\text{OFF}}$  was sampled from a normal distribution with a mean of 100k $\Omega$  and a standard deviation of 10,000.  $R_{\text{ON}}$  was sampled from a normal distribution with a mean of 10k $\Omega$  and a standard deviation of 1,000. A maximum encoding input voltage of 0.3V was used [34], with a failure rate of stuck devices to  $R_{\text{ON}}$  of 0.5%, and a failure rate of stuck devices to  $R_{\text{OFF}}$  of 0.5%. The range of terms used to compute the weighted score can be standardized to reduce biases, and depending on specific user requirements, different weightings can be applied.

## VI. DISCUSSION AND CONCLUSIONS

In Table II, it can be observed that MobileNetV2 with a batch size of 256 and a tile size of 64 achieved the best normalized weighted score. As can be seen in Fig. 3, for all network architectures other than GoogLeNet, the batch size used during inference had a negligible influence on the

TABLE II  
BEST CONFIGURATION FOR EACH UNIQUE ARCHITECTURE AND BIT-WIDTH.

Configuration			Required Devices (RD)				Read/Write Operations (RWO)			Test Set Accuracy (TSA) (%)	Normalized Weighted Score = [TSA / (RD × RWO)] <sup>†</sup>		
Architecture	Batch Size/ Tile Size	Bit-Width	Sparse/ Staggered	Dense (A) <sup>◊</sup>	Dense (B) <sup>†</sup>	Sparse/ Staggered	Dense (A) <sup>◊</sup>	Dense (B) <sup>†</sup>	Sparse/ Staggered		Dense (A) <sup>◊</sup>	Dense (B) <sup>†</sup>	
VGG-16	256/64	4	15,016x64x64	3,531x64x64	3,705x64x64	143x64	2,135x64	2,591x64	86.10	<b>0.4947</b>	0.1403	0.1098	
	256/32	6	60,063x32x32	14,077x32x32	14,818x32x32	566x32	8,048x32	10,340x32	87.86	<b>0.2546</b>	0.0758	0.0557	
	256/32	8	60,063x32x32	14,072x32x32	14,818x32x32	566x32	8,121x32	10,340x32	87.74	<b>0.2543</b>	0.0748	0.0557	
ResNeXt29	256/64	4	243,653x64x64	2,184x64x64	2,213x64x64	657x64	24,266x64	24,712x64	83.87	0.0055	<b>0.0186</b>	0.0180	
	64/64	6	243,653x64x64	2,070x64x64	2,213x64x64	657x64	22,681x64	24,712x64	86.08	0.0057	<b>0.0217</b>	0.0185	
	256/64	8	243,653x64x64	2,165x64x64	2,213x64x64	657x64	24,712x64	24,712x64	82.28	0.0054	<b>0.0180</b>	0.0176	
MobileNetV2	256/64	4	48,590x64x64	528x64x64	548x64x64	220x64	2,181x64	2,406x64	76.85	0.0878	<b>0.8251</b>	0.7182	
	256/32	6	194,257x32x32	2,092x32x32	2,191x32x32	875x32	8,525x32	9,524x32	88.71	0.0505	<b>0.4914</b>	0.4201	
	256/64	8	48,590x64x64	516x64x64	548x64x64	220x64	2,119x64	2,406x64	88.52	0.1014	<b>1.0000</b>	0.8283	
GoogLeNet	16/64	4	561,915x64x64	1,345x64x64	1,481x64x64	1,246x64	15,142x64	17,552x64	55.54	0.0000	<b>0.0327</b>	0.0254	
	16/256	6	35,120x256x256	91x256x256	92x256x256	79x256	1,068x256	1,127x256	85.58	0.0050	<b>0.1691</b>	0.1584	
	16/128	8	140,479x128x128	354x128x128	371x128x128	312x128	4,207x128	4,417x128	86.58	0.0021	<b>0.0888</b>	0.0470	

<sup>◊</sup>Dense (A) refers to the dense mapping scheme depicted in Fig. 1 (b). <sup>†</sup>Dense (B) refers to the dense mapping scheme depicted in Fig. 1 (d). <sup>†</sup>Min-max normalization of weight scores is performed to aid comparisons.

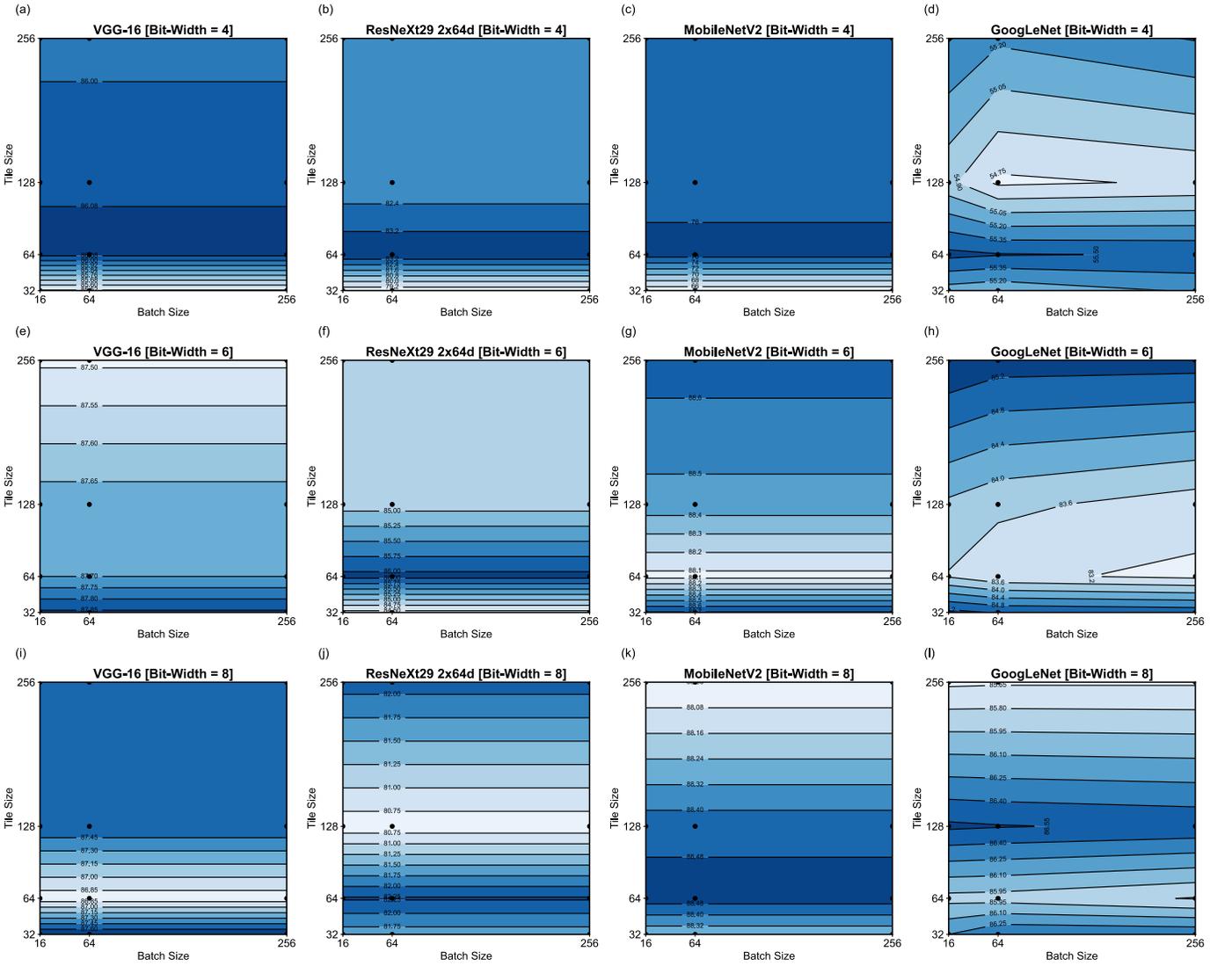


Fig. 3. Contour plots depicting the dependency of the test set accuracy on symmetrical tile sizes, the batch size, and the bit-width of simulated RRAM architectures, for each network architecture. Different tile shapes and batch sizes are explored for bit-widths of (a-d) 4, (e-h) 6, and (i-l) 8, respectively. Fixed seed values of 0 were used to ensure the same stochastic non-idealities were sampled during each simulation.

test set accuracy. Our empirical results indicate that for the investigated networks, symmetrical tiles with a size of  $\geq 64$  where deemed optimal. For all network architectures, the optimal tile shape was found to be dependent on both the network architecture used and the bit-width. This suggests that the optimal tile size for pre-trained CNNs cannot easily be determined without performing an exploratory analysis. Despite being limited in scope, we believe that the case study in Section V demonstrates the effectiveness of our presented DSE methodology to investigate and determine dependencies between different search space dimensions.

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