Systematic Design For Multistage Feed-forward Op-amp For High-Speed Continuous-Time $\Sigma\Delta$ ADCs

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***Abstract*—This paper presents a systematic design methodology for multi-stage feed-forward op-amps used in the active filters of continuous time $\Sigma\Delta$ ADC. This methodology can provide the specifications of each stage in the op-amp (from 2 stages to 4 stages) based on the required ADC specifications and can provide an estimate of the Signal to Noise Ratio (SNR) taking into consideration the effect of the transfer function of the op-amp. This method is then validated on a Lowpass and Bandpass $\Sigma\Delta$ ADCs.**

***Index Terms*—Continuous-time Sigma Delta ADC, High speed, Active Filters, Multistage Feed-forward Op-amp, Systematic Design.**

I. Introduction

Multi standard receivers are now needed more than before due to the emerge of new mobile standards standards such as 5G and 6G in the future, these new standards plus the old ones require the receiver to cover multiple bands in the electromagnetic spectrum. These requirements require high speed ADCs or wide tunable ADCs to cover all these ranges..

Continuous time sigma delta (CT$\Sigma\Delta$) ADCs are widely used for multistandard applications or Software Defined Radios (SDR), this is due to their low power consumption, inherent anti-aliasing filter and their ability to be widely tuned, the filters used in these ADCs are either passive filters as in [1] or active as in [2] and [3].

Active filters have the advantage of low area when compared to passive ones which uses inductors. but they require complex opamps to achieve high gain and unity gain frequency in GHz range. Usually multistage feedforward opamps are used as they can reach high gain and speed [4], but their design requirements become more difficult as the number of stages increase. Many studies tried to find a systematic design for these opamps as in [5] which proposed a design procedure for 4th order multistage feedforward opamp but it is based on many assumptions and requires several iterations to achieve the required specifications, also the choice of specifications has no connection with the ADC requirements (SNR, Fs, and so on) and these lead to high power consumption in order to get as high gain and BW as possible. Another study [6] introduced a gm/ID methodology for designing these opamps but it has some unanswered questions, for example there is no methodology to determine which transfer function should be chosen for the ADC as there is no simulation or test to determine the effect of gain and BW of each stage on SNR. Also, the opamp specifications are not based on system level design as it also tried to get high gain and BW even if the ADC doesn't require these values.

This paper presents a systematic design methodology for the multistage feedforward op-amps needed in the design of the active filter, this methodology simplifies the op-amp by dividing it into several single stage op-amps with gain and bandwidth specification for each stage. The produced specifications are verified in system level and in schematic level using 2 CT$\Sigma\Delta$ ADCs, a 4th order feedforward lowpass ADC and a 4th order feedback bandpass ADC.

This paper is organized as follows. Section II explains Multistage Feedforward Opamp Systematic Design. Section III shows system level design examples. Section IV presents Simulation results for a schematic Lowpass and Bandpass CT$\Sigma\Delta$ ADCs and compare the results with MATLAB.

II. Multistage Feedforward Opamp Systematic Design

Fig. 1 shows a block diagram for the FF opamp, where H_{am1},H_{am2},and H_{af2} represents a 2 stage FF opamp, and if H_{am3} and H_{af3} are added, we get 3 stage FF opamp and same for the 4 stages FF opamp. The high gain can be achieved from the main path $H_{am1,2,3,4}$ while the high speed is achieved from the FF path $H_{af2,3,4}$. As the number of FF stages increase, the design complexity of the FF opamp increases.

The proposed MATLAB tool can help in designing the FF opamp up to 4 stages. It needs only the ADC specifications (OSR, BW, Fo) and then (with some assumptions) produce the specifications (Gain and BW) required of each stage.

A. Quantitative analysis

The first step is to generate the transfer function of the 2,3, and 4 stages FF opamp, each stage is assumed to be a single

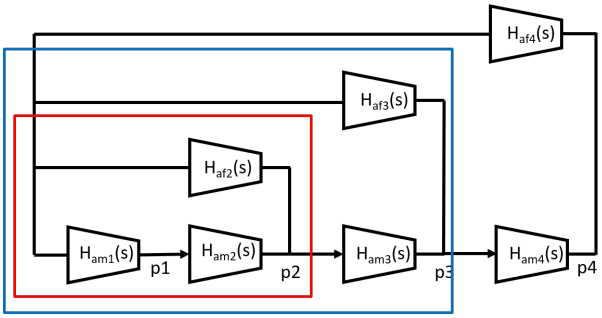

Fig. 1: Multistage Feedforward Compensated Opamp

pole amplifier with transfer function:

$$H(s) = \frac{A}{1 + \frac{s}{w}} \tag{1}$$

where A is the DC gain and w is the first pole in rad/sec. Then the transfer function (TF) and DC gain can be easily derived using hand analysis but as number of stages increases beyond 2, it becomes difficult to derive the TF so a mathematical tool can be used here to get the transfer function where the general form can be written as

$$\begin{aligned} TF(s) &= (H_{am1}H_{am2}H_{am3}H_{am4}...+ \\ &\quad H_{af2}(H_{am3}H_{am4}.....)+ \\ &\quad H_{af3}(H_{am4}H_{am5}H_{am6}).... + ... \\ &= \prod_{i=1}^{n} H_{ami} + H_{af2}\prod_{i=3}^{n} H_{ami} \\ &\quad + H_{af3}\prod_{i=4}^{n} H_{ami} + ... + H_{afn} \end{aligned} \tag{2}$$

from equation (2) we can derive the 3 stage FF opamp transfer function as

$$\begin{aligned} TF(s) = &\frac{Am1\ Am2\ Am3}{\left(\frac{s}{w1}+1\right)\left(\frac{s}{w2}+1\right)\left(\frac{s}{w3}+1\right)} + \\ &\frac{Af2\ Am3}{\left(\frac{s}{w2}+1\right)\left(\frac{s}{w3}+1\right)} + \\ &\frac{Af3}{\frac{s}{w3}+1} \end{aligned} \tag{3}$$

with DC gain equals to

$$DC\ Gain = Am1Am2Am3 + Af2Am3 + Af3 \tag{4}$$

and 4 stage FF opamp transfer function

$$\begin{aligned} TF(s) = &\frac{Am1\ Am2\ Am3\ Am4}{\left(\frac{s}{w1}+1\right)\left(\frac{s}{w2}+1\right)\left(\frac{s}{w3}+1\right)\left(\frac{s}{w4}+1\right)} + \\ &\frac{Af2\ Am3\ Am4}{\left(\frac{s}{w2}+1\right)\left(\frac{s}{w3}+1\right)\left(\frac{s}{w4}+1\right)} + \\ &\frac{Af3\ Am4}{\left(\frac{s}{w3}+1\right)\left(\frac{s}{w4}+1\right)} + \frac{Af4}{\frac{s}{w4}+1} \end{aligned} \tag{5}$$

and DC gain equals

$$\begin{aligned} DC\ Gain = &Am1Am2Am3Am4 + \\ &Af2Am3Am4 + Af3Am4 + Af4 \end{aligned} \tag{6}$$

Finding DC gain for each stage is not a problem since its equation is easy to derive as in equations (4), and (6), but other specifications as phase margin (PM), bandwidth (BW), unity gain bandwidth (fu) are difficult to determine especially with number of stages > 2.

Using MATLAB, these specifications can be found easily, but to increase the run speed, some assumptions are made as $Ami = Afi$ and Ami and Afi have same pole at wi. To make sure these assumptions will not cause problems inside the $\Sigma\Delta$ ADC, after finding the required specification, a matrix of transfer functions are built and tested in a simulink model for the ADC to determine the SNR.

III. Design Examples

To test the efficiency of the tool, it was used to generate the specifications of 4th order lowpass and bandpass $\Sigma\Delta$ ADCs.

A. 2 stage FF opamp

This example shows the generated specifications of 2 stage opamp for lowpass $\Sigma\Delta$ ADC. The inputs to the tool are shown in table I. The generated minimum requirements are shown in table II

TABLE I: Inputs for 2 stages opamp

Input Parameters	Value
$F0_{normalized}$	0
OSR	64
$Fs_{normalized}$	1
Opamp Order	2

TABLE II: Generated minimum requirements for 2 stages opamp

Input Parameters	Equation	Value
DC Gain (dB)	$20log_{10}(OSR)$	36
3 dB $BW_{normalized}$	$\frac{Fs}{2\ OSR}$	0.0078125
Phase margin (PM)	-	60
$Unity\ gain\ frequency\ (Fu)_{norm}$	Fs	1

The generated specifications have bode plot as shown in Fig. 2, then these transfer functions are tried in the 4th order lowpass $\Sigma\Delta$ ADC. Fig. 3 shows the power spectral densities (PSD) of the ADC using the generated 2 stages opamps.

Table V shows part of the generated specifications and the simulated SNR. where P1,2 are the normalized 1st pole of each stage (Hz)

B. 3 stage FF opamp

Another example is done using 3 stage FF opamp for the same ADC in the previous example. The inputs to the tool and the minimum requirements are the same as that in table I and II (except for the opamp order).

The bode plot is shown in Fig. 4, then these transfer functions are tested in the 4th order lowpass $\Sigma\Delta$ ADC. Table V shows the SNR Values.

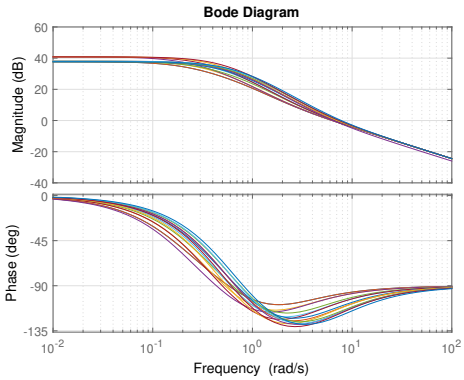

Fig. 2: Bode plot of the generated 2 stage opamp specifications

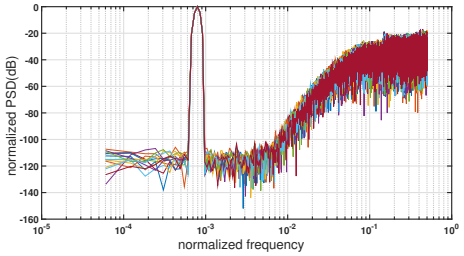

Fig. 3: PSD of 4th order lowpass ΣΔ ADC using 2 stage opamp

Table V shows part of the generated specifications and the simulated SNR.

C. 4 stage FF opamp

The 4 stages FF opamp specifications are generated for a 4th order BP CTΣΔ ADC. The inputs to the tool are shown in table III. The generated minimum requirements are shown in table IV and they are tested in simulink model to get the SNR. The most stringent requirement here is the ADC 3-dB BW which should be at Fo (normally Fo is in GHz range for high speed ADCs), so 3-dB BW is set to 10* ADC BW for more power efficient design and the limited gain at Fo will be handled in next chapters.

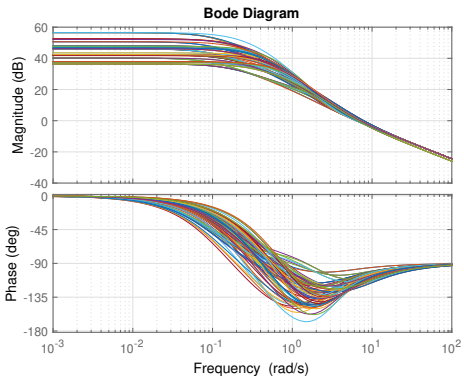

Fig. 4: Bode plot of the generated 3 stages opamp specifications

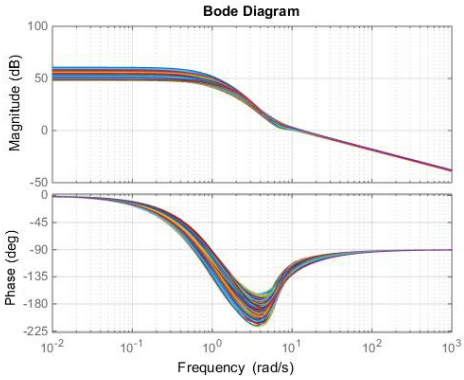

Fig. 5: Bode plot of the generated 4 stages opamp specifications

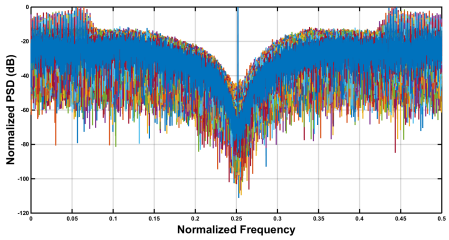

Fig. 6: PSD of 4th order bandpass ΣΔ ADC using 4 stages opamp

TABLE III: Inputs for 4 stages opamp

Input Parameters	Value
$F0_{normalized}$	0.25
OSR	64
$Fs_{normalized}$	1
Opamp Order	4

TABLE IV: Generated minimum requirements for 4 stages opamp

Input Parameters	Equation	Value
DC Gain (dB)	$20log_{10}(OSR)$	36
$3\ dB\ BW_{normalized}$	$10 * \frac{Fs}{2\ OSR}$	0.078125
Phase margin (PM)	-	60
$Unity\ gain\ frequency\ (Fu)_{norm}$	1.5 Fs	1.5

The bode plot is shown in Fig. 5, then these transfer functions are tried in the 4th order bandpass ΣΔ ADC. Fig. 6 shows the PSD of the ADC using the generated 4 stages opamps.

Table V shows part of the generated specifications and the simulated SNR.

IV. Simulation Results

After verifying the systematic flow in MATLAB, the flow is repeated to verify the idea in transistor level. From table

TABLE V: Generated results for the 2, 3 and 4 stages opamp

Number of stages	A1	A2	A3	A4	P1	P2	P3	P4	Gain (dB)	3 dB BW	PM	Fu	SNR LP (dB)	SNR BP (dB)
2	10	7	-	-	0.03	0.14	-	-	37.73	0.03	80.31	1	89.8	28.8
2	7	10	-	-	0.05	0.1	-	-	38.06	0.04	78.17	1.01	87.3	29.7
2	10	10	-	-	0.08	0.1	-	-	40.8	0.06	61.9	1.18	95.2	31.6
2	10	7	-	-	0.1	0.14	-	-	37.73	0.07	60.4	1.24	92.1	29.9
3	7	3	3	-	0.022	0.27	0.26	-	37.5	0.022	69	1.02	92.0	34.6
3	10	3	3	-	0.016	0.26	0.26	-	40.2	0.016	69	1.01	93.2	35.2
3	7	4	3	-	0.022	0.19	0.26	-	39.9	0.023	67	1.00	88.5	31.8
3	10	3	7	-	0.016	0.26	0.11	-	47.5	0.015	61	1.04	96.4	40.1
4	4	4	4	3	0.16	0.24	0.32	0.64	48.13	0.11	65.96	1.78	99.1	48.1
4	3	7	3	4	0.21	0.16	0.48	0.52	50.93	0.11	62.31	2.03	99.2	51.7
4	4	7	4	7	0.2	0.14	0.32	0.29	60.12	0.09	60.91	1.95	99.5	57.01
4	7	4	3	3	0.11	0.24	0.48	0.64	49.54	0.09	66.22	1.89	99.0	46.25

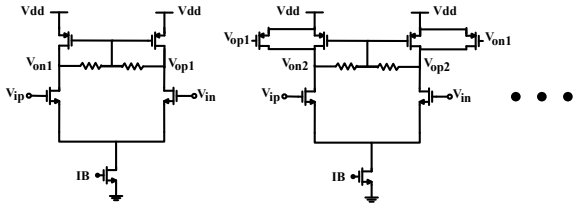

Fig. 7: Schematic of 4 stages opamp

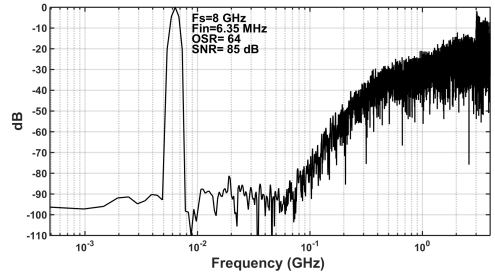

Fig. 8: Output Power Spectral Density for lowpass ADC

V, we can see that the bold rows give accepted SNR for both lowpass and bandpass but the first row has reasonable opamp specifications, as the 2nd bold row requires 60 dB gain and nearly 2*Fs which is not power efficient option especially at GHz Fs although it gives better SNR but . A 4th order FF lowpass CT$\Sigma\Delta$ and a 4th order FB bandpass CT$\Sigma\Delta$ (same as in [7]) are designed to test the systematic method in transistor level. Table VI shows the ADC specifications and

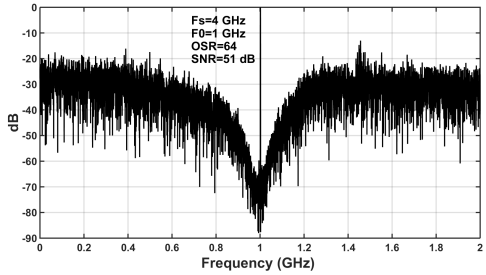

Fig. 9: Output Power Spectral Density for bandpass ADC

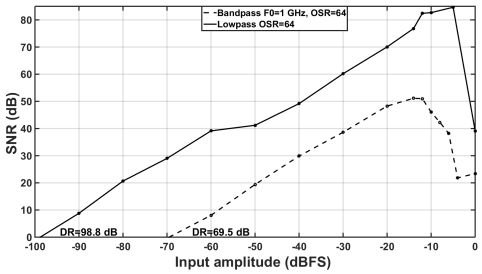

Fig. 10: SNR Vs Input amplitude

TABLE VI: MATLAB Vs Schematic Results

	Lowpass CT$\Sigma\Delta$	Bandpass CT$\Sigma\Delta$
Order	4th oder FF	4th order FB
Tech. (nm)	28-FDSOI	
VDD (V)	1.0/1.5	
Fs (GHz)	8	4
OSR	64	
SNR (MATLAB) (dB)	99.2	52
SNR (Transistor Level) (dB)	85	51

a comparison between MATLAB and Schematic level SNRs. It can be seen that MATLAB and Schematic level results are within accepted range taking into consideration the comparator and DACs effects and thermal noise, the opamp schematic is shown in Fig.7 (3rd and 4th stages are similar to 2nd stage).

Fig.8 and Fig.9 shows the power spectral density (PSD) for both the lowpass and bandpass respectively. Fig.10 shows SNR versus input amplitude for both ADCs resulting dynamic range of 98.8 dB for lowpass and 69.5 dB for bandpass.

V. Conclusion

A systematic design methodology for multistage feedforward op-amp targeting CT$\Sigma\Delta$ ADCs is presented using MATLAB where the proposed tool gets the ADC required specifications then produce the needed gain and bandwidth for each stage. the results are verified using simulink models and transistor level example for both LP and BP CT$\Sigma\Delta$ ADC.

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