

A CMOS-based Characterisation Platform for Emerging RRAM Technologies

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Abstract—Mass characterisation of emerging memory devices is an essential step in modelling their behaviour for integration within a standard design flow for existing integrated circuit designers. This work develops a novel characterisation platform for emerging resistive devices with a capacity of up to 1 million devices on-chip. Split into four independent sub-arrays, it contains on-chip column-parallel DACs for fast voltage programming of the DUT. On-chip readout circuits with ADCs are also available for fast read operations covering 5-decades of input current (20 nA to 2 mA). This allows a device’s resistance range to be between 1k Ω and 10M Ω with a minimum voltage range of ± 1.5 V on the device.

Index Terms—ReRAM, RRAM, memristor, characterisation, array

I. INTRODUCTION

Emerging memory technologies including resistive random access memory (ReRAM/RRAM) [1]–[4] provide potential solutions to the challenges faced by current memories due to their lower power consumption, scalability, non-volatility and high-speed operation. Apart from the typical use case as computer memory, such devices have other uses in applications such as in-memory computing [5], [6] and FPGAs [7], [8]. A common criteria of these applications is the use of large arrays with millions, billions or more of devices in a single chip [9]. Such scale brings additional challenges to these emerging technologies which need to be solved before reaching their full potential.

One such challenge is variability of a device’s state as the interfacing periphery circuitry should satisfy the entire working range to ensure optimal operation. Another challenge is the yield of the device and/or integration process [10], [11]. Being able to measure, model [12] and optimise this as per the application is vital in prolonging the life-span of the product.

Several of these emerging memory technologies are two terminal devices that operate by varying their port-to-port resistance [10], [13]. Varying this resistance is enabled by applying a voltage/current pulse/s within a set range, whilst reading the resistance is executed by using conventional methods; apply current and read voltage drop or vice-versa. Thus whilst characterising a few devices is possible using bench-top equipment [14], mass characterisation of devices

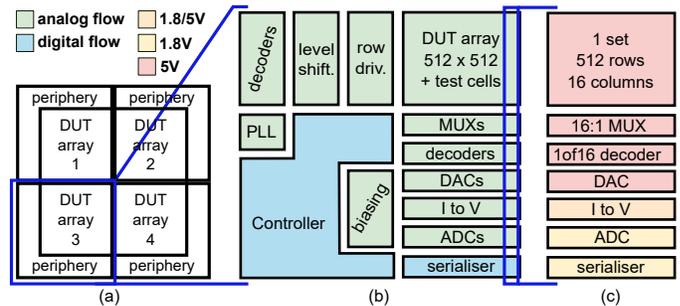


Fig. 1. System architecture: (a) Top level view; (b) array focused; (c) set focused.

requires a custom PCB [15]–[18] or chip-based platform [19]. Whilst a PCB-based platform is easy to customise, it limits the operation and number of devices under test (DUTs) due to the parasitic resistance and capacitance connected to the devices. On the other hand, a chip-based platform minimises the parasitics, enabling higher speed of operation whilst the DUTs are integrated within an environment that is also typical of the application.

This paper presents the top-level architecture to a novel chip-based characterisation platform for emerging resistive memory technologies with the capability of testing up to 1 million devices integrated on top of a 180 nm CMOS process. Section II describes the system architecture and design implementation. Section III then covers the DUT - CMOS integration process step for the case of RRAM. Section IV presents simulated results and Section V concludes the work.

II. SYSTEM ARCHITECTURE

Fig. 1 shows a simplified block diagram of the proposed characterisation platform. The platform consists of 4 identical and independently controlled sub-arrays, each with 512 rows and columns, bringing the total to 1 million 1T1R cells on chip. Due to layout constraints, 16 columns (also referred to as a set) share the same column-parallel circuitry which consists of a DAC, a current-to-voltage (I to V) converter, and an ADC. This enables 32 devices to be characterised in parallel from each sub-array at any time, with a total of 128 devices when

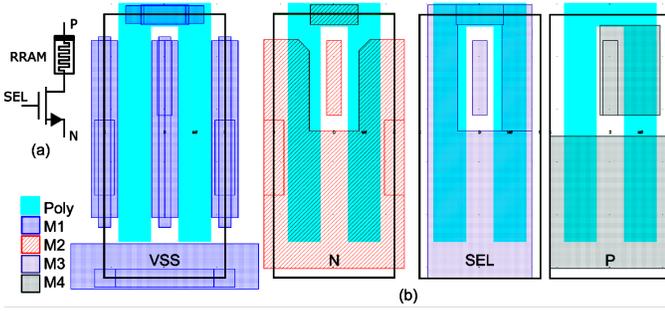


Fig. 2. 1T1R cell; (a) schematic using a nMOS transistor with W/L of $7.4\ \mu\text{m}/0.6\ \mu\text{m}$; (b) layout of cell and metal layers above the transistor; M2 for net N , M3 for net SEL and M4 for net P and intermediate DUT-nMOS net.

all sub-arrays are operational. All data from the 32 sets is then sent off-chip through a serialiser. System control is done through the on-chip controller fully configured through the SPI interface.

A. 1T1R Cell

The standard 1T1R structure (Fig. 2(a)) is designed with a 5 V nMOS transistor and a RRAM whose minimum resistance is assumed to be $1\ \text{k}\Omega$. It allows writing the RRAM in both forward and reversed direction by setting terminal P/N to a specific voltage up to 5 V and the other terminal N/P to 0 V. To satisfy the RRAM writing scheme, 1.5 V in both directions is required to change the device's state. As a result, an nMOS transistor is chosen due to a higher mobility than a same sized pMOS, thus minimising cell footprint. For the layout in Fig. 2(b), the RRAM is placed above the transistor to maximise the cell density as explained further in Section 4 resulting in cell dimensions of $5\ \mu\text{m} \times 2.28\ \mu\text{m}$, which are mainly determined by the size of the transistor. Each signal path is extended to cover as much area as possible to reduce the parasitic resistance of the track and enable faster settling times throughout the array.

B. Row Circuits

The row circuits consist of digital circuits to select one or more rows at a given time. Selecting just one cell is possible through the use of an address decoder which takes the gray-coded address provided by the controller and enables the corresponding row. Once a row is enabled, an independent *select* signal is then used to control the duration of the pulse. This gives finer control over the pulse width.

C. Column Circuits

The objective of the column circuits is two-fold; (1) apply a voltage across a DUT, and (2) measure the current flowing through it. This is possible through the circuits described below.

1) *Column Switches and Decoder*: Due to layout constraints a number of columns share the same set circuitry. As a result, analog switches are used to route the appropriate column to the circuit in use. The first level implements an analog multiplexer to enable one column out of the available

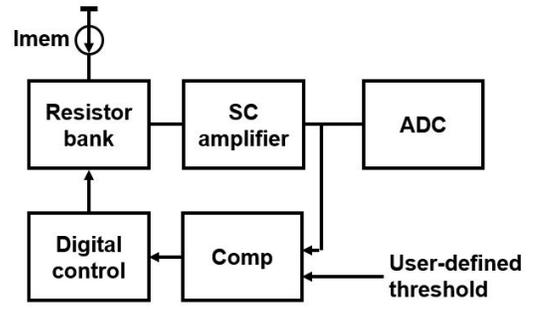


Fig. 3. A block diagram of the proposed readout system.

16 in a set. These switches are controlled by a decoder that takes a 4-bit binary input and enables a single column. The second level determines the polarity of the voltage applied to the P and N lines of the selected column. This is very similar to an H-bridge configuration, with the column of interest being the driven load.

2) *DAC*: This DAC generates the specified voltage to drive the DUT array to perform the desirable sweeps or characterisation procedures. The challenge for this DAC design is to drive a wide load range from $1\ \text{k}\Omega$ to $5\ \text{M}\Omega$. Also, its desired voltage output range is defined as 50 mV to 4 V (range decreases for low resistance). A traditional 8-bit voltage-mode R-2R DAC is implemented with 5 V MOSFETs to achieve an output range from 50 mV to 4.9 V. However, the final output range is determined by a high-drive strength rail-to-rail output buffer. This buffer uses a conventional complementary rail-to-rail amplifier together with a constant-gm circuit [20] as the input stage. Also, the indirect compensation technique [21] is used at the output stage to ensure a good phase margin and high unity-gain frequency for a wide load range.

3) *Current-To-Voltage Converter*: To enable an on-chip and fast characterisation, an on-chip readout system is implemented of which a block-level overview is depicted in Fig. 3. By configuring the DAC, a user-defined reading voltage is applied to the DUT, that generates a specific current based on resistance of the DUT that flows from the DAC, through the DUT and finally through the current-to-voltage converter. This current signal is captured, converted and amplified in the proposed readout system.

A 5-stage logarithmic resistor bank is employed to convert the input current to a voltage-mode signal for amplification. A switched-capacitor (SC) amplifier is then used to amplify the small output voltage of the resistor bank to ensure proper use of the full input range of the ADC. To keep the voltage across the resistor bank within a small range (less than 50 mV), a comparator with a programmable threshold is used. Additionally this threshold determines the voltage range at the output of the amplifier which is then fed to the ADC. The algorithm used for the resistor bank control is very similar to that found in an SAR ADC. The resistor with the lowest resistance is activated during the first clock cycle and the amplified output is compared with the threshold. If the output is higher, the algorithm terminates here. In the other instance, the algorithm moves to the next resistor and repeats the process

until the amplified output is either larger than the threshold, or the last resistor has been selected. When terminated the state of the selected resistor is stored and sent to the serialiser for off-chip data transfer.

4) *ADC*: A 12-bit SAR ADC digitises the resulting voltage from the preceding I-to-V converter block. It has been designed to operate with a sampling frequency of 250 kHz and an input range 0.1 V to 1.7 V. The two major challenges in this design have been: (1) minimising power consumption and (2) 12-bit resolution without on-chip calibration. This ADC consists of shift registers for timing signal generation, a capacitor type DAC, and a dynamic comparator. The DAC employs a fully differential C-2C capacitor array to minimise effects due to parasitic capacitance. It directly uses the bottom plate of capacitor arrays to sample and hold the input signal. A dynamic comparator [22] is used for lower kick-back noise and lower energy consumption. To minimise the area used by the capacitor arrays, the minimum unit capacitor is used for the DAC, resulting in a total area of $560 \mu\text{m} \times 60 \mu\text{m}$ for the ADC. In addition, the capacitor used for the MSB check is split into a copy of the remaining capacitors [23] to minimise power consumption and obtain a faster charge/discharge transient at the cost of a higher number of control signals.

D. Serialiser

A two-stage serialiser is added at the bottom of the ADC stage to capture the data generated by the 32 sets (16 columns each) in addition to two extra control packets. Every set provides 26-bits of data, 12-bits of which come from the ADC, another 5-bits from the I-to-V converter and the remaining bits are added to the packet to provide further information about the column including its address. The two control packets also provide feedback on the running operations. The main idea of the two-stage serialiser is to use the first stage to browse the packets quickly and then use the second stage to serialize the targeted packet with 2 bits out of the chip per cycle. The first stage is a 34-entry shift-register with 26-bit resolution which captures the 32 data packets from the 32 sets in addition to the 2 control packets. This big shift-register browses the 34 packets within the minimum number of clock cycles and delivers the targeted 26-bit packet to the second stage which is a small 26-bit shift-register. The small shift-register serialises the data out of the chip with 2 bits at a time to increase the overall transmission throughput whilst minimising lane data rate. Unlike a one-stage serialiser, the two-stage design serialises the packet number N completely out after $(1+N+13)$ cycles instead of $(N \times 13 + 13)$ cycles. The serialiser is implemented using the digital ASIC flow.

E. System controller

All the blocks mentioned earlier require a number of control signals for operation. A controller has been designed to generate these signals based on the current system configuration that is written through a serial interface. The controller supports two main operations; (1) a write and (2) a read. During a write, the appropriate row and column/s are selected, the DAC

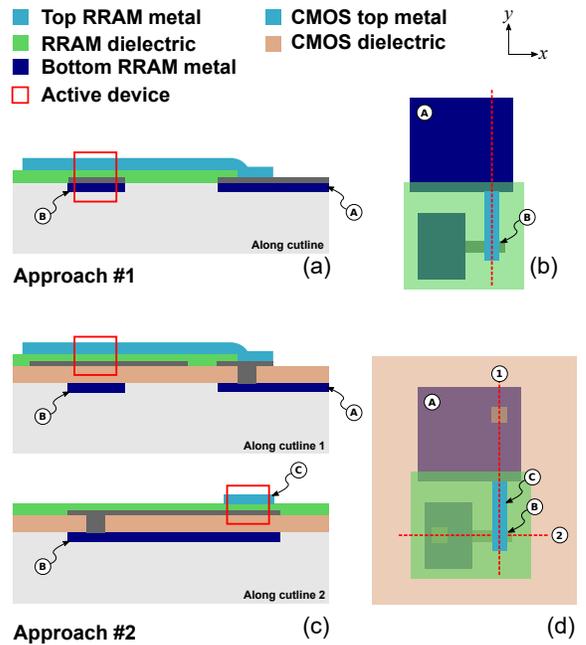


Fig. 4. CMOS-DUT integration approaches as described in Section III. In the via-less approach (a, b) RRAM is connected directly to the top-most CMOS metal whereas in the second approach (c, d) this is done through vias in the CMOS capping dielectric.

voltage set, and the cell enabled for a specific pulse width. This operation is used to program the device without measuring the resulting current. In the case of RRAM, it is expected that during a write, given appropriate values for the voltage and pulse width, the device will experience a change in resistance. On the other hand, apart from applying a voltage, a read operation also enables the I-to-V converter, ADC and serialiser to measure the current, digitise it, and transfer the data off-chip. In the case of RRAM, this operation is used to run the conventional IV sweep on the device, or to measure the current resistive state of the DUT (e.g. $V_{read} = 0.5 \text{ V}$).

III. DUT-CMOS INTEGRATION

The proposed platform is oriented towards the characterisation of two terminal DUTs. Integrating the actual devices onto it is done using regular back-end-of-line processes (BEOL) after the CMOS substrate has been formed. There are two approaches explored, depending on the way the CMOS layer interfaces the DUT. The first involves etching away the capping dielectric and fully exposing the final CMOS metal layers. This approach presents a simpler integration route as no vias are required to connect to the circuitry below the device. It also eliminates any additional parasitic capacitance that may be present between the bottom RRAM electrode and the top-most CMOS metal layer. This comes at the cost of increased routing complexity on the BEOL layers. The second approach retains the capping dielectric and uses vias to connect to the circuitry below. This simplifies routing complexity (as the CMOS and RRAM layers are fully separate) at the cost of increased processing complexity (vias and additional parasitic capacitance). Fig. 4 summarises the two approaches.

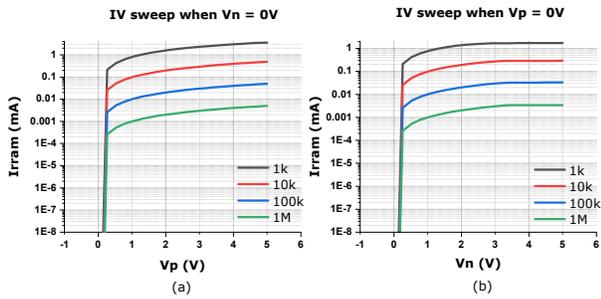


Fig. 5. IV plots of the cell at different resistance values; (a) forward mode (+ve V across DUT) and (b) reversed direction (-ve V across DUT).

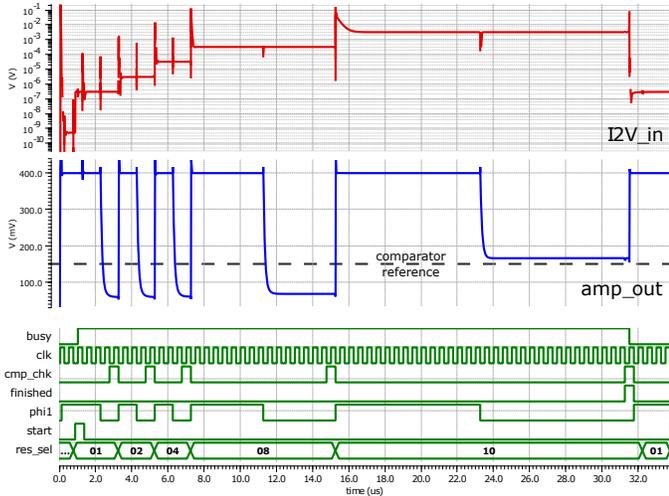


Fig. 6. Operation of I-to-V circuit for a 20 nA input current; $I2V_in$ is the input node; amp_out is the output of the amplifier; cmp_chk is the point of comparison to the voltage reference; res_sel is the resistor select (0x01 - least resistance to 0x10 - highest resistance).

The prototype devices consist of a Metal-Insulator-Metal structure (MIM) in the form of BE/AL/TE (bottom electrode, active layer and top electrode respectively). Electrodes (BE/TE) can be a selection of platinum (Pt), gold (Au) and silver (Ag) for different types of interfacial behaviour (Schottky for Pt, ohmic for Au [24] and diffusive/filamentary for Ag) with nominal thicknesses of 20/30/50 nm respectively. AL materials that have been considered are TiO_2 , AlO_x/TiO_2 [25] or ZnO [26]. All RRAM materials are deposited using RF magnetron sputtering in either an argon atmosphere (for Pt) or oxygen/argon atmosphere. Au deposition has been performed using electron beam evaporation. All layers are defined with e-beam lithography (using 200/200 nm PMMA/MMA resist) and lift-off in NMP bath. Capping dielectric is stripped using ion-beam milling either fully (in the first, via-less, approach) or partially (in the second approach).

IV. RESULTS AND DISCUSSION

The 1T1R cell was simulated for multiple resistor values, mimicking the effect of a DUT under the same condition. The resulting current range is shown in Fig. 5. The maximum current supported through is approximately 1.5 mA (with 1.5 V across a 1 k Ω DUT). On the other hand, given the range of

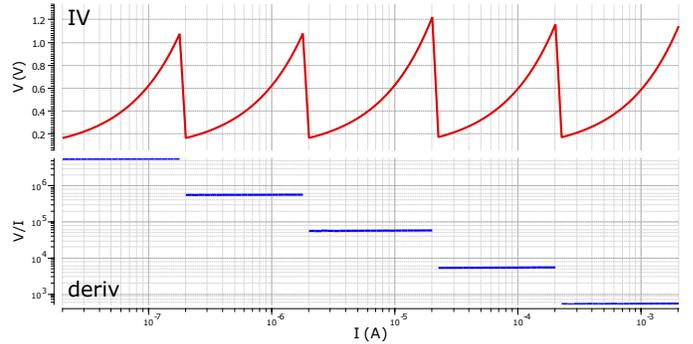


Fig. 7. IV plot of I-to-V circuit. Points shown are for the final selected resistor for that conversion; $deriv$ is the derivative showing the five different gains.

TABLE I
SYSTEM SPECIFICATIONS

Parameters	Value
Guaranteed max. V across DUT	± 1.5 V
DUT resistance range	1 k Ω - 10M Ω
# of cells, # of test cells	1M, 32k
Cell configuration, cell size	1T1R 5 V, 5 μ m x 2.28 μ m
Min. pulse width	5ns
DAC resolution, output range	8 bits, 50 mV - 3 V
Current measurement range	20 nA - 2 mA
ADC resolution, sample rate	12 bits, 250 kSPS

resistance and voltage used, the resulting current range spans 5 decades, which match the 5 stages in the I-to-V converter.

A transient simulation of this circuit is shown in Fig. 6 with an input current equal to 20 nA. With the use of a switched-capacitor amplifier, there are two phases for each resistor; a sampling (and resetting) phase and an amplifying phase. Additionally as evinced in Fig. 6, both the sampling and the amplifying phase for the highest resistance are longer when compared to that of the lowest resistance in the resistor bank. This is there to optimise the time per stage as required by the settling time analysis of the entire set circuit. A full characterisation of the circuit is illustrated in Fig. 7. This shows the nominal behaviour of the circuit over a wide range of current. Additional specifications for the chip are listed in Table I.

V. CONCLUSION

This work presents a CMOS-based, on-chip characterisation platform for emerging memory technologies with particular focus on forming-free RRAM. The chip consists of four independent sub-arrays with a full resolution of one million devices. On-chip DACs provide a programmable voltage across the device, whilst current-to-voltage and ADC circuits are used to digitise the measured current over a 20 nA to 2 mA range.

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REFERENCES

- [1] P. Jain *et al.*, “A 3.6Mb 10.1Mb/mm² Embedded Non-Volatile ReRAM Macro in 22nm FinFET Technology with Adaptive Forming/Set/Reset Schemes Yielding Down to 0.5V with Sensing Time of 5ns at 0.7V,” in *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, Feb. 2019, pp. 212–214, iSSN: 2376-8606.
- [2] R. Fackenthal *et al.*, “A 16Gb ReRAM with 200MB/s write and 1GB/s read in 27nm technology,” in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2014, pp. 338–339, iSSN: 2376-8606.
- [3] A. Kawahara *et al.*, “An 8 Mb Multi-Layered Cross-Point ReRAM Macro With 443 MB/s Write Throughput,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 178–185, Jan. 2013, conference Name: IEEE Journal of Solid-State Circuits.
- [4] T. Liu *et al.*, “A 130.7mm² 2-layer 32Gb ReRAM memory device in 24nm technology,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2013, pp. 210–211, iSSN: 2376-8606.
- [5] C.-X. Xue *et al.*, “Embedded 1-Mb ReRAM-Based Computing-in-Memory Macro With Multibit Input and Weight for CNN-Based AI Edge Processors,” *IEEE Journal of Solid-State Circuits*, vol. 55, no. 1, pp. 203–215, Jan. 2020, conference Name: IEEE Journal of Solid-State Circuits.
- [6] P. Chi *et al.*, “PRIME: A Novel Processing-in-Memory Architecture for Neural Network Computation in ReRAM-Based Main Memory,” in *2016 ACM/IEEE 43rd Annual International Symposium on Computer Architecture (ISCA)*, Jun. 2016, pp. 27–39, iSSN: 1063-6897.
- [7] Y. Y. Liauw *et al.*, “Nonvolatile 3D-FPGA with monolithically stacked RRAM-based configuration memory,” in *2012 IEEE International Solid-State Circuits Conference*, Feb. 2012, pp. 406–408, iSSN: 2376-8606.
- [8] N. C. Dao *et al.*, “Memristor-Based Pass Gate for FPGA Programmable Routing Switch,” in *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2021, pp. 1–5, iSSN: 2158-1525.
- [9] D. D. Antoniadis *et al.*, “Open-Source Memory Compiler for Automatic RRAM Generation and Verification,” in *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2021, pp. 97–100, iSSN: 1558-3899.
- [10] IRDS, “International Roadmap for Devices and Systems 2020 Edition Beyond CMOS,” Tech. Rep., 2020.
- [11] J. S. Meena *et al.*, “Overview of emerging nonvolatile memory technologies,” *Nanoscale Research Letters*, vol. 9, no. 1, p. 526, Sep. 2014. [Online]: <https://doi.org/10.1186/1556-276X-9-526>
- [12] S. Maheshwari *et al.*, “Design Flow for Hybrid CMOS/Memristor Systems—Part I: Modeling and Verification Steps,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 12, pp. 4862–4875, Dec. 2021, conference Name: IEEE Transactions on Circuits and Systems I: Regular Papers.
- [13] IRDS, “International Roadmap for Devices and Systems 2020 Edition More Moore,” Tech. Rep., 2020.
- [14] Tektronix, “Pulse I-V Characterization of Non-Volatile Memory Technologies,” Tech. Rep.
- [15] F. V. Lupo *et al.*, “Custom measurement system for memristor characterisation,” *Solid-State Electronics*, vol. 186, p. 108049, Dec. 2021. [Online]: <https://www.sciencedirect.com/science/article/pii/S0038110121000940>
- [16] J. Cayo *et al.*, “Design Steps towards a MCU-based Instrumentation System for Memristor-based Crossbar Arrays,” in *2021 10th International Conference on Modern Circuits and Systems Technologies (MOCAS)*, Jul. 2021, pp. 1–5.
- [17] P. Foster *et al.*, “An FPGA Based System for Interfacing with Crossbar Arrays,” in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Oct. 2020, pp. 1–4, iSSN: 2158-1525.
- [18] R. D. L. Fuente *et al.*, “On the Development of MCU-based ad hoc HW Interface Circuitry for Memristor Characterization,” in *2020 European Conference on Circuit Theory and Design (ECCTD)*, Sep. 2020, pp. 1–5, iSSN: 2474-9672.
- [19] T. Maeda *et al.*, “Resistance Measurement Platform for Statistical Analysis of Emerging Memory Materials,” *IEEE Transactions on Semiconductor Manufacturing*, vol. 33, no. 2, pp. 232–239, May 2020, conference Name: IEEE Transactions on Semiconductor Manufacturing.
- [20] S. Yan *et al.*, “Constant-g/sub m/ techniques for rail-to-rail CMOS amplifier input stages: a comparative study,” in *2005 IEEE International Symposium on Circuits and Systems*, 2005, pp. 2571–2574 Vol. 3.
- [21] V. Saxena *et al.*, “Indirect feedback compensation of CMOS op-amps,” in *2006 IEEE Workshop on Microelectronics and Electron Devices, 2006. WMED '06.*, 2006, pp. 2 pp.–4.
- [22] B. Razavi, “The StrongARM Latch [A Circuit for All Seasons],” *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, 2015, conference Name: IEEE Solid-State Circuits Magazine.
- [23] B. Ginsburg *et al.*, “An energy-efficient charge recycling approach for a SAR converter with capacitive DAC,” in *2005 IEEE International Symposium on Circuits and Systems*, May 2005, pp. 184–187 Vol. 1, iSSN: 2158-1525.
- [24] L. Michalas *et al.*, “Electrical characteristics of interfacial barriers at metal—TiO₂ contacts,” *Journal of Physics D: Applied Physics*, vol. 51, no. 42, p. 425101, Sep. 2018. [Online]: <http://dx.doi.org/10.1088/1361-6463/aadbd2>
- [25] S. Stathopoulos *et al.*, “Multibit memory operation of metal-oxide bi-layer memristors,” *Scientific Reports*, vol. 7, no. 1, Dec. 2017. [Online]: <http://dx.doi.org/10.1038/s41598-017-17785-1>
- [26] F. Mangasa Simanjuntak *et al.*, “Practical approach to induce analog switching behavior in memristive devices: Digital-to-analog transformation,” *Memristors [Working Title]*, Aug. 2021. [Online]: <http://dx.doi.org/10.5772/intechopen.98607>