Power Delivery for Ultra-Large-Scale Applications on Si-IF

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Abstract—In recent years, with the rise of artificial intelligence and big data, there is an even greater demand for scaling out computing and memory capacity. Silicon interconnect fabric (Si-IF), a wafer-scale integration platform, promotes a paradigm shift in packaging features and enables ultra-large-scale systems, while significantly improving communication bandwidth and latency. Such systems are expected to dissipate tens of kilowatts of power. Designing an efficient and robust power delivery methodology for these high power applications is a key challenge in the enablement of the Si-IF platform. Based on several figureof-merit parameters, an efficient power delivery methodology is matched with each of three candidate applications on the Si-IF, namely, artificial intelligence accelerators, high-performance computing, and neuromorphic computing. The proposed power delivery approaches were simulated and exhibit compatibility with the relevant ultra-large-scale application on Si-IF. The simulation results confirm that the dedicated power delivery topologies can support ultra-large-scale applications on the SI-IF.

Index Terms—Power delivery, heterogeneous integration, Si-IF, dielet, wafer-scale, AI accelerators, HPC, TPU.

I. INTRODUCTION

Over the last few decades, system-on-chip (SoC) integration has been the mainstream integration approach in the semiconductor industry for high-performance applications. Recently, Cerebras, a wafer-size compute system has been demonstrated [1],[2]. Cerebras provides a significant increase in compute and memory capacity, but requires fabrication at extremely high yield and does not support heterogeneity.

Silicon interconnect fabric (Si-IF) is a heterogeneous integration platform and a promising solution to address the challenges of SoCs [3]. The Si-IF replaces the complex conventional packaging with a single-layer integration hierarchy. In this technology, dielets (small unpackaged dies) are attached to a Si substrate that serves as the package and the printed circuit board (PCB). The passive Si substrate includes interconnects for signaling and power delivery. The Si-IF is a system-on-wafer that supports the integration of heterogeneous dielets fabricated using disparate technologies, materials, and processes [3],[4].

Power delivery and thermal management are key challenges in wafer-scale systems, especially in assemblies of high power density dielets [5]. That said, utilizing Si (relatively high thermal conductivity of 149 W/mK) as the substrate and package, reduces the thermal challenge within the Si-IF platform, as compared to other wafer-scale integration approaches.

As shown in Figure 1, two general approaches for power delivery on Si-IF are considered, (i) from connectors at the periphery of the wafer, and (ii) from the backside of the platform. In the first approach, converters and regulators are



Fig. 1. Schematics of the periphery and backside power delivery approaches on the Si-IF.

placed at the periphery of the wafer, and the current will be delivered to the dielets using the Si-IF horizontal interconnects [6]. Although cheaper and easier to implement, peripheral power delivery suffers from significant resistive losses as well as reduction of on-Si-IF area dedicated to functional dielets, and therefore only compatible with low-power applications. Alternatively, in the second approach, converters are placed on a dedicated external PCB or at the backside of the Si-IF, and the current will be delivered to the dielets using throughwafer vias (TWVs) [7],[8]. Here, high-power applications can be supported while requiring high fabrication cost and complexity.

Three principal wafer-scale applications, including artificial intelligence (AI) accelerators, neuromorphic computing, and high-performance computing (HPC), are considered in this paper. For each application, a commercial SoC-based product is chosen and modeled using optimal-size dielets for integration on the Si-IF. Four power delivery topologies (based on either peripheral or backside power delivery) are simulated, modeled, and compared with respect to several figure of merit (FOM) parameters. Specifically, resistive and inductive voltage drop, resistive and inductive power loss, area, and fabrication challenges.

The rest of the paper is composed of the following sections. The structure of the Si-IF and the proposed power delivery topologies are presented in Section II. In Section III, the selected commercial products for each application of interest are introduced. Simulation results, comparison of the proposed topologies, and related discussions are provided in Section IV. Finally, some concluding remarks are offered in Section V.

II. SI-IF AND POWER DELIVERY TOPOLOGIES

The Si-IF is a wafer-scale chiplet-based platform that supports a small inter-dielet spacing (< 100 μ m) and a small vertical (between dielet and platform) interconnect pitch (< 10 μ m).



Fig. 2. A schematic of the Si-IF platform.

These parameters allow an ultra-large heterogeneous system to be integrated with high density on a 300 mm wafer [3].

As shown in Figure 2, the structure of the Si-IF consists of copper (Cu) pins, Si wafer, TWVs, interconnects, Cu pillars, Cu pads, and dielets. Note that the Cu pins, TWVs, and PCB are optional components of the platform for backside power delivery and cooling purposes, *e.g.*, flash cooling [9]. Dielets on the Si-IF are either functional dielets (FDs) or utility dielets (UD). UDs are critical nodes in the network that enable global communication, power conversion and management, synchronization, and test of the Si-IF [10]. UDs on the Si-IF platform are similar to routers within a network on chip (NoC) architecture. Additional properties of the Si-IF are described in detail in [3]. Typical dimensions of features on the Si-IF platform are listed in Table I.

Schematics of the power delivery topologies under evaluation, including one peripheral (PT) and three backside (BT1, BT2, and BT3) topologies, are shown in Figure 3. As shown in Figure 3(a), PT includes a ring at the periphery of the wafer which is dedicated to the converters, regulators, and required passives to reduce the high input voltage (48 V) to point-of-load (POL) voltage (48/POL). The current, in this case, will be delivered to the dielets at POL voltage through on-Si-IF interconnects and Cu pillars. It is assumed that, in the PT topology, 30% of the wafer area is occupied by converters, regulators, and required passives [6]. BT1 is a lowvoltage high-current topology that includes a 48/POL converter on a dedicated external PCB (illustrated in the bottom of Figure 3(b)). BT2 is a high-voltage low-current power delivery approach that includes a 48/POL converter within each UD

 TABLE I

 TYPICAL FEATURE DIMENSIONS OF THE SI-IF PLATFORM [11],[12].

Feature	Value
Optimal dielet area	1-100 mm ²
Inter-dielet pitch	100 µm
Maximum substrate area	70,685 mm ²
Contact pad area	20 µm ²
Cu pillar diameter/height/pitch	5/5/10 µm
Cu pin diameter/height/pitch	1.5/20/3 mm
TWV diameter/height/pitch	100/500/200 µm
Si substrate diameter/thickness	300/0.5 mm
Interconnect width/thickness/pitch	2/2/4 µm
Number of interconnect layers	2–4

on the top side of the wafer. In BT2, Cu pins are not used in the structure (less heat dissipation is expected due to the low-current nature of this topology), and the wafer is directly connected to a dedicated PCB using ball grid arrays (BGAs). Given that each UD in the BT2 topology, serves as a power source for surrounding FDs, the FD-UD tile configuration must be determined. Two tile configurations for BT2 are considered, namely, BT2 8 and BT2 24. BT2 8 represents an 8-1 tile structure (shown in Figure 4(a)), where each UD delivers power to 8 surrounding FDs. Alternatively, BT2 24 represents a 24-1 tile structure (shown in Figure 4(b)), where each UD delivers power to 24 nearby FDs. The size of the tile corresponds to a tradeoff between effective area and power losses. For example, assigning more FDs to each UD, *i.e.*, larger tile, means more area is dedicated to FDs, leading to higher computing capacity on the one hand, and, on the other hand, to increased power loss and voltage noise. BT3 is a hybrid topology that includes a two-stage voltage conversion, a 48/12 converters on the dedicated external PCB and a 12/1 converters on the backside of the Si wafer.

A three-stage hierarchical decoupling capacitors (decaps) system is modeled for all power delivery topologies to allow for a fair comparison of voltage noise. In PT, decaps are placed on the topside of the wafer within the peripheral ring, in UDs, and in FDs. In BT1 and BT3, decaps are located on the external PCB, on the backside of the wafer, and on the top side of the wafer. For BT2, decaps are located on the external PCB, on the top side of the wafer, and also within the UDs. Details regarding the type and density of decaps are provided in Table II. Furthermore, as typically practiced, a fourth stage of decaps can be included on the FDs for all topologies.

III. MODELING APPLICATIONS OF INTEREST

A wafer-scale platform supports the integration of a large number of cores as well as high memory capacity. Applications with highly parallel workloads are, therefore, the best candidates for utilizing such platforms [6]. As such, AI accelerators, neuromorphic computing, and HPC have been selected as the applications of interest as well as their commercial representatives, respectively, Intel Loihi [14], AMD EPYC [15], and Google tensor processing unit (TPU) [16]. Due to the lack of available data for newer generations, the specifications of the first generation of these three commercial products have been used. Given that dielets on the Si-IF are unpackaged chips, specifications of the selected products in the unpackaged form are required. These specifications are listed in Table III. A dielet on the Si-IF should optimally be of an area in the range of 1–100 mm², based on tradeoffs among IP reusability, yield, testing complexity, handling considerations, and I/O complexity/power [3]. Based on the parameters of functional blocks within the floorplan of each commercial application, including power delivery, memory bandwidth, processing capabilities, and communication protocols, the unpackaged chip of each application is divided into several dielets to meet the area requirement of the Si-IF platform and in line with the dielet paradigm shift in system integration [17]. The specifications



Fig. 3. Schematics of power delivery topologies: (a) PT, (b) BT1, (c) BT2, and (d) BT3.

 TABLE II

 PARAMETERS OF THE CONSIDERED DECAPS FOR THE PROPOSED POWER DELIVERY TOPOLOGIES [13].

Location	Туре	Topologies	Capacitor density (nF/mm ²)	ESL (nH)	ESR (m Ω) / time constant (ns)		
PCB	electrolytic capacitor	BT1, BT2, BT3	2,600 - 4,800	3000 - 6000	10 - 20		
Backside of the wafer	ceramic capacitor	BT1, BT3	8,800 - 40,000	300 - 400	10 - 20		
On top of the wafer	DTCAP	PT, BT1, BT2, BT3	300 - 1500	Negligible	2 < RC < 20		
Inside UDs	CMOS capacitors	PT, BT2	1 – 3	Negligible	RC < 250		
In side FDs	CMOS capacitors	PT	1 – 3	Negligible	RC < 250		



Fig. 4. Two tile arrangements for BT2. (a) 8–1 tile structure, and (b) 24–1 tile structure.

of the Si-IF-compatible dielets for each product are also listed in Table III.

SuperCHIPS is a short-range simple and low-power communication protocol for the Si-IF platform [18]. Based on the communication specifications among the functional blocks of each application and the communication parameters of SuperCHIPS [12], a required power budget associated with short-range communication is added to the thermal design power (TDP) of each dielet. In other words, communication demand – similar to the area, power, and interconnect – is adjusted for each commercial product to match the new requirements of the dielet assembly.

IV. SIMULATION RESULTS AND DISCUSSION

Each commercial application was "reassembled" using Si-IF-compatible dielets and compatible electrical models were derived. The electrical model of the Si-IF structure is adopted from [7]. Decap values have been calculated based on expressions provided in [19]. For BT2, the electrical model of BGAs with 300 μ m diameter and 200 μ m height, is taken from [20]. For Intel Loihi, a low-power density system, the

converter parameters are derived from [21], whereas for the other two, high-power density, applications, from [22]. SPICE simulations were performed using MATLAB/Simulink [23].

The simulation results are shown in Figure 5, demonstrating the total voltage drop (resistive voltage drop and inductive noise) and total power loss (resistive and inductive loss). All results are normalized to the values obtained for PT.

It can be concluded from the results in Figure 5(a), that for the scaled out Intel Loihi on the Si-IF, representing the neuromorphic computing application, PT is the best power delivery topology. From Figure 5(b), it can be concluded that for the scaled out Google TPU on the Si-IF, representing the AI accelerator application, backside power delivery has an advantage as compared to PT, and BT1, exhibiting a marginal superiority as compared to BT2, is the best power delivery topology. Finally, from the results shown in Figure 5(c), for the scaled out AMD EPYC on the Si-IF, representing the HPC application, BT2_8, exhibiting a marginal superiority over BT2_24, is the best power delivery topology.

To provide a comprehensive comparison among the proposed power delivery topologies for the different applications, additional FOMs are considered. Specifically, a comparison of the applications in terms of area, computing performance, and power consumption are listed in Table IV. The computing capacity, in floating point operations per second (FLOPS), of the "reassembled" applications on Si-IF, is also provided in Table IV to allow for performance comparison. It can be seen from Table IV that topologies BT1 and BT3 exhibit the highest performance for all applications, this is due to the largest area dedicated to FDs. Alternatively, it can be seen from the simulated results that, for extremely low-power density applications such as Intel Loihi, peripheral power delivery provides the best tradeoff. This is due to the low

TABLE III
SPECIFICATIONS OF THE THREE COMMERCIAL APPLICATIONS AND THE SI-IF-COMPATIBLE DIELET FOR EACH APPLICATION.

	Intel Loihi (ne	uromorphic computing)	AMD EPYC	(HPC)	Google TPU (AI accelerator)		
	Original Chip	Si-IF dielet	Original Chip	Si-IF dielet	Original Chip	Si-IF dielet	
Platform	SoC	Si-IF	MCM	Si-IF	SoC	Si-IF	
Area (mm ²)	60	60	852	85	331	82	
Number of chip(s)	131	1	4	1	1	1	
Process technology (nm)	14	14	14	14	28	28	
TDP (W)	0.082	0.085	180	25	75	40	
Supply voltage(s) (V)	0.5 - 1.25	1	0.8 - 1.4	1	1 – 5	1.8	
Current (A)	0.065 - 0.164	0.085	128 - 225	25	15 – 75	22.22	
Frequency (GHz)	0.032	0.032	2 – 3	3	0.7	0.7	
Cores	131 ^a	131	4× 8-core Chiplet	4	1	1	
Throughput (TFLOPS)	1.26	1.26	6.14	0.61	23	6	
Memory bandwidth	3.44 Gspike/s	3.44 Gspike/s	55 GB/s	55 GB/s	34 GB/s	34 GB/s	

^{*a*} $128 \times (neuromorphic cores) + 3 \times (x86 Quark cores)$



Fig. 5. Simulated power loss and voltage drop of the three commercial applications on the Si-IF: (a) Intel Loihi (b) Google TPU (c) AMD EPYC. Note that the voltage drop values for BT1 and BT3 in (a) are about two orders of magnitude greater than the other values and therefore omitted from the plot for visibility.

 TABLE IV

 Comparison of FOMs of the three commercial applications "reassembled" on the SI-IF platform.

		Intel Loihi on Si-IF				AMD EPYC on Si-IF				Google TPU on Si-IF					
	РТ	BT1	BT2_8	BT2_24	BT3	РТ	BT1	BT2_8	BT2_24	BT3	РТ	BT1	BT2_8	BT2_24	BT3
Number of FDs	825	1,178	1,047	1,131	1,178	582	831	739	798	831	603	862	766	828	862
Total delivered power (W)	70.1	100.1	89	96.1	100.1	14,550	20,775	18,475	19,950	20,775	24,120	34,480	30,460	33,120	34,480
Computing performance (PFLOPS)	1.04	1.48	1.32	1.43	1.48	0.73	1.05	0.93	1.01	1.05	3.62	5.17	4.6	4.97	5.17

current demand by the application that significantly reduces the resistive loss on the top side of the Si-IF. Furthermore, in terms of fabrication considerations, PT topology is simplest. Whereas, fabricating Cu pins, placing decaps and converters at the backside of the wafer, and designing integrated converters within UDs add complexity to the backside power delivery topologies, significantly increasing the total cost.

The proposed power delivery topologies support a wide range of power, from tens of watts to tens of kilowatts. Furthermore, the proposed topologies support the integration of dielets with a wide variety of power densities, from 0.001 to 0.5 W/mm².

V. CONCLUSIONS

Three potential wafer-scale computing applications are modeled, simulated, and compared in terms of power and performance capacity. State-of-the-art commercial representative applications, including Intel Loihi, AMD EPYC, and Google TPU have been characterized for integration on the Si-IF. Four power delivery topologies, supporting a wide range of power densities and total power, have been proposed and compared based on several FOMs. Overall, demonstrated by simulation results, backside power delivery topologies exhibit a strong effect of inductive loss (due to the large interconnects in the backside of the Si-IF). This renders the backside power delivery topologies less effective for low-power applications, as compared to the peripheral topology. Alternatively, for highpower applications, backside power delivery topologies are best due to the highly resistive interconnect on the top side of the Si-IF. The obtained results confirm that the proposed power delivery topologies support integration of heterogeneous scalable systems on the Si-IF with extremely high computing performance.

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