An Efficient FPGA-based Accelerator for Deep Forest

Mingyu Zhu, Jiapeng Luo, Wendong Mao, Zhongfeng Wang

School of Electronic Science and Engineering

Nanjing University, Nanjing, China

Email: mingyu.zhu@smail.nju.edu.cn, luojiapeng1993@gmail.com, wdmao@smail.nju.edu.cn, zfwang@nju.edu.cn

Abstract—Deep Forest is a prominent machine learning algorithm known for its high accuracy in forecasting. Compared with deep neural networks, Deep Forest has almost no multiplication operations and has better performance on small datasets. However, due to the deep structure and large forest quantity, it suffers from large amounts of calculation and memory consumption. In this paper, an efficient hardware accelerator is proposed for deep forest models, which is also the first work to implement Deep Forest on FPGA. Firstly, a delicate node computing unit (NCU) is designed to improve inference speed. Secondly, based on NCU, an efficient architecture and an adaptive dataflow are proposed, in order to alleviate the problem of node computing imbalance in the classification process. Moreover, an optimized storage scheme in this design also improves hardware utilization and power efficiency. The proposed design is implemented on an FPGA board, Intel Stratix V, and it is evaluated by two typical datasets, ADULT and Face Mask Detection. The experimental results show that the proposed design can achieve around $40 \times$ speedup compared to that on a 40 cores high performance x86 CPU.

Index Terms—Deep Forest, Random Forest, Decision Tree, Machine Learning, Hardware Acceleration, FPGA

I. INTRODUCTION

With the rapid development of machine learning, deep neural networks (DNN) [1] have achieved great breakthrough in artificial intelligence literature. Though DNN has dominated the machine learning research fields nowadays, it has some obvious deficiencies such as high computational complexity, slow training speed, and lack of flexibility on small datasets. In 2017, a new tree-based ensemble learning method, Deep Forest (DF), was proposed by Zhou and Feng [2]. As shown in Fig. 1, its cascade structure makes DF able to do representation learning like deep neural networks. As an alternative to conventional deep learning methods, it has the following advantages over deep neural networks. Firstly, DF has almost no multiplication operations, which means low computational complexity. Secondly, DF can perform well when there are only small datasets or low-dimension datasets in contrast to DNN which requires large datasets. Thirdly, there are less hyperparameters in DF than in DNN, which makes DF easy to train. However, as the number of forests and the depth of the model increase, the computational complexity grows

severely. Since the CPU cannot meet the real-time application requirements, it is of great necessity to accelerate the inference of the deep forest on hardware.

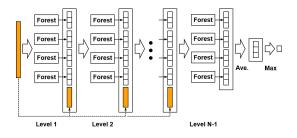


Fig. 1. Illustration of the cascade forest structure.

Many hardware accelerators have been developed for treebased models like Random Forest [3] to improve the speed. When it comes to Deep Forest, we face more problems. Firstly, since Deep Forest contains a large-scale ensemble of decision trees, it is a big challenge to store all the trees in limited space. Secondly, if we traverse all trees in parallel, the problem of node computing imbalance will arise due to the different path length of different trees and inputs.

In this paper, we propose the first hardware accelerator for DF based on FPGA, which improves processing speed with high classification accuracy and low power consumption. The main contributions of this paper are summarized as follows:

- A delicate node computing unit (NCU) is designed to decompose the inference of a single decision tree into fine-grained logic calculation, in order to accelerate the processing. Meanwhile, an optimized storage scheme is introduced to store a large number of trees with limited on-chip memory resources.
- Based on the NCU, a specialized hardware architecture, together with an efficient dataflow is proposed to alleviate the problem of node computing imbalance in the classification process, while maintaining high classification accuracy and low power consumption.
- The design is implemented on Intel Stratix V FPGA, which is also the first work for accelerating Deep Forest on hardware. The experimental results show that the proposed design can achieve around $40 \times$ speedup compared to that on a 40 cores high performance x86 CPU.

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II. BACKGROUND

A. Hardware Acceleration for Tree-based Algorithms

Several previous works have targeted hardware acceleration of the single decision tree and Random Forest. In 2012, Van Essen et al. [4] conducted a comparative study on the acceleration of inference processing of random forests by multi-core CPU, GP-GPU and FPGA. The experimental results showed that FPGAs can provide the highest performance solution while GP-GPUs still have high energy consumption that is sensitive to sample size and makes it difficult to be applied to mobile devices or edge devices. In their hardware design, the calculation cycle of each node is 5 clock cycles which can be further shortened. Sagib et al. [5] designed a pipeline structure for DT inference, and proposed an acceleration architecture composed of parallel processing nodes. Nakahara et al. [6] proposed a multi-valued decision diagrams based on random forests. In the diagram, each variable only appears once on the path in order to reduce inference latency. The disadvantage is that the number of nodes increases which will slow down the training process as a result. Alharam et al. [7] improved the real-time performance of the random forest classifier by reducing the number of nodes and branches to be evaluated, and reducing the branch length by numerical splitting.

However, different from the other tree-based models, Deep Forest is an ensemble of ensembles which makes it a big challenge to deal with the large resource consumption and the large number of calculations. In addition, the prior works mainly focus on shortening the branch length of each tree which brings small speed improvement. In this paper, we accelerate the inference of DF with the aid of the NCU and propose a special overall architecture for DF based on FPGA.

B. Deep Forest

The deep forest algorithm includes two parts: Multi-Grained Scanning and Cascade Forest.

Inspired by the layer-by-layer processing of the original features in DNN, Deep Forest adopts a cascading structure, as shown in Fig. 1. The cascade forest structure stacks multiple forests in this way to obtain enhanced features and better learning performance. In the cascade forest, the input of the first layer is the feature vector of the instance, and the output of each layer is a set of class vectors. The output vectors of the previous layer and the original feature vector are concatenated together as the input of the next layer. Here we use two random forests [3] and two completely-random tree forests [8] in each layer.

Fig. 2 illustrates the generation of the class vector. The traversed paths of the instance are highlighted in orange. For each instance, each forest averages the percentages of different classes of training data given by all trees in the same forest.

The overall procedure of Deep Forest uses the multi-grained scanning process to enhance the cascade forest. By using multiple sizes of sliding windows, the transformed feature vectors contain more information and different kinds of outputs are sent to the corresponding layer of the cascade forest. DF terminates training when the performance cannot be improved.

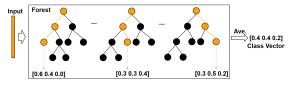


Fig. 2. Illustration of class vector generation.

III. PROPOSED DESIGN

A. Node Computing Unit

Deep Forest contains a cascade structure of ensemble trees, which makes it have higher computational complexity than other tree-based models, so it is important to reduce memory requirements and improve inference speed. Firstly, the storage scheme optimizes the format used to store the trees, while including all the information of each node in a 32-bit word. Secondly, we propose a computation-efficient node computing unit (NCU) and it can shorten the node operation period to 4 clock cycles while [4] uses 5 clock cycles.

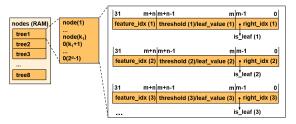


Fig. 3. Storage of trees and memory layout of each node.

In traditional storage scheme of tree-based models, the information of a single tree includes address of feature, threshold and addresses of the left and right child nodes. Our goal is to store each node of a tree in a 32-bit word. However, if the address of feature occupies 8 bits and the threshold occupies 16 bits, the left 8 bits memory is not enough for the addresses of all child nodes of an 8-depth tree. To tackle the problem, we propose an optimized storage scheme. Fig. 3 shows the storage of trees and the memory layout of each node. In our design, one nodes RAM stores the information of 8 trees of maximum depth d, and each tree has at most 2^{d} -1 nodes. The format of each node includes three fields. For non-leaf nodes, the first field stores the *feature_idx* deciding which feature will be used. The second field stores the *threshold* (*n* bits) which will be compared with the selected feature. For the addresses of child nodes, we use the pre-order traversal method to store the nodes, which means the memory position of a left child node always follows its parent node. In this way, we can deduce the address of a left child node from its parent node address. Therefore, the third field only stores the address of the right child (*m* bits) with a sign bit. When it comes to the leaf nodes, the sign bit of the *right idx* turns to 1, which distinguishes two kinds of nodes. For the leaf nodes, the second field stores the *leaf_value* (*n* bits) which is the output of the tree. In our design, *m* is 9, and without the address of the left child node, 20% storage space of trees are saved.

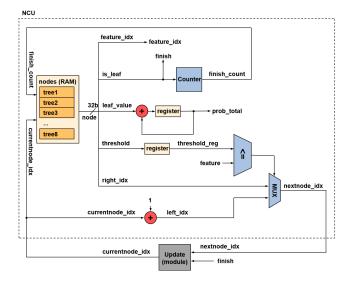


Fig. 4. The NCU and the node updating module. The NCU includes the nodes RAM memory storing the information of all trees in a group and the logic carrying out the comparison and accumulating the output of the trees.

In our design, all trees in a forest are divided into several groups and one NCU takes charge of a group of trees stored in one RAM. The description of the NCU and the node updating module is shown in Fig. 4. The design includes the nodes RAM memory, a main input, currentnode_idx, which is used to store the address of current node, a main output, nextnode idx, which is used to store the address of next node, and the logic that carries out the comparison and accumulates the *prob_total*, which is the output of the trees. To start, as the nodes RAM stores 8 trees, the *currentnode_idx* is concatenated with the *finish count* to get the information of the current node from the nodes RAM. Then, the *feature_idx* of the nonleaf nodes is concatenated with the *finish_count* to select one feature from all input features. After a clock cycle, we get the *feature* and it is compared with the *threshold_reg*. In our design, we use the combinational logic instead of the sequential logic to implement the comparator. Finally, the comparison result is sent to a multiplexer, deciding whether the left child or the right child will be the next node. To obtain the address of the left child, *left_idx*, we add 1 to the *currentnode_idx*. As the output, the *nextnode_idx* needs to be sent to the **update** module to get the *currentnode_idx* which will be used in the next round.

If the current node is a leaf node, the *is_leaf* value is 1 and is sent to the **counter** to get the counting result, *finish_count*. Meanwhile, the *leaf_value* is accumulated with the previous *prob_total* to get a new one. As a result, the overall calculation cycle of each node is shortened to four clock cycles which is one clock cycle less than that of [4].

B. Overall Architecture and Dataflow

For Deep Forest inference, the cascade forest occupies most of the time, so it's crucial to accelerate this part on hardware. We insert a pipeline at the end of each layer in order to accelerate the processing. The proposed overall architecture is illustrated as Fig. 5. In our design, each layer occupies different on-chip resource. There are two forests in one layer, each of which is processed by one **PE**. A forest consists of 32 trees and 8 trees are packed into a group and are processed by one and the same **NCU**. Therefore, each **PE** is composed of 8 **NCUs** and all of them are run in parallel. The final prediction is obtained by averaging the output of the last layer, and then sent to the off-chip **DRAM**.

There are three kinds of buffers to store data on the chip. **Input Buffer**, whose basic unit is RAM, stores three feature vectors produced by the multi-grained scanning, supposing we use three sizes of sliding windows. **Layer 1 \sim 4 Buffer** and **Output Buffer** store the input features of layer $1 \sim 4$ and the output vector of the whole on-chip logic.

Average is composed of adders and a shift register. The adders accumulate the classification results of all NCUs in one PE. As there are 32 trees in a forest, a shift register is used to get the mean value of all trees. When the averaging is finished, the result will be stored in a register.

Update contains a counter and a register. The counter records the period of the NCU. Once the period reaches four clock cycles, the address of the current node in a register, *currentnode_idx*, is replaced by the address of the next node, *nextnode_idx*. When the module receives the finish signal from the corresponding NCU, *currentnode_idx* turns to zero.

Controller receives the finish signals of all layers and counts the number of final results. It takes charge of data transport from off-chip DRAM to Input Buffer and from registers to Layer $1{\sim}4$ Buffer. It is worth noting that we concatenate the data fetched from Layer $1{\sim}4$ Buffer with the original feature vector fetched from the corresponding Input SRAM when Layer $1{\sim}4$ Buffer receives the signal from the controller.

Since different samples have different path lengths, it will cause the problem of node computing imbalance. To solve this problem, we propose the following dataflow. All NCUs in one PE are run in parallel, and each NCU is responsible for a group of trees instead of only one decision tree as the traditional methods. Once the NCU finishes a tree, it immediately processes the next one. The decision trees in the same group are sequentially traversed in a serial manner. In this way, we can mitigate the impact of gaps between various path lengths. Moreover, we insert a pipeline at the end of each layer to improve data throughput.

IV. EXPERIMENTS

A. Configuration

In this section, we use two DF models trained on ADULT [9] and Face Mask Detection [10] respectively. Face Mask Detection is a new image dataset distinguishing whether a person wears a mask correctly or not. For ADULT, the multigrained scanning is abandoned considering that the features have few sequential or spacial relationships. There are 4 layers in this model and each layer consists of one completelyrandom tree forest and one random forest, each containing 32 trees. For Face Mask Detection, 3 sizes of sliding windows

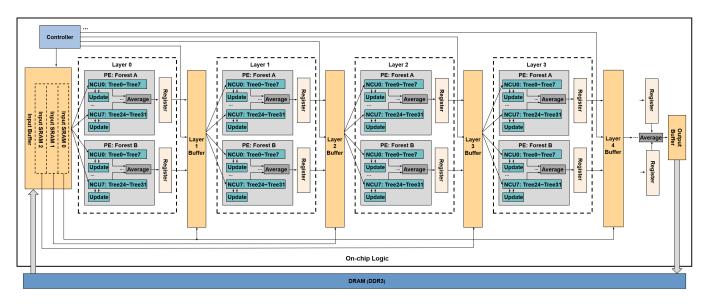


Fig. 5. The overall architecture. Each layer contains two PEs and each PE contains eight NCUs, each of which processes eight trees.

are used in the multi-grained scanning. The cascade forest is composed of 3 layers and the configuration of each layer is the same as the model trained on ADULT.

B. Results

We run the above two models on Intel Xeon Gold 6148 CPU (40 cores), and our hardware design is implemented on FPGA (Intel Stratix V), reaching a clock frequency of 400 MHz.

The proposed design decreases the usage of on-chip resourses. The resource utilization of our design on Intel Stratix V is shown in Table I. Because of the different data sizes, the models trained by the two datasets are implemented on different chips.

TABLE I THE RESOURCE UTILIZATION OF OUR DESIGN

	ADULT	Face Mask Detection
Device	Stratix V 5SGXMA3	Stratix V 5SGXEAB
ALMs	41,377 / 128,300 (32%)	213,104 / 359,200 (59%)
Memory (KB)	314 / 2,392.5 (13%)	420 / 6,600 (6%)
DSP Blocks	0	0

Table II shows the comparison of our implementation on FPGA at a clock frequency of 400 MHz with CPU. We evaluate the throughput rate on the two datasets, and find that our design achieves great speedup compared to the 40 cores high performance x86 CPU. It increases the throughput rate 40 times on ADULT and 1,871 times on Face Mask Detection. The proposed design also brings a great improvement on the latency.

Since the complexity of the deep forest algorithm is higher than the other tree-based algorithms, the energy efficiency becomes another important performance when these methods are implemented on FPGA. Table III shows the comparison of our work with [4]. In our design, the energy efficiency on

 TABLE II

 The Comparison of Our Design on FPGA (400MHz) with CPU

	Throughput Rate		Latency		
	(Ksamples/s)		$(\mu \mathbf{s})$		
	CPU	Ours	Speedup	CPU	Ours
ADULT	37.59	1,525	$40 \times$	34,000	2.52
Face Mask Detection	0.75	1,413	1,871×	877,000	2.36

 TABLE III

 THE COMPARISON OF OUR WORK WITH [4]

	Ours	[4]
Platform	Intel Stratix V	Xilinx Virtex 6
Plationii	5SGXMA3	XC6VLX
Number of FPGAs	1	2
Frequency (MHz)	400	100
Throughput Rate (Ksamples/s)	1,525	31,250
Power (W)	2.64	11
Energy Efficiency (GOPS/W)	517,117	499,968

ADULT surpasses that of [4], but the latter needs more than one FPGA to implement the same number of trees as one layer in our model.

V. CONCLUSION

In this paper we propose an efficient hardware architecture for the deep forest model which is also the first work to accelerate DF. Implemented on Intel Stratix V FPGA, the proposed design achieves at least $40 \times$ speedup compared to that on a 40 cores high performance x86 CPU. Since there are no previous works on hardware acceleration of DF, we compare it with the hardware accelerator of Random Forest and find our design has comparable energy efficient while consuming less hardware resources. There are many potential applications for the proposed design, especially some classification tasks on mobile devices.

REFERENCES

- [1] Ian Goodfellow, Yoshua Bengio, and Aaron Courville. *Deep Learning*. Deep Learning, 2016.
- [2] Z. H. Zhou and J. Feng. Deep Forest: Towards An Alternative to Deep Neural Networks. 2017.
- [3] Breiman. Random forests. Machine Learing, 2001,45(1)(-):5-32, 2001.
- [4] Brian Van Essen, Chris Macaraeg, Maya Gokhale, and Ryan Prenger. Accelerating a Random Forest Classifier: Multi-Core, GP-GPU, or FPGA? In IEEE International Symposium on Field-programmable Custom Computing Machines, 2012.
- [5] Saqib, Dutta, Plusquellic, Ortiz, Pattichis, and MS. Pipelined Decision Tree Classification Accelerator Implementation in FPGA (DT-CAIF). *IEEE Transactions On Computers*, 2015,64(1)(-):280–285, 2015.
- [6] H. Nakahara, A. Jinguji, S. Sato, and T. Sasao. A Random Forest Using a Multi-valued Decision Diagram on an FPGA. In 2017 IEEE 47th International Symposium on Multiple-Valued Logic (ISMVL), 2017.
- [7] A. K. Alharam and A. Shoufan. Optimized Random Forest Classifier for Drone Pilot Identification. In 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020.
- [8] Fei Tony Liu, Kai Ming Ting, Yang Yu, and Zhi Hua Zhou. Spectrum of Variable-Random Trees. *Journal of Artificial Intelligence Research*, 32(1):355–384, 2008.
- [9] K. Bache and M. Lichman. UCI Machine Learning Repository. 2013.
- [10] Péter Baranyi. TP Toolbox. https://www.kaggle.com/ashishjangra27/ face-mask-12k-images-dataset.