Improving Spiking Neural Network Accuracy Using Time-based Neurons

Hanseok Kim*† and Woo-Seok Choi*
*Department of ECE, ISRC, Seoul National University, Seoul, South Korea
†Samsung Electronics, Hawseong, South Korea
Email:{anjeo, wooseokchoi}@snu.ac.kr

Abstract—Due to the fundamental limit to reducing power consumption of running deep learning models on von-Neumann architecture, research on neuromorphic computing systems based on low-power spiking neural networks using analog neurons is in the spotlight. In order to integrate a large number of neurons, neurons need to be designed to occupy a small area, but as technology scales down, analog neurons are difficult to scale, and they suffer from reduced voltage headroom/dynamic range and circuit nonlinearities. In light of this, this paper first models the nonlinear behavior of existing current-mirror-based voltagedomain neurons designed in a 28 nm process, and show SNN inference accuracy can be degraded by the effect of neuron's nonlinearity. Then, to mitigate this problem, we propose a novel neuron, which processes incoming spikes in the time domain and greatly improves the linearity, thereby improving the inference accuracy compared to the existing voltage-domain neuron. Tested on the MNIST dataset, the inference error rate of the proposed neuron differs by less than 0.1% from that of the ideal neuron.

Index Terms—Artificial neural network, spiking neural network, time-based signal processing, integrate-and-fire neuron, ANN-to-SNN conversion

I. INTRODUCTION

Deep neural networks (DNNs), or artificial neural networks (ANNs), have evolved into a state-of-the-art approach for machine learning tasks, and increasing number of services, e.g. classification, searching, translation, and recommendation. Exploiting ANNs in a growing number of applications demands techniques for efficient implementation of ANN algorithms. However, realizing ANN algorithms on existing computing systems poses formidable challenges. Specifically, in conventional von-Neumann architectures, memory access dominates the latency and energy cost for realizing ANN algorithms [1].

As an alternative to the von-Neumann architecture, neuromorphic systems based on spiking neural networks (SNNs) imitating the human brain are attracting attention for lowpower deep learning hardware. In particular, architectures that employ non-volatile memory crossbars and SNNs have gained interests due to the fact that 1) no memory access is required, and 2) implementing matrix-vector multiplication, which is a ubiquitous operator in machine learning applications, is simple. Each neuron of the SNN can output a spike, and the frequency of occurrence of this spike can be considered the

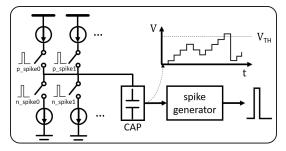
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real-valued neuron output of the ANN. This provides the SNN-based system with another feature, an event-driven system: it operates only when an event occurs, i.e. system stays in an idle state when no event occurs, which leads to power reduction in many practical scenarios.

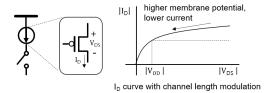
Unfortunately, however, in spite of these favorable aspects in hardware, SNNs have not been widely used as ANNs because SNNs are difficult to train, and the performance of SNNs has been worse than that of ANNs. Since SNNs exploit binary activation functions to generate spikes and the derivative of the binary activation is zero almost everywhere, conventional gradient-based learning cannot be applied. Various workaround methods such as [2]–[6] have been proposed to train high-performance SNNs, but their performance has not been scaled as well as ANNs for deeper and larger models. Recently works such as [7], [8] showed that, instead of training SNNs from scratch, a high-performance SNN can be obtained by converting a trained ANN into an equivalent SNN using integrate-and-fire (IF) neurons.

Such integrate-and-fire neurons can be implemented using either digital circuits or analog circuits. In the case of digital neurons, the desired computation such as multiply and accumulate (MAC) can be accurately performed without any error, whereas it requires many transistors consuming power and area. Moreover, synchronous digital systems need power-hungry global clock distribution. On the other hand, when neurons are implemented using analog circuits, MAC can be implemented with relatively fewer transistors. For instance, analog SNN neurons proposed in [8], [9] (depicted in Fig. 1(a)) are voltage-domain neurons, i.e. membrane potential is mapped to voltage, where spike inputs are converted into current and accumulated in a capacitor. Although simple, conventional current-mirror-based voltage-domain neurons suffer from nonlinear behavior due to the channel length modulation of the transistor in deep submicron technologies.

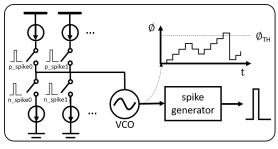
In this paper, we first investigate the nonlinearity of the voltage-domain analog neurons in a 28 nm CMOS process, and model its behavior to see how much it degrades the performance, or SNN inference accuracy. In order to mitigate the nonlinear problem, we propose a new time-based analog neuron, which is also modeled and simulated at a system level to compare its performance with the existing scheme. Simulation results demonstrate that analog neuron's nonlinear behavior can degrade the performance even for small SNNs



(a) Conventional current-mirror-based voltage-domain neuron



(b) Nonlinearity of voltage-domain neuron



(c) Proposed time-domain neuron

Fig. 1: Conceptual diagrams for conventional and proposed neurons.

and the proposed SNN using time-based neurons shows negligible accuracy difference from that using ideal neurons.

II. BACKGROUND

A. ANN-to-SNN conversion

It is known that training SNN with traditional backpropagation is difficult [10]. In spite of various studies on training SNN [6], [11], the performance has not yet reached the ANN. Instead, many studies have been conducted to convert trained ANN parameters to SNN parameters, so the SNN can have the same performance as the trained ANN [12], [13]. In [7], through effective parameter normalization, the accuracy of the converted SNN approaches that of the original ANN. Despite these achievements, it is challenging to maintain accuracy in practice since analog circuits suffer from noise, reduced voltage headroom/dynamic range, and nonlinearity. Among many potential nonideal factors, we will focus on nonlinearity and discuss how it manifests in ANN-to-SNN conversion.

B. Nonlinearity of voltage-domain neuron

The conceptual diagram of the conventional current-mirrorbased voltage-domain neuron [8], [9] is described in Fig. 1(a).

When a spike occurs, a current flows into or out of the capacitance depending on the weight polarity, and the capacitance voltage is considered a membrane potential. The output spikes of the previous layer control the switch of the current source, accumulating the spike as membrane potential, and the magnitude of the current source is determined by the weights of the SNN. When the membrane potential reaches a threshold voltage, the neuron generates a spike and the membrane potential decreases by the threshold voltage. The inherent problems of this implementation are as follows. V_{DS} must be larger than V_{OD} for the current source to be in the saturation region, and even if it is in the saturation region, the current value is changed by V_{DS} due to channel length modulation as shown in Fig.1(b). Acquiring a voltage headroom by increasing supply voltage can mitigate the problem, but this leads to higher power consumption, which undermines the benefits of SNN. Also, exploiting a cascode current source to relax channel length modulation could be a possible solution, but it decreases voltage headroom and reduces the dynamic range of membrane potential. Therefore, for voltage-domain neurons where nonlinearity inevitably occurs, it is necessary to investigate how this characteristic affects the SNN performance.

C. Impact of nonlinearity on SNN

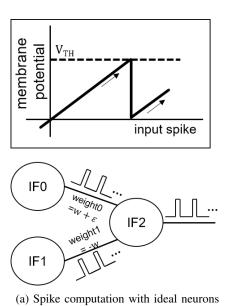
In order to understand the effect of nonlinearity on SNN, consider a simple network consisting of three IF-neurons as shown in Fig. 2. The outputs of two neurons (IF0,IF1) are applied to the next neuron (IF2), and the outputs of IF0 and IF1 generate spikes at the same rate. Additionally, let us assume that weight1 is negative (-w) and weight0 is positive $(w+\epsilon)$ as described in Fig. 2. If the IF-neuron is ideal (Fig. 2(a)), the membrane potential will increase at a constant rate because positive spikes are slightly stronger than negative spikes. It increases until the membrane potential exceeds the threshold, and an output spike will be generated. Then, the membrane potential will be subtracted by the threshold voltage, and it continues to generate spikes at a constant rate.

On the other hand, if IF-neuron is nonlinear as shown in Fig. 2(b), the membrane potential will gradually increase as in the ideal case when the potential is near zero. However, even if the magnitude of weight1 is larger than that of weight0, at a point where the positive spike and the negative spike have the same strength because of the nonlinear characteristic, the membrane potential will no longer increase. This point is expressed as "neutral point" as shown in Fig.2b. In this case, no spike is generated ever. To get rid of this nonlinearity, Section III proposes a time-based neuron that fundamentally removes the voltage-domain nonlinear behavior.

III. PROPOSED SPIKING NEURAL NETWORK

A. Time-based neuron for SNN

SNN neurons should be able to accumulate input spikes. In voltage-domain neurons, the accumulation function is implemented by flowing currents into a capacitor and converting it into a voltage. On the other hand, time-based neurons





ideal nonlinear neutral point input spike

IF0 no spike

IF1 IF2 no spike

(b) Spike computation with nonlinear neurons

take advantage of voltage-controlled oscillators (VCOs) and embed the membrane potential in the time, or phase, domain. As shown in Fig. 1(c), when spikes are received as inputs, VCO frequency is changed and accumulation of spikes can be obtained from the VCO phase. When the phase shift reaches a certain threshold, which can be detected by a phase detector, the time-based neuron generates an output spike.

B. Linearity of time-based neuron

As shown in Fig.1, current sources are used in the time-based neuron, which is not ideal either. Nevertheless, it does not cause nonlinearity in the time-based neuron because the drain voltage of the current source is not accumulated with spike inputs unlike the drain voltage in the voltage-domain neuron. In the time-based neuron, at the moment when the spike comes in, the drain voltage will rise a little, but when the spike disappears, the voltage will fall back to the original value. Therefore, the current source can flow the same amount of current regardless of the accumulated input spike. In addition, there is no limitation for membrane potential because phase is able to rotate indefinitely, whereas the range of membrane potential in the voltage-domain neuron is bounded by the supply voltage. This characteristic is also advantageous to increase the resolution of membrane potential.

IV. EXPERIMENTS

A. Circuit design and simulation

In order to model realistic linearity characteristics, both voltage-domain neuron and time-domain neuron are designed in a 28 nm process and simulated. The voltage-based neuron is simulated while applying spikes of constant ratio to the input, and the output voltage of the capacitor is measured. The time-based neuron is simulated by applying the same spikes and measuring the output phase shift. As a result, membrane

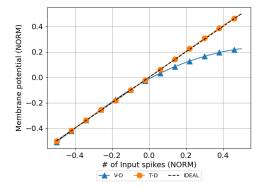


Fig. 3: Simulated membrane potential via input spikes of ideal, voltage-domain, time-domain neuron.

potential via input spikes is obtained as shown in Fig. 3. Note that ranges of membrane potential and the number of input spikes are normalized to -1 to 1. As the number of input spikes to the voltage-based neuron increase, the amount of change in the membrane potential per spike becomes smaller due to channel length modulation. On the other hand, in the case of time-based neuron, the amount of change in the membrane potential per spike keeps constant in the entire range just like the ideal case.

B. System-level simulation with nonlinearity modeling

To find out how the neuron's nonlinearity affects SNN, system-level simulation is performed to classify MNIST dataset with both voltage-domain and time-domain neuron model. For the experiments, we customized and exploited the ANN-to-SNN conversion tool, which is an open source released by [7]. The simulation setup is configured as described in 4. LeNet-5 [14] is chosen for classification, and after training the model with MNIST, the trained parameters

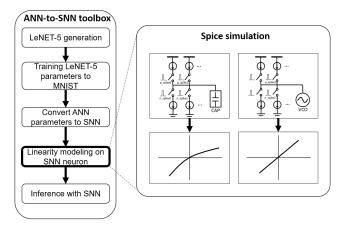


Fig. 4: SNN simulation setup with linearity modeling.

are extracted and converted into SNN layers. Then, MNIST classification with neuron models extracted from circuit simulation is carried out. Three different models—voltage-based neuron, time-based neuron, and ideal neuron—are applied to the simulation and compared as shown in Fig. 5 The x-axis represents the simulation timestep and every simulation timestep, it computes membrane potential and determines whether a spike is fired. The y-axis is the classification error rate. It takes some time for error rate to reach its stable point because spikes sequence in SNN is a stochastic process and a few samples cannot represent their final value. After the error rates have been stabilized, the time-based neuron has an error rate (4.25%) almost similar to that of ideal neuron (4.2%). On the other hand, the accuracy of the voltage-based neuron is degraded.

Since the performance degradation of the voltage-based neuron model may have occurred simply due to failing to cover the full range of the ideal model as shown in Fig. 3, several attempts to re-scale the nonlinear transfer curve of the voltage-based neuron model are conducted. Fig. 6a shows the nonlinear models re-scaled in various ways. Re-scaling with constant factors (1.2, 1.4, 1.5, 1.6, 1.8, 2) and fitting to the maximum range of the ideal curve are performed. Despite various re-scaling, all results have less performance than time-domain neuron as shown in Fig. 6b. As mentioned in Section II-C, nonlinearity can only be compensated by adjusting each coefficient individually, so it cannot achieve the performance corresponding to the ideal neuron or voltagebased neuron with any simple re-scaling. Through simulation results above, it is shown that the nonlinearity of the voltagebased neuron degrades SNN performance while the time-based neuron has high accuracy close to the ideal neuron.

V. CONCLUSION

In this paper, the nonlinear behavior of existing voltagebased neurons is characterized in a 28 nm process, and we demonstrate that these nonlinear characteristics can cause significant SNN performance degradation. In order to overcome the analog neuron design challenges posed by deep submicron

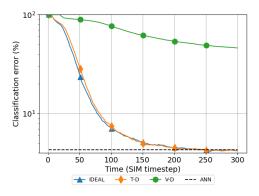
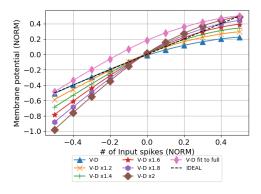
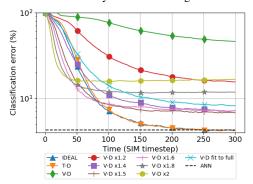


Fig. 5: LeNet5 MNIST classfication with linearity modeling



(a) Re-scaled nonlinearity model of voltage-domain neuron



(b) LeNet5 MNIST classfication with re-scaled model

Fig. 6: Re-scaled voltage-domain neuron model and MNIST classification.

technologies, a time-based neuron is proposed to guarantee linear characteristics. Tested on the MNIST dataset, the proposed neuron achieves 4.25 % classification error differing less than 0.1 % from that of the ideal neuron.

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