VSA: Reconfigurable Vectorwise Spiking Neural Network Accelerator

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Abstract—Spiking neural networks (SNNs) that enable lowpower design on edge devices have recently attracted significant research. However, the temporal characteristic of SNNs causes high latency, high bandwidth and high energy consumption for the hardware. In this work, we propose a binary weight spiking model with IF-based Batch Normalization for small time steps and low hardware cost when direct training with input encoding layer and spatio-temporal back propagation (STBP). In addition, we propose a vectorwise hardware accelerator that is reconfigurable for different models, inference time steps and even supports the encoding layer to receive multi-bit input. The required memory bandwidth is further reduced by two-layer fusion mechanism. The implementation result shows competitive accuracy on the MNIST and CIFAR-10 datasets with only 8 time steps, and achieves power efficiency of 25.9 TOPS/W.

Index Terms—Spiking neural network, deep learning accelerators

I. INTRODUCTION

Artificial neural network (ANN) becomes popular in recent years due to its excellent performance, but it contains a large amount of data transfer and complex calculations that is not suitable for resource-constrained battery-powered mobile devices. Therefore, spiking neural network (SNN), a brain-inspired computing models, is currently developed as an alternate to ANN since its binary spikes transmission is relatively simple for hardware implementation. So far, [1]-[4] have demonstrated their application specific designs enable inference or learning with extremely low power consumption, but they are limited to small neural network architectures or simple datasets. Only the large-scale neuromorphic hardware systems such as TrueNorth [5] and Loihi [6] can perform the large-scale neural network and can reconfigure. However these modern SNN architectures achieve lower throughput and higher energy per neuron, compared to ANN accelerators. [7] attribute this phenomenon to the temporal aspect in SNN that process data across many time steps. This makes the inference time extremely long and repeatedly accessing the same data from memory will consume a lot of unnecessary energy. In addition, a stateful spiking neuron needs to record membrane potential every time step that will increase off-chip memory transfer, which leads to more power consumption.

To address above issues, this paper proposes a reconfigurable vectorwise SNN hardware accelerator that needs small

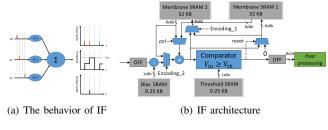


Fig. 1. IF neuron

time steps and low hardware cost and memory bandwidth through model and hardware optimizations. For the SNN model, this paper integrate the binary neural network (BNN) training method into SNN to directly train a binary weight spiking model, which minimizes the off-chip memory transfer and on-chip storage. The first layer is designed to be an encoding layer [8], which receives multi-bit positive inputs and generate spikes for the next layer. This can greatly reduces the time steps required for inference. Furthermore, the proposed integrate and fire (IF)-based Batch Normalization (BN) reduce BN overhead on hardware. For the hardware part, this design can reconfigure to support different inference time steps and models, and also supports the encoding layer to receive multibit inputs as well as spiking layer processing with spike inputs with a vectorwise input format. In addition, the memory bandwidth is further reduced by tick batching [7] and layer fusion mechanism. The result shows better performance and implementation cost compared to other approaches.

II. BINARY WEIGHT SPIKING NEURAL NETWORK

A. Spiking Networks

This work adopts spatio-temporal back propagation (STBP) [9] to directly train the network and replace Leaky Integrate-and-Fire neuron to Integrate-and-Fire neuron (IF) to reduce hardware cost. Fig. 1(a) shows the behavior of IF neurons, which includes membrane potential update (Eq. (1)) and spike firing condition (Eq. (2)).

$$V^{l}[t+1] = V^{l}[t](1-o^{l}[t]) + w^{l}o^{l-1}[t+1]$$
(1)

$$o^{l}[t+1] = f(V^{l}[t+1]), f(x) \begin{cases} 1, & x \ge V_{th} \\ 0, & \text{otherwise.} \end{cases}$$
 (2)

where $V^{l}[t]$ denotes the membrane potential at the time step t, w^{l} is the weights, $o^{l-1}[t+1]$ is the output spike

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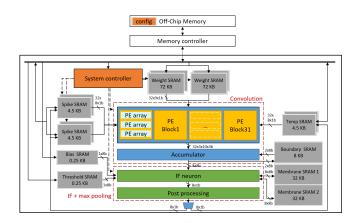


Fig. 2. System architecture

from previous layer at the time step t+1, f(.) is the firing function and V_{th} is the threshold. During model inference, neurons receive asynchronous weighted input and accumulate them into membrane potential. Whenever membrane potential reaches the threshold, neurons fire an output spike and reset membrane potential.

B. IF-based Batch Normalization

To further minimize off-chip memory transfer and onchip storage, we further combining the Binary Neural Networks [10] training method into the above method to reduce the model weights to (-1,+1). For binary neural network, batch normalization [11] is a widely mechanism to enable training of the binary weight networks. However, BN suffers from complex computation and high hardware cost. To solve this problem, we propose an IF-based BN, which is inspired by the bias-based BN [12]. The IF-based BN integrates BN into IF neuron computation by rearranging the membrane potential integration and threshold in the firing condition from the original formulation as Eq. (3) to Eq. (4).

$$\left[\gamma\left(\frac{x[1]-\mu}{\sqrt{\sigma^2}}\right)+\beta\right]+\left[\gamma\left(\frac{x[2]-\mu}{\sqrt{\sigma^2}}\right)+\beta\right]+\dots \ge V_{th} \quad (3)$$

$$\sum_{t=1}^{T} [x[t] - (\mu - \frac{\sigma}{\gamma}\beta)] \ge \frac{\sigma}{\gamma} V_{th}$$
(4)

where $\gamma, \beta, \mu, \sigma^2$ denote the BN parameters: gamma, beta, running mean, running variance and x[t] denote convolution output at time step t. As illustration in Eq. (4), the new formulation just needs to subtract the convolution output with a new bias $(\mu - \frac{\sigma}{\gamma}\beta)$ and compare with a new threshold $\frac{\sigma}{\gamma}V_{th}$ to generate the desired output spike, which reduces the extra hardware BN overhead.

III. ARCHITECTURE AND DATA FLOW

A. Overview

Fig. 2 shows the proposed system architecture. This design accesses weight and input from off-chip memory and stores them into weight and spike SRAM buffers. For the spike ping-pong buffer, one will be accessed at time-step t and the

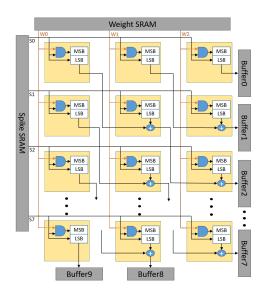


Fig. 3. PE array

other will be accessed at time-step t+1. The weight ping-pong buffer stores different layer's weight in each buffer. Each PE block processes one channel of input spike at time step t and each PE array computes one vector of them to generate the convolutional partial sum. Total 32 PE blocks can process 32 channels of input. The output of PEs will be accumulated by the accumulator to complete a convolution operation. Then, the IF neurons accumulate membrane potential and fire output spike accordingly. The result will go through the post processing if needed. The result will be saved to temp SRAM and then transferred to off-chip memory. Above process is repeatedly for all time steps of a layer input spike before moving to the next layer to prevent membrane potential from being transferred off and back on chip. With this, the weight data is also reused during the spike processing of all time steps.

B. PE Blocks

PE block consists of three PE arrays, which is constructed by 8×3 PEs as shown in Fig. 3. In the figure, eight input spikes broadcast horizontally and three weights broadcast vertically. They are multiplied using AND gate then summed up along the diagonal direction. The outputs will be stored in ten registers individually, which are partial sums of one filter column for one input channel column.

Both spike (0,1) and weight (-1,+1) are binary value, multiplying them will get a set of possible multiplication result (-1,0,1). We represent weight using only one sign bit, so weight -1 is stored as 1 and weight +1 is stored as 0. As a result, the multiplication result can be simply computed by a logic equation $o = \{s \& w, s\}$.

C. Accumulator

Fig. 4 shows the accumulator, which is divided to a threestage pipeline for shorter critical path. Three vectorwise partial sums of the same channel from three PE arrays is summed up

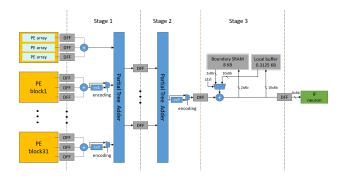


Fig. 4. Accumulator



(a) Data flow chart of a PE block



(b) Data flow Scheduling

Fig. 5. (a) Data flow chart for example in Fig. 6. For the I/O part, the same color blocks corresponds to the same SRAM. For the computation part, the same color blocks will be summed up as partial sums. (b) Data flow scheduling expressed by mathematical formulas.

first, and then the 32 output channels from 32 PE blocks is summed up with a tree adder that is divided to two partial tree adders.

If input channel number is larger than 32, they will be further divided to groups with group size 32 and then each group will be sent to PEs sequentially for processing. These partial group results are then accumulated at the last stage of the accumulator to generate the final convolution outputs. Simultaneously, we will also store the boundary information of a tile into the boundary SRAM and accumulate them with output from the neighboring tile afterward.

D. Data flow of convolution

Fig. 5(a) shows the data flow of a PE block process on example as shown in Fig. 6. This case only assume 5×3 PE arrays for clarity. In our data flow, one column vector of input is broadcasted horizontally along the PE array row and one column vector of filter weight is broadcasted vertically along the PE array column. With this data flow, the products along

										OA1	OB1	OC1
A1	B1	C1	D1	E1						OA2	OB2	OC2
A2	B2	C2	D2	E2		WA1	WB1	WC1		OA3	OB3	OC3
A3	B3	СЗ	D3	E3	x	WA2	WB2	WC2	=	OA4	OB4	OC4
A4	B4	C4	D4	E4		WA3	WB3	WC3		OA5	OB5	OC5
A5	B5	C5	D5	E5						OA6	OB6	OC6
										OA7	OB7	OC7

Fig. 6. A convolution example with 5×5 inputs, 3×3 weights, and 7×3 outputs.

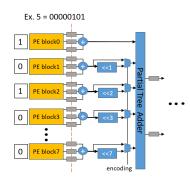


Fig. 7. The mapping example of encoding layer

the diagonal direction will be summed up and then accumulate with other PE arrays' outputs in the same cycle to generate convolutional results. The bottom boundary part of outputs (e.g. OA6, OA7) will be stored in the boundary SRAM to be accumulated with the top boundary part of outputs (e.g. OA1, OA2) of the neighboring tile afterward. In this schedule, all PEs are activated and contributed to the results, which achieves full hardware utilization. It is worth noting that each PE block only accesses one vectorwise input at a time that efficiently reuse the data.

This vectorwise scheduling can be expressed by mathematical formulas as in Fig. 5(b) that takes only three cycles to complete the example. This data flow achieve high parallelism and simple control while maintaining full hardware utilization.

E. Encoding layer

The first layer of our model is a encoding layer [8] that receives multi-bit inputs and generates spikes for the following spiking layer. To support the encoding layer with the same hardware without large overhead, we split the 8-bit inputs to eight 1-bit input bitplanes, and assign each bitplane to one PE block. Eight bitplanes will takes eight PE blocks. Thus, every eight PEs block correspond to the same weight. With this, we use the first stage accumulator that shifts the PE result and sums all these bitplane results to achieve the multi-bits convolution as shown in Fig. 7.

This mechanism is applicable when the inputs are positive, thus the inputs are normalized to (0, 1) during training.

 TABLE I

 Two network structures on two different datasets.

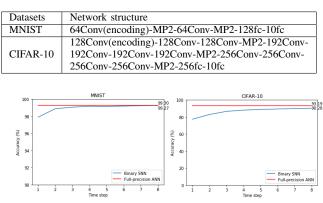


Fig. 8. Accuracy comparison between ANN and SNN

F. IF Neuron

Fig. 1(b) shows the architecture of the IF neuron that receives the convolutional results and accumulate them with the residue membrane potential stored in SRAM. The accumulated potential is compared with the threshold, which will fire a spike and reset the membrane potential in the corresponding position once reaching the threshold.

For the encoding layer, the convolutional results will be stored to the second membrane SRAM first and then accumulated with the residue potential from the fist membrane SRAM to continuously generate output of different time steps.

G. Layer fusion for lower memory bandwidth

Due to temporal input nature of SNN and limited on-chip buffer size, a naive SNN implementation will execute the model layer by layer that stores per layer output to external memory and load it back for next layer processing. This will need to save spikes of all time-steps to off-chip memory for consecutive processing and results in high data access and power consumption. To reduce this overhead, we adopt the layer fusion [13] that executes two layers successively inside the chip and then stores output to external. To support this, we increase the weight SRAM large enough to store the weights of two layers. The output spikes in temp SRAM won't be transferred to off-chip memory and will be directly sent to PE blocks to process the next layer's computation. The membrane potential will be stored in the second membrane SRAM and the output will replace the value in the spike SRAM that just been processed, then transfer to off-chip memory. Thus, the input and output transfer reduced by half.

IV. EXPERIMENTAL RESULTS

A. Network simulation result

Table. I shows two network structures for MNIST and CIFAR-10 datasets to evaluate accuracy and analyze hardware performance. Fig. 8 shows the accuracy comparison between full-precision ANN model and binary weight SNN model with different time steps. Our SNN model can achieve similar

 TABLE II

 Comparison with the results on CIFAR-10 of other approaches.

Model	Precision	Time steps	Accuracy
Sengupta et al. [14]	full-precision	2500	91.55%
Wu et al. [8]	full-precision	12	90.53%
Rathi et al. [15]	full-precison	200	92.02%
RMP-SNN [16]	full-precision	256	93.04%
Wang et al. [17]	binary	100	90.19%
Ours	binary	8	90.28%

 TABLE III

 PERFORMANCE SUMMARY AND COMPARISON WITH OTHER DESIGNS.

	This work	SpinalFlow [7]	BW-SNN [4]	
Technology	40nm	28nm	90nm	
Voltage (V)	0.9	-	0.6	
Frequency (MHz)	500	200	10	
Reconfigurable	Yes	Yes	fixed 5-CONV	
Precision (bits)	binary	8 fixed	binary	
PE number	2304	128	8208	
SRAM (KB)	230.3125	585	12.75	
Peak Throught (GOPS)	2304	51.2	64.46	
Area (KGE) (logic only)	114.98	-	225	
Area eff. (GOPS/KGE)	20.038		0.286	
Alea ell. (GOPS/KGE)	¹ 20.038	-	¹ 0.644	
Core power (mW)	88.968	162.4	0.625	
Power eff. (TOPS/W)	25.9	0.315	103.14	
rower en. (TOPS/W)	² 25.9	-	² 103.14	

¹Normalized area efficiency that is scaled to 40nm

²Normalized power efficiency that is scaled to 40nm and 0.9V

accuracy as the ANN model in short time steps. Table. II compares existing state-of-the-art results with our model on the CIFAR-10 dataset. Our model has competitive accuracy but with significant time step reduction and binary weight, which not only avoids the huge computational cost, but also reduces the off-chip access amount.

B. Hardware analysis

Table. III shows the performance summary and comparison with other SNN designs. This design is synthesized with TSMC 40nm library using the Synopsys Design Compiler, achieving peak 2304 GOPS at 500MHz and consumes 88.968 mW for CIFAR-10. The DRAM access amount is reduced from 1450.172 KB to 938.172 KB with layer fusion, a total reduction of 35.3%. Compared to the other reconfigurable design [7], they have lower throughput and power efficiency due to their element wise sparse processing. [4] is a dedicated five layers SNN ASIC, and thus achieves lower power by eliminating number of memory accesses. But that design cannot be reconfigured for other models and have very low logic area efficiency.

V. CONCLUSION

In this paper, we integrate the proposed IF-based Batch Normalization into the binary weight spiking neural network to reduce the hardware cost. Our model achieve 90.28% accuracy on CIFAR-10 using only 8 time steps. In addition, the proposed reconfigurable vectorwise accelerator can handle the different models at will, and supports the multi-bit input encoding layer and layer fusion mechanism according to the configuration. Our design can operate at 25.9 TOPS/W under peak efficiency with better power and area efficiency than the previous reconfigurable design and higher flexibility than the fixed network design.

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