

# An Adaptive Converter for Current Neural Stimulators Achieving up to 79% Power Dissipation Reduction

Mert Koç<sup>1</sup>, Salar Chamanian<sup>1,\*</sup>, Halil Andaç Yiğit<sup>1</sup>, Hasan Uluşan<sup>1,\*\*</sup>, Haluk Külah<sup>1,2</sup>

Email: {koc.mert, ayigit, kulah}@metu.edu.tr schamanian@ucsd.edu hasan.ulusan@bsse.ethz.ch

<sup>1</sup>Department of Electrical and Electronics Engineering, METU, Ankara, Turkey

<sup>2</sup>METU-MEMS Center, Ankara, Turkey

\*Currently with Department of Electrical and Computer Engineering, University of California San Diego, San Diego, CA, USA

\*\*Currently with Department of Biosystems Science and Engineering, ETH Zurich, Basel 4058, Switzerland

**Abstract**— Power consumption in neural stimulation devices such as cochlear implants, or retinal implants, is an important issue. These devices operate in volume constrained conditions and therefore have a drawback in terms of energy storage. This means that the converters used for the necessary voltage compliance in these devices must be as efficient as possible. This work describes a system implementing an adaptive converter together with a constant current stimulator. The adaptive converter utilizes a three-stage charge pump with a total of 600 pF on-chip MIM capacitors occupying 1 mm<sup>2</sup> area. Fed from a single supply, it can provide 3.3/6/9/12 V output with varying load current between 100 to 900  $\mu$ A. The converter changes its output, i.e., stimulator supply voltage depending on the digitally controlled stimulation current. This eliminates the unused voltage headroom and provides more efficient operation compared to constant voltage converters. In addition, reduced number of bulky off-chip flying capacitors make the converter appealing for volume constricted stimulators, such as fully implantable cochlear implants. An H-bridge was used to create the stimulation current, enabling single supply operation. Operational stage number and pulse frequency modulation was utilized to configure the output. In-vitro tests show a decrease of up to 79% in the power dissipation of the constant current stimulator compared to its constant 12 V operation.

**Keywords**—charge pump, DAC, efficiency, neural stimulation, pulse frequency modulation

## I. INTRODUCTION

Neural stimulation is utilized by a wide range of therapeutic devices like pacemakers, retinal implants, cochlear implants, devices utilizing neural stimulation for pain relief etc. In some of these applications, the stimulator device is placed inside the human body, which brings the issue of volume constraints with it. In other words, the capacity of the energy storage device used to power the stimulating device is limited. Moreover, in some examples these storage units may not even be rechargeable. Thus, stimulator devices must be as efficient as possible to operate for longer periods of time.

For the stimulation of the neurons, several methods can be adopted. Frequently used ones are voltage mode, charge mode and current mode. In terms of efficiency, voltage mode is the most advantageous, however, the amount of charge delivered to the neurons cannot be controlled due to varying load. With charge mode stimulation this is possible, but the need for large capacitors makes this mode unfit for volume constrained applications. Thanks to its ability to control charge injection and safety [1], current mode is advantageous for functional electrical stimulation (FES) applications. However, the aspect where current mode, or constant current stimulators (CCS) suffer, is efficiency. This is due to its high voltage compliance

requirement. Nonetheless, the moderate efficiency of the CCS can be improved by utilizing an adaptive low power step-up converter. Traditionally, a conventional step-up converter is used to create the high voltage necessary for neural stimulation. Yet, as shown in Fig. 1 (a), the potential developed across the electrodes due to the tissue-electrode interface changes with the stimulation current. If the generated high voltage adapts to the stimulation current, as shown in Fig. 1 (b), the average supply will decrease and in turn, the dissipated power will drop.

This work proposes an adaptive converter utilizing 600 pF on-chip 12 V rated MIM capacitors powering a stimulator. The output of the converter is configured according to the stimulation current to decrease the supply voltage at low and moderate current levels. The charge pump used in the adaptive converter is expected to output various voltages, thus, a modified three-stage version of the boost converter in [2] is utilized. The charge pump uses bootstrapping technique so that the number of level shifters is reduced. Additionally, the terminal voltages, including well-substrate voltage differences, of most switches do not exceed the input voltage, which enables the use of low-voltage transistors. The configurable output voltage causes a significant decrease in power consumption for moderate stimulation current levels compared to its constant 12 V operation. This translates to a longer operation period for the prosthetic device. The organization of the paper is as follows: in Section II the circuit design is described, and Section III presents the experimental results. Finally, the Section IV presents the conclusion.

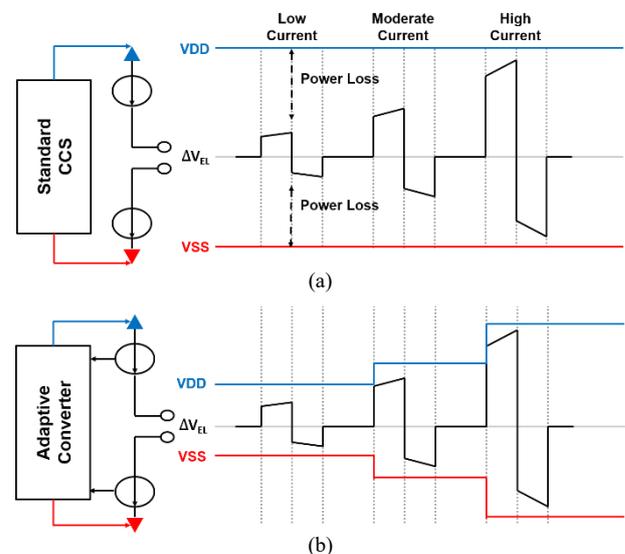


Fig. 1. Waveforms showing the fundamental idea of the converter.

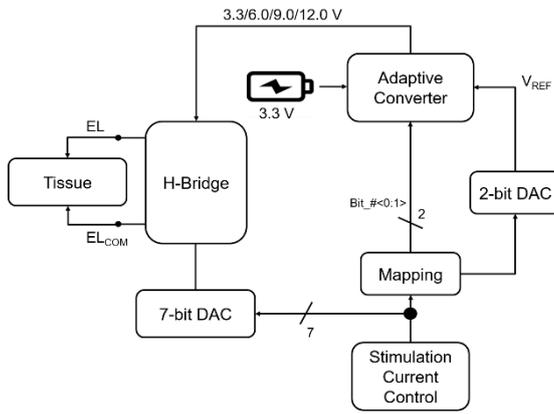


Fig. 2. Block diagram of the neural stimulation circuit.

## II. CIRCUIT DESCRIPTION

Fig. 2 shows the block diagram of the single supply CCS circuit. The biphasic current pulse is created by the H-bridge with the appropriate control signals in the source and sink cycles as shown in Fig 3 (a) and (b). The supply voltage for the H-bridge is created with an adaptive converter, which utilizes three charge pump stages and pulse frequency modulation (PFM) control to arrange its output voltage. Adjustment of the stimulation current is done with a 7-bit control signal. These 7-bits are mapped to 2-bits, which are used to determine the number of operating charge pump stages. In addition, these 7-bits are also mapped to create the necessary reference voltage ( $V_{REF}$ ) with the help of a 2-bit DAC. This  $V_{REF}$  is used for PFM control of the charge pump.

### A. H-Bridge and 7-bit DAC

For constant current simulation, biphasic current pulses are used as shown in Fig. 3 (b) to provide charge balance on the neurons. To create the biphasic pulse from a single supply, the H-bridge shown in Fig. 3 (a), which is similar to the one in [3], is controlled with the  $P_A$  and  $P_C$  control signals. It is supplied by  $V_{HIGH}$  created by the charge pump. These are also depicted in Fig. 3 (a), (b). As a result, the stimulation current shown below the control signals is obtained. In addition, an electrode shorting switch,  $P_{short}$ , is utilized that shorts the electrodes to eliminate any residual charge on the neural tissue after stimulation. To adjust the magnitude of the stimulation current, a 7-bit DAC is used.

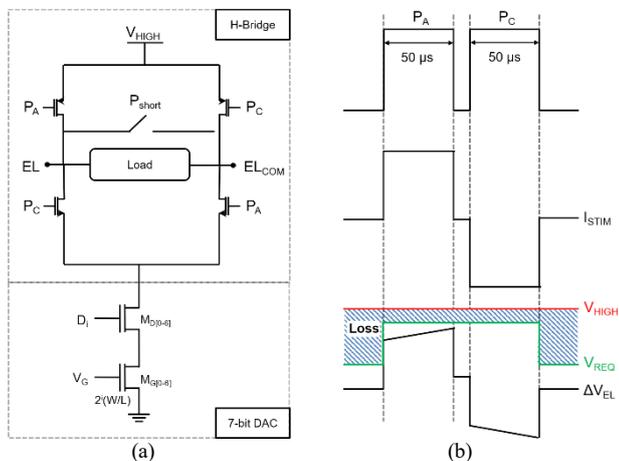


Fig. 3. (a) H-bridge and 7-bit DAC (b) control signals and resulting biphasic pulse and electrodes' potential difference.

Gate voltage  $V_G$  of transistors  $M_{G[0-6]}$  is kept constant at 3.3 V and the stimulation current is controlled digitally by the 7-bits, turning on or off  $M_{D[0-6]}$ . The resulting potential difference between the two electrodes for the applied biphasic stimulation current is presented in Fig. 3 (b). The peak point of this waveform can be calculated according to the load between EL and  $EL_{COM}$ , i.e., the stimulation electrodes, which can be modelled as a resistance and capacitance connected in series [4]. This means that the maximum voltage developed across the electrode will be different for high and low stimulation currents. In other words, the necessary voltage to perform proper stimulation will reduce at lower currents. Moreover, if the supply voltage configures itself according to the stimulation current, the dissipated power will drop.

### B. Adaptive Converter

The block diagram of the adaptive converter can be seen in Fig. 4. As mentioned, a 3-stage charge pump is used. The number of operational stages can be adjusted depending on the necessary output voltage. This is done for coarse adjustment of the output voltage and is performed by "Bit\_1" and "Bit\_2". These bits determine where the output voltage is taken from by controlling the four switches connected at the end of each charge pump stage and input voltage. Besides, they also control the drivers for the switches in the charge pump, where they are disabled when the corresponding stage is not operational. For fine tuning of the output voltage, PFM is adopted. The reason for the two-piece control can be explained as follows. Switched capacitor converters have discrete conversion ratios. The desired output voltage can be obtained for certain loads by utilizing a controlling scheme such as manipulating the switching frequency, capacitor size [5] etc. However, their efficiencies drop dramatically for output voltages that deviate too much from the discrete voltages switched capacitor circuits provide. In other words, the efficiency for a three-stage charge pump, which quadruples the supply voltage, will be much higher at 12 V output voltage compared to 9 V for a 3.3 V supply voltage. This is because by either changing the switching frequency or the capacitor size, the output impedance of the switched capacitor converter is manipulated [6]. Hence the excess power is dissipated across that impedance, similar to a linear regulator. To decrease the amount of power dissipated across this impedance, the number of operational charge pump stages is manipulated to decrease the difference between the desired output voltage and discrete voltage provided by the charge pump. For PFM control, an OTA is used to adjust the frequency of the voltage-controlled oscillator by comparing the reference voltage with the divided output voltage so that it can stay constant for different load conditions. Moreover, a non-overlapping clock generator is utilized to overcome short-circuit losses.

The heart of the adaptive converter is the charge pump proposed in [2], which is the improved version of the cross-coupled charge pump. One stage of the charge pump can be seen in Fig. 5. There are two flying capacitors per stage,  $C_i$  and  $C_i'$ . The operation principle is as follows. Node  $B_i'$  or  $B_i$  are charged to  $V_{i-1}$  in one phase and then boosted with the input voltage. In other words, when  $\phi_1$  is HIGH,  $B_i$  is equal to  $V_{i-1}$  and when  $\phi_2$  is HIGH, it is boosted with the input voltage and fed to  $V_i$ . The same operation is valid for  $B_i'$  as the charge pump operates in two opposite phases. For the clock phase diagram and further clarification, [2] can be referred to.

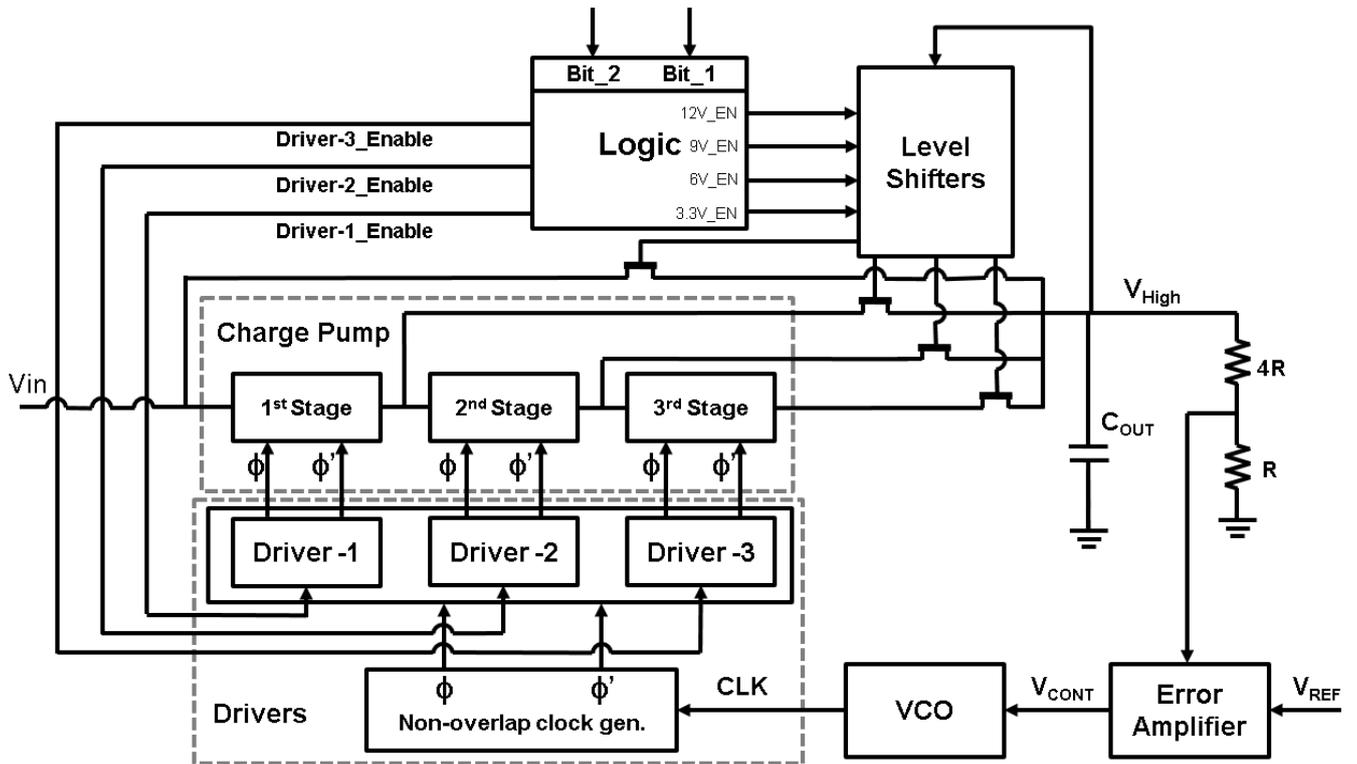


Fig. 4. Block diagram of the step-up converter.

The charge pump utilizes bootstrapping technique so that it does not require level shifters. The number of stages in this work is three as voltages up to 12 V are desired and the supply is 3.3 V. Additionally, 200 pF flying capacitor per stage is utilized, which are all on-chip  $1\text{fF}/\mu\text{m}^2$  MIM capacitors to decrease volume. The 3-stage charge pump was modified so that individual charge pump stages can be turned on and off and the output can be taken from any of the stages with additional switches as shown in Fig. 4.

### C. Operation Principle

Magnitude of the stimulation current is adjusted digitally with the 7-bit control signal. This control signal is mapped to two bits, namely Bit\_1 and Bit\_2, with a lookup table that is created beforehand according to the load. Moreover, the same lookup table and a DAC are used to generate  $V_{\text{REF}}$ . Depending on Bit\_1 and Bit\_2, the number of operational stages and thus, the output is changed. When Bit\_2 is zero and Bit\_1 is one, only one stage is operational, and the output is 6 V. When they are both one, all three stages are operating, and the output voltage is 12 V. Again, depending on these two bits the reference voltage should be adjusted.

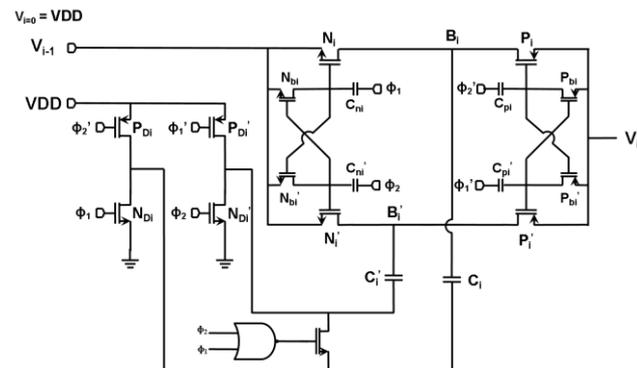


Fig. 5. One stage of the charge pump.

For example, if only one stage is operational, the output voltage will be 6 V, thus, a reference voltage of 1.2 V must be provided to the error amplifier as the output voltage is divided by 5. If all three stages are operational, the reference voltage will be 2.4 V for an output voltage of 12 V etc. This way, the step-up converter will provide the H-bridge with the right amount of supply voltage according to the stimulation current and the average power dissipation will decrease. Moreover, towards the end of the stimulation the output of the charge pump is pulled to maximum. This is to ensure that the H-bridge has enough voltage compliance in the subsequent period, should the stimulation current increase.

### III. TEST RESULTS

The proposed design was implemented in 180 nm high voltage CMOS technology (Fig. 6). Total area occupation is  $1\text{ mm}^2$ , where the 600 pF on-chip MIM capacitors occupy the most area. The converter was tested with an H-bridge and 7-bit DAC. 7-bits controlling the magnitude of the stimulation current were adjusted off-chip with an Arduino Uno. With the utilization of a lookup table for the specific load the controller mapped these seven bits to two bits for operational stage number control. It also provided the necessary signals to create a reference voltage by utilizing an off-chip 2-bit DAC.

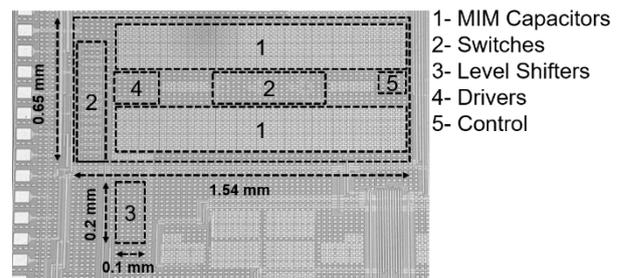


Fig. 6. Die micrograph of the adaptive converter.

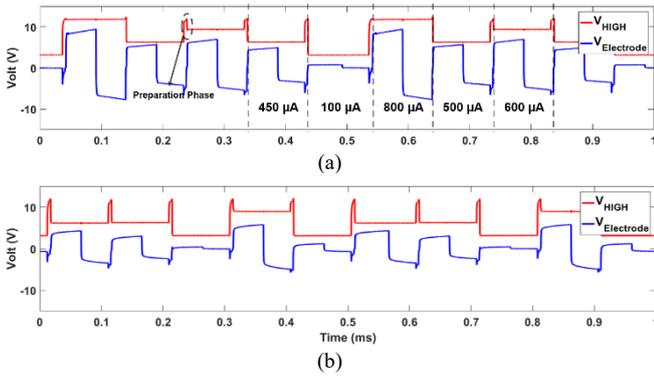


Fig. 7. Adaptive converter output and electrode voltage for (a) 9.76 kΩ and 33 nF load (b) in vitro test.

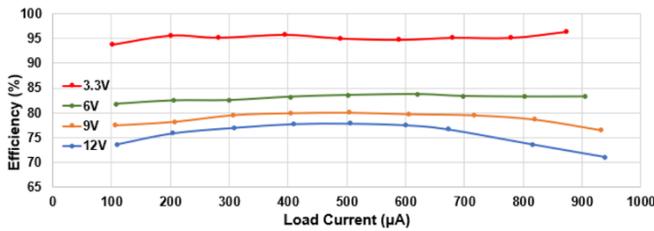


Fig. 8. Adaptive converter efficiency for specified load range.

Testing of the adaptive voltage supply was first done using an off-chip filter capacitor of 1.2 nF at the converter output with a load of 9.76 kΩ and 33 nF connected in series between the electrodes. Resulting waveforms can be seen in Fig. 7 (a) with different levels of stimulation currents. Five stimulation current values were adjusted by the 7-bit DAC and tested in a loop. In the figure, at 0.5 ms the converter is operating with 3.3 V output because the stimulation current is 100 μA, thus the voltage compliance is low. After 3.3 V, the converter configures its output to 12 V as the next period of stimulation is performed with 800 μA current. Another point that can be noticed from Fig. 7 (a) is that the converter is increasing its output to 12 V in the preparation phase before the subsequent stimulation is started. This way it is ensured that the H-bridge is provided with sufficient voltage compliance to continue proper operation if the next stimulation current increases. This can be observed around 730 μs. The adaptive converter was also tested with a single channel platinum stimulation electrode in a saline mixture and the resulting waveforms are shown in Fig. 7 (b). The electrode was measured with Agilent E4980A LCR meter and its impedance was determined to be series 7 kΩ and 65 nF in Cs-Rs configuration. The efficiency of the converter for different output and load conditions is shown in Fig. 8. Additionally, the power dissipation values of the converter for constant current stimulation for the specified load are illustrated in Fig. 9 for a range of stimulation current levels. In this figure the power values for both the adaptive voltage configuration, in which converter output changes, and constant configuration, in which output is constant at 12 V, is shown. Also provided in this waveform are the respective output voltages of the converter corresponding to the stimulation current in adaptive configuration. As can be seen, the difference is most profound at moderate current values. For 500 μA stimulation current, the power difference is 4.1 mW between the adaptive and constant converter output configuration, which corresponds to a 53% decrease. For 200 μA, on the other hand, the difference is 2.4 mW, which

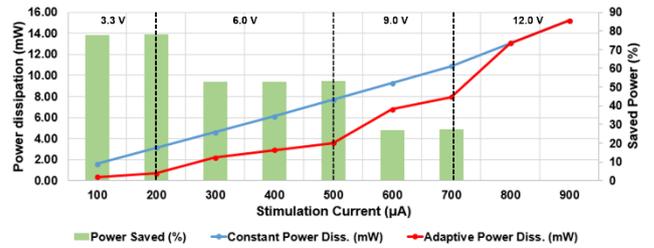


Fig. 9. Power dissipation for constant and adaptive converter and saved power in percentage for a load of 9.76 kΩ and 33 nF.

corresponds to a 79% decrease in power dissipation. This is because at such low current levels, the H-bridge and 7-bit DAC are driven with the input supply and the adaptive converter is not operating. For higher stimulation currents the charge pump is operating in the constant 12 V configuration and the power dissipation is the same as the constant output configuration.

#### IV. CONCLUSION

Constant current stimulators' safety and control on charge injection make them appealing. To reduce their issue of efficiency an adaptive converter is presented. The converter utilizes on-chip MIM flying capacitors to decrease total volume. Frequency and operational charge pump stage number are controlled to configure the converter's output. By supplying the H-bridge with the right amount of voltage compliance, the power dissipation of the stimulator is reduced. Compared to constant 12 V operation, a reduction of up to 4.1 mW in power dissipation is observed, which is a 53% decrease. This ratio reaches 79% for 200 μA stimulation current, as the stimulator is directly supplied from 3.3 V input supply.

#### ACKNOWLEDGMENT

This work has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (grant no:682756).

#### REFERENCES

- [1] H. Lee, H. Park and M. Ghovanloo, "A power-efficient wireless system with adaptive supply control for deep brain stimulation," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2203-2216, 2013.
- [2] Y. Allasameh and S. Gregori, "High-performance switched-capacitor boost-buck integrated power converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3970-3983, 2018.
- [3] H. Ulasan, A. Muhtaroglu and H. Kulah, "A sub-500 μW interface electronics for bionic ears," *IEEE Access*, vol. 7, pp. 132140-132152, 2019.
- [4] B. Swanson, P. Seligman, and P. Carter, "Impedance measurement of the Nucleus 22-electrode array in patients," *Ann. Otol. Rhinol. Laryngol.*, vol. 104, no. 166, pp. 141-144, 1995.
- [5] Y. Ramadass, A. Fayed and A. Chandrakasan, "A fully-integrated switched-capacitor step-down DC-DC converter with digital capacitance modulation in 45 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2557-2565, 2010.
- [6] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841-851, 2008.