Experimental Evaluation of Grid Support Enabled PV Inverter Response to Abnormal Grid Conditions

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Experimental Evaluation of Grid Support Enabled PV Inverter Response to Abnormal Grid Conditions

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***Abstract*—As revised interconnection standards for grid-tied photovoltaic (PV) inverters address new advanced grid support functions (GSFs), there is increasing interest in inverter performance in the case of abnormal grid conditions. The growth of GSF-enabled inverters has outpaced the industry standards that define their operation, although recently published updates to UL1741 Supplement SA define test conditions for GSFs such as volt-var control, frequency-watt control, and voltage/frequency ride-through, among others. This paper describes the results of a comparative experimental evaluation on four commercially available, three-phase PV inverters in the 24.0-39.8 kVA power range on their GSF capability and its effect on abnormal grid condition response. The evaluation examined the impact particular GSF implementations have on run-on times during islanding conditions, peak voltages in load rejection overvoltage scenarios, and peak currents during single-phase and three-phase fault events for individual inverters. Testing results indicated a wide variance in the performance of GSF enabled inverters to various test cases.**

***Index Terms*—anti-islanding, fault current, frequency-watt control, load rejection overvoltage, ride-through, volt-var control**

I. Introduction

In an effort to positively enhance the impact of increasing amounts of distributed energy resources, grid-tied photovoltaic (PV) inverters are increasingly being designed to provide advanced grid support functions (GSF) that can provide voltage and frequency support at their local point of interconnection. Among others, these GSFs include voltage ride-through (VRT), frequency ride-through (FRT), fixed power factor (FPF), volt-var control (VVC), and frequency-watt control (FWC). The increased implementation of these functions has been complemented by the release of utility specific interconnection standards such as California Public Utilities Commission Rule 21 and Hawaii Rule 14H [1,2], as well as updates to UL1741 Supplement SA and ongoing revisions to IEEE1547-2003 [3,4].

Utilities are increasingly interested in inverter GSF capabilities addressed by new standards. This paper describes the results of laboratory testing of advanced PV inverters undertaken by the National Renewable Energy Laboratory (NREL) on behalf of the Florida Power and Light Company (FPL). FPL recently commissioned a 1.1 MW-AC PV installation on a carport near the Daytona International Speedway in Daytona Beach, Florida. In addition to providing a source of clean energy production, the site serves as a live test bed for a variety of different solar inverters—36 installed inverters from eight manufacturers.

Four test inverters were selected by FPL, herein referred to as Inverter 1-4. Each three-phase inverter model was rated between 24.0-39.8 kVA, and with different GSF capabilities. A series of GSF characterization tests were run, including VRT, FRT, FPF, VVC, and FWC. While high penetrations of GSF-capable PV inverters have the potential to provide significant voltage and frequency support on distribution feeders, grid operators face significant challenges in considering their impact on protection equipment and voltage support devices, among other considerations [5]. Other considerations are inverter response to abnormal grid conditions, such as (unintentional) islanding, transient over-voltage, and fault conditions, with GSFs enabled.

Since many GSFs have the objective of supporting the grid during voltage and frequency excursions, there is concern that such functions could adversely impact islanding detection. Modeling studies such as those in [6] suggest that certain anti-islanding detection methods coupled with GSFs can have adverse impacts on islanding run-on times (ROT) when multiple inverters are present on a distribution feeder. The work in [7] examines the effect of GSFs on anti-islanding ROTs, but tests single-phase inverters sized ≤6 kW. The study in [8] evaluates the effect of VVC, VRT, FRT, and fixed power factor operation on ROTs for a 12 kW inverter, leading to inconclusive results about GSF impacts on islanding detection.

LRO occurs when a portion of a distribution feeder disconnects from the grid, resulting in a high PV generation-to-load ratio. During the typically brief period before inverter controls detect the island condition, current injected by the inverter into the load can cause transient overvoltages. This phenomenon was previously studied by NREL for small residential inverters and a 12 kW commercial inverter without GSF capability [9]. The study in [10] presents improvements in LRO peak voltages due to improvements in inverter firmware for three-phase inverters, but does not focus on variations in performance due to GSFs.

Efforts have been made to improve modeling of inverter controllers under fault conditions, but the analyses are often limited to the simulation domain [11]-[13], although the study in [14] does match prototype hardware testing to inverter fault models. UL1741 requires fault current ratings for grid-tied inverters, but such listing information is not as comprehensive as the data in this study, nor does it address three-phase faults. This paper summarizes the results of hardware testing of these abnormal conditions with GSFs enabled for 24.0-39.8 kVA three-phase inverters, providing a comparative performance analysis between the four test inverters.

II. Test Configuration

Four different PV inverters that are installed at the FPL solar site were selected for this study. All inverters were individually connected to a 45 kVA AC voltage source with three independently controllable phases, which served as the grid simulator for all tests. Each inverter was sourced by a pair of 1000V/30A PV simulators from the AMETEK TerraSAS family, with each connected to one of the independent MPPT trackers on each inverter. A solar current vs. voltage ("I/V") profile was selected such that the inverter would run at full power and be near the maximum power point of the I/V curve, at a DC voltage on the higher end of its stated power point tracking range. For tests below full power, the irradiance value of the curve was adjusted to attain the target AC output power.

The basic one-line circuit for all tests is shown in Figure 1, with the different functions of switches S1 and S2 described in the sections that follow. Switch S1 was realized with a shunt trip circuit breaker, and was opened for anti-islanding and LRO tests. Switch S2 was a controllable contactor with very low impedance path to ground for fault tests. Individual phases or all three phases could be connected to switch S2 prior to initiating faults. The load bank was a 100 kVA RLC load bank with independent loading on each of the phases, 100 W step sizes for resistive elements, and 75 VA step sizes for reactive elements.

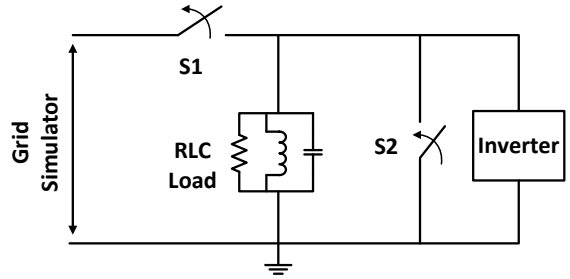

Figure 1. Basic one-line circuit diagram for anti-islanding, LRO, and fault tests

All inverters were 60 Hz, 277/480 VAC, three-phase models, listed for use in North America. A summary of basic inverter specifications along with their GSF capabilities are shown in Table I. Prior to completing the abnormal tests, a number of characterization tests for the VRT, FRT, FPF, VVC, and FWC functions were completed. These tests closely followed the procedures described in the updated revision of UL1741, and results were provided to FPL for comparative evaluation purposes.

For anti-islanding, LRO, and fault tests, different combinations of these GSFs were enabled in order to evaluate the effect of each function on the response to each abnormal grid condition. The VRT and FRT settings used in this study followed the guidelines given in Rule 21. Since a number of the trip times and magnitudes and times are adjustable under this standard, the example Rule 21 settings in UL1741 Table SA9.1 and SA10.1 for VRT and FRT, respectively, were programmed.

Inverter 1 was not capable of being programmed for the maximum low VRT trip times, so a modified trip time was used that well exceeded the IEEE1547 limits; this was likewise true for the high FRT trip time. Additionally, only two low voltage trip magnitudes could be simultaneously programmed on this inverter rather than three, so all abnormal tests were run with the two lowest magnitudes programmed. Inverter 2 was much more limited in its ride through capabilities for both VRT and FRT. The widest possible ride-through limits and longest trip times were programmed for this inverter, which were in excess of the IEEE1547 limits but well within the Rule 21 limits. Details of ride-through settings and performance for each inverter were provided to FPL in a detailed technical report.

Table I. Basic specifications of test inverters

Inverter	Nominal Real Power (kW)	Nominal Reactive Power (kVA)	GSF Capability
1	24.0	24.0	VRT†, FRT†, FWC, VVC
2	36.0	39.8	VRT†, FRT†
3	36.0	36.0	VRT, FRT, FWC, VVC
4	30.0	33.0	VRT, FRT, VVC

†Settings modified from Rule 21 defaults due to ride-through capability limitations.

A series of three FWC and VVC characteristic curves were defined in conjunction with FPL for the characterization tests, referred to as "mild", "moderate", and "aggressive" based on their slopes, as shown in Figure 2. Each FWC curve was characterized by its start frequency and stop frequency, with a linear power curtailment region connecting the two. Similarly, VVC curves were characterized by a dead band around nominal voltage (except "aggressive"), a linear region for increasing/decreasing reactive power, and maximum reactive power limits. The peak reactive power for these curves was dependent on inverter capability, and was scaled accordingly to each test inverter. The VVC curves were all symmetrical as a function of voltage, whereas FWC curves only addressed over-frequency events. The most aggressive curve for both VWC and FWC was programmed for subsequent abnormal tests.

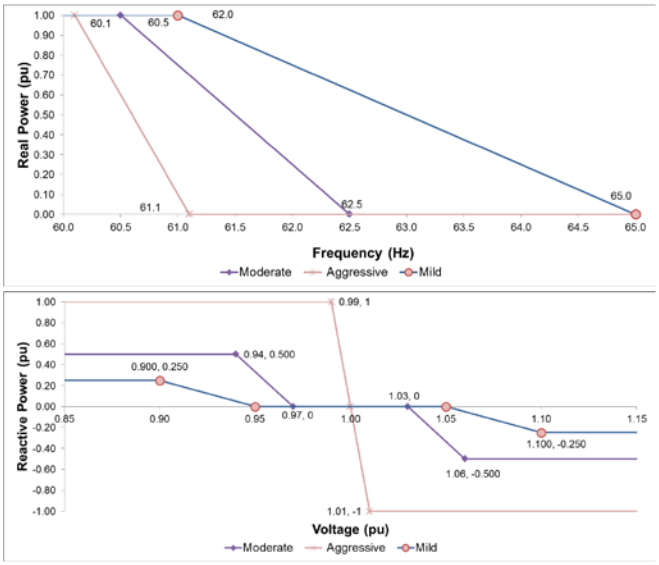

Figure 2. Characteristic curves tested for FWC (top) and VVC (bottom)

III. Anti-Islanding Tests

All anti-islanding tests were run under the test procedures in IEEE1547.1, which describes the use of a resonant RLC load to create a difficult loading scenario for islanding detection. All tests were run at 100% inverter power and the RLC load was tuned for unity quality factor, such that the fundamental component of grid current was <2% of nominal. After the circuit was operating in steady state, switch S1 was opened and the inverter ROT was measured via the current waveform. Each test was run a total of five times, with 1% changes in the inductive load for each successive test.

Three different sets of GSFs were programmed on the test inverters for each set of tests, where available. The widest FRT and VRT settings were programmed for all tests, and were the only GSFs enabled for the first set of tests. For the second set of tests, inverters capable of VVC functionality were programmed with the "aggressive" curve along with the FRT/VRT settings. Note that in some cases, some reactive power was output from the test inverter at nominal voltage due to the aggressive characteristic curve, so the reactive load was adjusted accordingly to minimize grid current. Finally, inverters capable of FWC were programmed with the "aggressive" FWC curve along with the FRT/VRT settings (VVC disabled). Each set of GSF settings was repeated at five different loading cases, creating a maximum of 15 tests per inverter.

All ROTs are summarized in Figure 3 for each test case. VVC was not programmable for Inverter 2 and FWC was not programmable for Inverter 2 or Inverter 4, so these tests cases were not run. Inverter 2 had increased ROTs at both the maximum and minimum inductive loads, so several additional tests were run, creating a total of 11 test cases. A summary of the mean and maximum ROTs for each set of test cases is summarized in Table II.

As seen from the summary data, there were mixed results depending on the test inverter and the GSFs enabled. Overall, Inverter 1 had the shortest and most repeatable ROTs, including the shortest overall ROT of all test cases. Inverter 3 tended to have the longest ROTs for each of the different GSF settings. Note that longer ROT does not necessarily imply worse behavior between inverters; IEEE1547 requires that inverters cease to energize within two seconds of island formation, and the time under which such detection occurs is dependent on the manufacturer's choice of detection strategy, and may be purposely programmed to sustain longer ROTs.

Figure 3. Anti-islanding testing summary showing ROTs for every test case

The more important metric to consider is the effect of GSF combination on ROT for each inverter. For Inverter 1, the mean and maximum ROT decreased with VVC enabled, and decreased further with FWC enabled. Regardless, the ROTs were all much faster than the required trip time and differences were on the order of several AC cycles. Similarly, the mean and maximum ROTs for Inverter 4 decreased slightly with VVC enabled, but the differences were also within several AC cycles.

TABLE II. MEAN AND MAXIMUM RUN-ON TIMES

GSFs Enabled	Metric	Inverter Number and ROT (ms)			
		1	2	3	4
VRT/FRT	Mean	142	275†	624	264
	Max	154	731†	772	305
VRT/FRT/ VVC	Mean	135	N/A	831	210
	Max	140	N/A	1076	240
VRT/FRT/ FWC	Mean	69	N/A	1593	N/A
	Max	72	N/A	1671	N/A

† Statistics based on 11 tests rather than 5.

Inverter 3 demonstrated increased mean and maximum ROTs with VVC, and higher yet ROTs with FWC enabled. However, even the peak ROT for all test cases (1671 ms) was safely with the two-second trip requirement, as seen in Figure 4. Although Inverter 3 consistently had the longest ROTs with FWC enabled, it significantly reduced output power around 400-500 ms after the island event was triggered, before disconnecting ~1.0-1.5 seconds later. This behavior was consistent for all tests with FWC enabled, suggesting that the inverter still detected an island within several hundred milliseconds, but was programmed to disconnect from the grid much later when operating with FWC mode enabled.

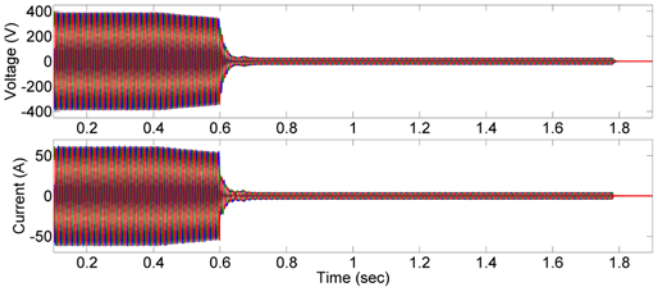

Figure 4. Longest islanding ROT for Inverter 3

IV. Load Rejection Overvoltage Tests

A series of LRO tests were run for each inverter at various inverter output power to load power (P_I/P_L) ratios, following the same procedures are those described in [9]. Inverter power was set to 33%, 67%, and 100% of nameplate; load power consumption was set to 10%, 33%, 50%, 67%, and 100% of nameplate inverter power. Every combination of these set points where inverter output power was greater than or equal to load power was tested, creating 11 unique test cases. The first 11 tests were run with FRT and VRT settings enabled. For inverters capable of VVC, a subsequent set of four tests was run at the four highest P_I/P_L ratios with the aggressive VVC curve enabled. The basic test circuit is sown in Figure 1, except only purely resistive loads were used. Once the inverter was running at the target power level, switch S1 was opened, forcing all inverter output current into the resistive load. The peak voltage was measured using a sampling rate of 100 kHz at the oscilloscope with no filtering enabled.

Figure 5 shows the peak overvoltage magnitude (proportional to peak nominal L-N voltage) for every test case as a function of P_I/P_L ratio. For higher P_I/P_L ratios, higher overvoltage magnitudes are expected (assuming an ideal current source model for the inverters). As shown in Figure 5, there were mixed results depending on the test inverter and P_I/P_L ratio, and there is no clear correlation between P_I/P_L ratio and the peak overvoltage magnitude, except perhaps for lower P_I/P_L ratios. In general, Inverter 3 had among the lowest overvoltage peaks. Almost no overvoltage was measured for Inverters 1 or 3 for unity P_I/P_L ratios. Inverter 4 had several of the largest overvoltages for any of the tests, but the maximum for any test case was 152% of nominal, which is well below some overvoltages measured in [9]. Finally, there was no clear evidence that enabling VVC caused any increase in peak voltage, and in several cases the peaks were lower than cases without VVC enabled.

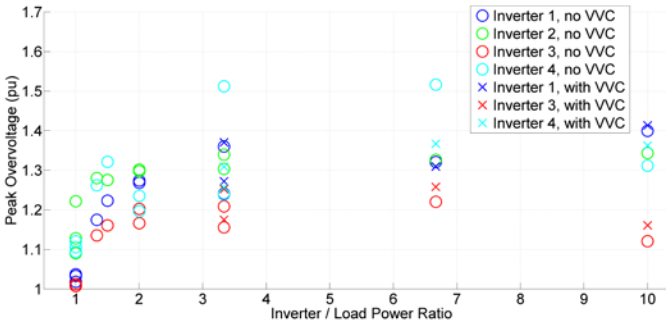

Figure 5. Load rejection overvoltage testing summary data showing peak voltages as a function of inverter to load power ratio

A waveform plot for the worst-case peak voltage for two of the inverters is shown in Figure 6. Note that for these figures, the grid simulator was disconnected just after 1 ms, and the time scale is not aligned between the two plots. A maximum peak of 141% of nominal occurred on Inverter 1 at 100% output power, 10% load power, and VVC enabled, which are considered the worst case test conditions. In most tests for Inverters 1-3, the peak overvoltages were a single pulse (sometimes on several phases), lasting a very brief period of time on the order of tens of microseconds. Inverter 4 had several longer overvoltage durations, such as the bottom plot, which shows a maximum peak voltage of 152% of nominal, which occurred at 67% inverter power, 10% load power, and VVC disabled, and continued for several AC cycles before the inverter tripped.

V. Fault Tests

The third abnormal condition of interest was the effect of GSFs on fault current contribution. Each inverter was run at full power, and several single-phase to ground and three-phase to ground fault tests were executed. Each of the four fault types was tested at unity power factor and at both ±0.80 power factor. Each test was repeated three times to randomize the phase angle on the AC cycle at which the fault occurred, leading to a total of 36 tests per inverter. Fixed power factor operation was tested because it was programmable for every inverter, and it also served as a proxy for inverter behavior when operating in VVC mode away from nominal voltage.

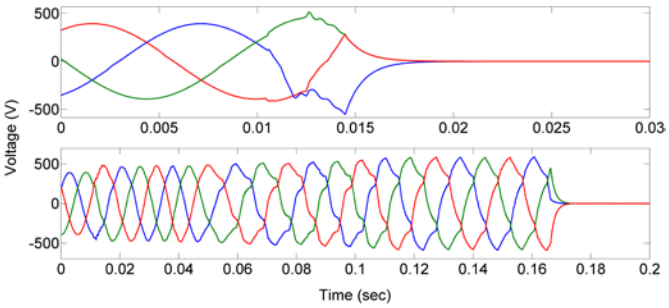

Figure 6. Worst case LRO test runs showing 141% peak overvoltage for Inverter 1 (top) and 152% peak overvoltage for Inverter 4 (bottom).

For each test, the inverter was run at full power, and the load was set to approximately match the inverter output in order to minimize grid current. The load was resistive for unity power factor, and a combination of resistive and inductive or capacitive for tests at ±0.80 power factor (negative power factor is leading current, using generator convention). The test was started with switch S1 closed and switch S2 opened in Figure 1. Once running at steady state, a timing circuit was used to open S1 approximately 8-10 ms before switch S2 was closed, in order to protect the grid simulator. A balanced load was added to the circuit so the inverter would continue to operate at nominal conditions for the small period of time after S1 was opened, creating an island for a brief time window. AC current was measured at each of the three phases at the inverter terminals to determine the fault current contributions using a 10 MHz probe, and measurements were sampled at 10 MHz at the oscilloscope in order to capture high frequency content of the fault current. All tests were run with VRT and FRT enabled, and both VVC and FWC disabled.

The normalized peak currents of all single-phase (top) and three-phase (bottom) fault test results are shown in Figure 7. The magnitude of the peak fault current was largely independent of which phase was faulted, so a total of nine test cases are summarized together for each power factor value in the top figure. Table III shows the mean and maximum peak fault current for each set of three-phase fault tests at different power factors (single-phase summary is not provided since peak currents were much lower).

For single-phase faults, three of the four inverters had a slightly higher mean peak current at -0.80 power factor, but the range of peak values significantly overlapped for all inverters at all power factors. Inverters 1, 3, and 4 had very similar magnitudes and ranges of fault currents; Inverter 2 had both the largest peak current values and the widest range of responses. The maximum single-phase fault current peak was 202.7 A (2.99 per unit) from Inverter 2. The reported fault maxima are the peak of any of the three phases, and in some cases occurred on a phase other than the one that was faulted.

For three-phase faults, Inverters 1 and 2 had the most consistently low and repeatable peak fault currents. Inverter 3 had the largest range and magnitude of fault currents peaks, with a maximum across all tests of 683.3 A (11.16 per unit) at unity power factor. For three-phase fault data, the reported currents are the maximum of any of the in individual phases, and are not additive across all phases. Power factor had no clear effect on peak fault currents for single-phase or three-phase faults.

Fault current peaks were typically very short in duration, on the order of tens of microseconds. The 683.3 A fault peak was the largest for all test cases but only had duration of ~39 µs, as seen in Figure 8. However, inverters sometimes continued operation for several hundred milliseconds after the peak current event occurred. In no test cases did the fault current open the 60 A, Type J time delay fuses.

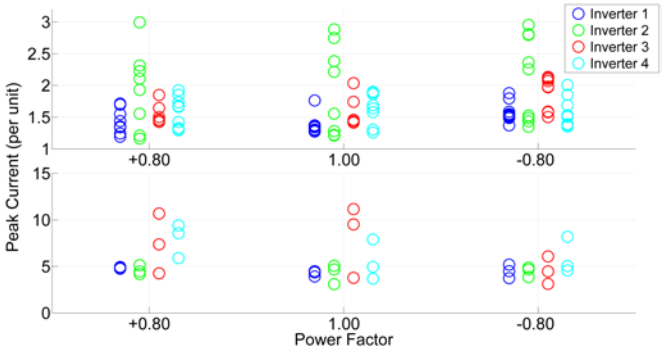

Figure 7. Normalized peak phase fault current for single phase to ground tests (top) and three phase to ground tests (bottom)

TABLE III. MEAN AND MAXIMUM PEAK CURRENTS FOR THREE PHASE TO GROUND FAULT TESTS

Power Factor	Metric	Inverter Number and Peak Current (A)			
		1	2	3	4
+0.80 (lagging)	Mean	198.2	310.5	455.3	446.5
	Max	202.0	347.3	654.0	528.0
1.00	Mean	173.8	290.0	499.1	309.3
	Max	183.3	343.3	683.3	443.3
-0.80 (leading)	Mean	182.7	302.5	278.9	333.1
	Max	212.0	330.0	372.0	460.0

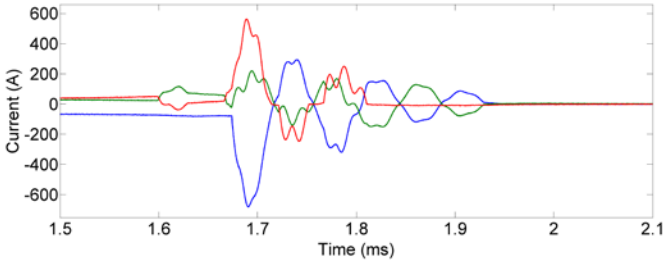

Figure 8. Phase currents from Inverter 3 during fault testing, showing maximum peak fault current of 683.3 A

CONCLUSIONS

The tests described in this paper examined the response of several PV inverters with advanced GSFs to abnormal grid conditions. Four commercially available inverters rated 24-36 kW were characterized for their ride-through, FPF, VVC, and FWC capability and were subjected to anti-islanding, LRO, and fault conditions with different combinations of these GSFs enabled. Islanding tests showed that neither FWC nor VVC had a clear effect on ROT. All inverters were shown to meet the two second ROT maximum required by existing standards. LRO tests yielded no clear dependence on VVC or inverter to load power ratio on the peak voltages observed, which typically had very short duration and never exceeded 152% of nominal. Single- and three-phase to ground fault tests showed no clear dependence on power factor for peak fault current contribution. The results indicate a significant variation in how GSF-enabled inverters respond to various grid conditions. Future work will examine the effects of varying output power levels, choosing different GSF settings, further investigation into the effect of FWC on islanding ROT, and interactions among multiple inverters.

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