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DOI 10.1109/ISIE45063.2020.9152442

Publication date 2020

Document Version Accepted author manuscript

Published in 2020 IEEE 29th International Symposium on Industrial Electronics, ISIE 2020 - Proceedings

Citation (APA)

Beloqui Larumbe, L., Qin, Z., & Bauer, P. (2020). On the Importance of Tracking the Negative-Sequence Phase-Angle in Three-Phase Inverters with Double Synchronous Reference Frame Current Control. In 2020 IEEE 29th International Symposium on Industrial Electronics, ISIE 2020 - Proceedings: Proceedings (pp. 1284-1289). Article 9152442 (IEEE International Symposium on Industrial Electronics; Vol. 2020-June). IEEE. https://doi.org/10.1109/ISIE45063.2020.9152442

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On the Importance of Tracking the Negative-Sequence Phase-Angle in Three-Phase Inverters with Double Synchronous Reference Frame Current Control

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Abstract—A voltage imbalance at the AC terminals of a threephase inverter creates a ripple in the power signal on the DC side. In order to minimize this ripple, several techniques can be applied, in which a double Synchronous Reference Frame (SRF) current control structure is very typical. In this approach, both the positive and negative sequence currents are controlled. This technique has been shown to have an adequate response against imbalances; however, this paper shows that in the typical implementation of the double SRF control, the output AC pqinstantaneous powers will have a constant error due to the phaseangle misalignment of the negative sequence with the positive sequence. Based on mathematical formulations and simulation results, this paper shows that this AC-power error exists, and that it is due to the above reason. In order to overcome this, this paper proposes to have a phase-tracking system that specifically follows the negative sequence phase-angle. The results show that this implementation is able to properly control the output AC power.

Index Terms—Phase-Locked Loop, Negative sequence, double Synchronous Reference Frame, Dual current control, Converter

I. Introduction

In the context of an increasing population of powerelectronic converters (PECs), ensuring their adequate dynamic response has become crucial for the proper operation of power systems. In order to achieve that, different control approaches can be implemented in the converters. In offshore wind turbine inverters, for example, it is very typical to implement a control structure called double Synchronous Reference Frame (SRF) or dual-controller [1] due to its superior dynamic performance under unbalanced grid conditions [2]–[4].

In order to be able to inject a constant instantaneous three-phase power in the presence of a voltage imbalance, it is necessary to inject a specific set of positive- and negative-sequence currents [5]. In order to do that, the double SRF current control manages simultaneously and separately both sequences, for which two dq-frames are built: one rotating with the positive sequence and one with the negative sequence. For building these two SRFs, the phase-angles of both sequences are needed. The positive sequence is typically tracked by using a Phase-Locked Loop (PLL). By contrast, in the typical implementation (for example, as shown in [1]–[4]), the negative sequence is not tracked, and it is simply assumed that its phase-angle is equal to the positive sequence phase-angle negated.

However, the above assumption is not true. What this paper brings is that this implementation will create a steady-state error in the output power. Also, this paper shows how this steady-state error does not appear whenever the phase-angle of the negative sequence is specifically tracked, and it discusses different methods to achieve it.

The mathematical explanation as to why this error appears in the typical double SRF implementation is given in Section II. Several case studies are defined in Section III and, in Section IV, simulation results show that this error exists, and that it can be avoided by also tracking the negative sequence. Since the main purpose of the paper is not to thoroughly discuss how to track the negative sequence, but rather that it is necessary, different possible tracking methods are discussed only at the end of the paper, in Section V. The paper concludes with Section VI.

II. On the necessity of separately tracking the negative sequence

A. The double SRF control structure

This paper investigates a three-phase inverter as in Fig. 1. The converter is controlled in grid-feeding mode with a dual controller or double SRF current control. The typical implementation is shown in Fig. 2 a). In here, the output voltage of the converter $v_{\rm abc}$ is used by the phase-angle tracking system (which, in this case, is just a three-phase SRF-PLL) to track the positive-sequence phase-angle (θ_{1p}) , generating the signal θ_{PLL} . With θ_{PLL} , a dq-frame is created that in steady-state rotates at $\theta_{\rm PLL} = \theta_{1\rm p} = \omega_1 t$, where ω_1 is the fundamental frequency. In this frame, the positive sequence current appears as a DC component that can be tracked with no steady-state error with the use of a PI controller, H_i . The negative sequence in this frame appears at the frequency $2\omega_1$, which can be filtered through a notch filter $H_{\rm n}$. Similarly, another dq-frame is created for controlling the negative sequence currents, for which the

This work is funded by TKI Wind op Zee under the project Large Offshore Wind Harmonics Mitigation (LOW-HarM) by the Rijksdienst voor Ondernemend, The Netherlands.



Fig. 1: Schematic of the inverter under study.

phase-angle θ_{PLL} is also used but the rotation is done in the opposite direction. This dq-frame, then, rotates at the frequency $-\theta_{\text{PLL}} = -\theta_{1\text{p}} = -\omega_1 t$. An extra term, θ_{comp} , can be used in the dq-to- $\alpha\beta$ transformations to compensate for the filtering, computation and modulation delay at ω_1 [6]. The decoupling constant K_d is commonly selected as $L\omega_1$.

Note in Fig. 2 a) that, in the usual implementation, in order to transform the currents into the positive dq-frame, the transformation $e^{j\theta} = e^{j\theta_{\rm PLL}}$ is used, whereas for the negative sequence $e^{-j\theta} = e^{-j\theta_{\rm PLL}}$ is used (which is, in essence, an $e^{j\theta}$ transformation with the angle negated). However, this ignores the fact that there may be a steady-state phase-shift between the positive and negative sequences. As acknowledged in [7], in reality, the phase-angle of the negative sequence is $\theta_{\rm 1n} = -\omega_{\rm 1}t - \phi_{\rm n}$, so if the phase-angle $-\omega_{\rm 1}t$ is used for constructing the second SRF, a steady-state error will occur. This error is elaborated in subsection II-C.

In contrast to the typical implementation, this paper proposes to use the scheme in Fig. 2 b), where both sequences are targeted, and in steady-state: $\theta_{\text{PLL}} = \theta_{1\text{p}} = \omega_1 t$ and $\theta_{\text{PLL}} = \theta_{1\text{n}} = -\omega_1 t - \phi_{\text{n}}$. Some methods for tracking both sequences are shown in Section V.

B. Frame transformations with the negative sequence

The positive and negative sequence voltages are shown in (1) and (2), respectively.

$$v_{\rm pa}(t) = V_{\rm pRMS}\sqrt{2}cos(\omega_1 t)$$

$$v_{\rm pb}(t) = V_{\rm pRMS}\sqrt{2}cos(\omega_1 t - \frac{2\pi}{3})$$

$$v_{\rm pc}(t) = V_{\rm pRMS}\sqrt{2}cos(\omega_1 t - \frac{4\pi}{3})$$

$$v_{\rm na}(t) = V_{\rm nRMS}\sqrt{2}cos(\omega_1 t + \phi_{\rm n})$$

$$v_{\rm nb}(t) = V_{\rm nRMS}\sqrt{2}cos(\omega_1 t + \phi_{\rm n} - \frac{4\pi}{3})$$

$$v_{\rm nc}(t) = V_{\rm nRMS}\sqrt{2}cos(\omega_1 t + \phi_{\rm n} - \frac{2\pi}{3})$$
(2)

The transformation of these *abc*-voltages to the $\alpha\beta$ -frame is shown in Fig. 3. In this figure, the phasor of phase *b* in the positive sequence is advanced with respect to phase *a*, in agreement with the traditional Clarke transformation shown in (3) (in which the positive-sequence rotates counterclockwise).

$$C = K \begin{bmatrix} \cos(0) & \cos(-\frac{4\pi}{3}) & \cos(-\frac{2\pi}{3}) \\ \cos(-\frac{\pi}{2}) & \cos(-\frac{11\pi}{6}) & \cos(-\frac{7\pi}{6}) \end{bmatrix} = K \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}$$
(3)



(b)

Fig. 2: Double Synchronous Reference Frame (a) typical implementation (b) proposed implementation by specifically tracking the negative sequence.

With respect to the negative-sequence, note that if a standard transformation is imposed in the negative sequence voltages (or currents) as: $v_{n\alpha\beta} = Cv_{nabc}$, then the resulting $\alpha\beta$ vector rotates clockwise, and this $\alpha\beta$ voltage will be defined with respect to the axes α_p and β_p shown in Fig. 3. From this reference frame, the necessary phase-angle to input to the rotational matrix shown in (4), in order to get a dq-frame alligned with the $\alpha\beta$ vector is $-\omega_1 t - \phi_n$ (i.e. $T(\theta = -\omega_1 t - \phi_n)$).

$$T(\theta) = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}$$
(4)

Of course, it is possible to define another $\alpha\beta$ -frame from which the necessary θ to get a dq-frame alligned with the $\alpha\beta$ vector is $-\omega_1 t$. This $\alpha\beta$ -frame is given by α_n and β_n in Fig. 3. However, in order to reference the $\alpha\beta$ vector from this frame, the matrix in (3) should not be used, but rather (5) (i.e. (6) holds).

$$C_{\text{neg}} = K \begin{bmatrix} \cos(0+\phi_{\text{n}}) & \cos(-\frac{4\pi}{3}+\phi_{\text{n}}) & \cos(-\frac{2\pi}{3}+\phi_{\text{n}}) \\ \cos(-\frac{\pi}{2}+\phi_{\text{n}}) & \cos(-\frac{11\pi}{6}+\phi_{\text{n}}) & \cos(-\frac{7\pi}{6}+\phi_{\text{n}}) \end{bmatrix}$$
(5)

$$T(\theta = -\omega_1 t - \phi_n)C = T(\theta = -\omega_1 t)C_{\text{neg}}$$
(6)

However, note that in order to construct C_{neg} , ϕ_n is needed anyway. Since ϕ_n varies over time and it is different in different converters, it is needed to continuously track it. Further, note that if C_{neg} is used, then the $\alpha\beta$ -frame signals of the positive and negative sequences would not be referred to the same frame. Thus, it makes more sense to use a standard Clarke transformation as in (3) and then apply $T(\theta = -\omega_1 t - \phi_n)$. In this case, the final α and β axes chosen would be α_p and β_p .

C. Steady-state error in typical implementation of double SRF

The typical implementation of the double SRF assumes that $\theta_{1n} = \theta_{1p} = -\omega_1 t$, which means that, in the typical implementation, the *d*-axis in the negative sequence SRF would not lay on top of the $\alpha\beta$ vector of the negative sequence ($v_{n\alpha\beta}$ in Fig. 3). This axis is shown in Fig. 3 under the label " d_n wrong"; whereas the correct axis would be " d_n right".

Assuming that K = 2/3 is chosen in (3), then the dq values of the negative sequence voltage in the negative SRF should be as in (7). However, if $-\theta_{1p}$ is used to construct the negative SRF, then the dq values would be according to (8), which are wrong.

$$v_{\rm d \ SRF -} = V_{\rm nRMS} \sqrt{2}$$

$$v_{\rm q \ SRF -} = 0$$
(7)

$$v_{\rm d \ wrong \ SRF} = V_{\rm nRMS} \sqrt{2cos(\phi_{\rm n})}$$
(8)

$$v_{
m q\ wrong\ SRF}$$
 _ = $-V_{
m nRMS}\sqrt{2sin(\phi_{
m n})}$



Fig. 3: Transformation of *abc*-frame voltages to the $\alpha\beta$ -frame.

The whole control philosophy of the double SRF is to construct one SRF aligned with the positive sequence (in steady state, $v_{q \text{ SRF } +} = 0$) and another aligned with the negative sequence (in steady state, $v_{q \text{ SRF } -} = 0$). If the alignment is correct, then it is possible to use the d-axis to control the active power, and to use the q-axis to control the reactive power. In normal operation, without voltage imbalance, usually the dq current references for the negative SRF would be zero. However, if there is a voltage imbalance, it is necessary to inject a controlled set of negative-sequence currents in order to have an instantaneous three-phase power without ripple [5], so these references would not be zero [1].

However, if the negative SRF is not properly aligned, a current reference in its q-axis would create both active and reactive power in the negative sequence, so the controller will fail its purpose. Note that it is not possible to compensate this error, because ϕ_n is arbitrary. This error will be shown with simulations in Section IV using the case studies defined in Section III.

III. Case study definitions

Let's define the Case A as the case in which the output voltage of the inverter is unbalanced as in (9), with $V_{\rm RMS} = 690/\sqrt{3}$. In this case, the amplitude of the voltage in phase a is different from such in phases b and c, both of which are equal and lower than in phase a.

$$v_{\rm a}(t) = V_{\rm RMS}\sqrt{2}cos(\omega_1 t)$$

$$v_{\rm b}(t) = 0.4V_{\rm RMS}\sqrt{2}cos(\omega_1 t - \frac{2\pi}{3})$$

$$v_{\rm c}(t) = 0.4V_{\rm RMS}\sqrt{2}cos(\omega_1 t - \frac{4\pi}{3})$$
(9)

If the *abc*-to-0*pn* sequence transformation is applied to $v_{abc}^T = [V_{\text{RMS}} \angle 0, 0.4 V_{\text{RMS}} \angle \frac{2\pi}{3}, 0.4 V_{\text{RMS}} \angle \frac{4\pi}{3}]$ using (10) (with $\alpha = e^{i\frac{2}{3}\pi}$), then the resulting phasor vector in the 0*pn* sequences would be: $v_{0pn}^T = [79.7 \angle 0, 239 \angle 0, 79.7 \angle 0]$. In this case A, there is an imbalance at the terminals of the converter of 33.3%, however $\phi_n = 0^\circ$.

$$A^{-1} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix}$$
(10)

Now, let's define the Case B as in (11). In this case, the amplitude of the voltage in phase a and b are equal between each other but different from such in c.

$$v_{\rm a}(t) = V_{\rm RMS}\sqrt{2}cos(\omega_1 t)$$

$$v_{\rm b}(t) = V_{\rm RMS}\sqrt{2}cos(\omega_1 t - \frac{2\pi}{3})$$

$$v_{\rm c}(t) = 0.3V_{\rm RMS}\sqrt{2}cos(\omega_1 t - \frac{4\pi}{3})$$
(11)

If the *abc*-to-0*pn* transformation is applied to $v_{abc}^T = [V_{\rm RMS} \angle 0$, $V_{\rm RMS} \angle \frac{2\pi}{3}$, $0.3 V_{\rm RMS} \angle \frac{4\pi}{3}]$, then the resulting phasor vector in the 0*pn* sequences would be: $v_{0pn}^T = [92.95 \angle -1.05$, $305.42 \angle 0$, $92.95 \angle 1.05]$. In this case B, the imbalance is of 30.4%, however $\phi_{\rm n} = 1.05$ rad = 60°.

In case A, the dq values for the positive sequence voltage would be $v_{dq SRF +}^T = [338, 0] V$, no matter which phasetracking system is implemented. Further, as $\phi_n = 0^\circ$, the dqvalues for the negative sequence voltage would also be equal no matter the implementation: $v_{dq SRF -}^T = [113, 0] V$.

In case B, $v_{dq SRF+}^{T} = [432, 0]V$, no matter which phase-tracking system is implemented. As $\phi_n = 60^\circ$, the dq values for the negative sequence voltage for the typical implementation of the phase-tracking system would be $v_{dq SRF-}^{T} = [66, -114]V$, whereas the correct values would be $v_{dq SRF-}^{T} = [131, 0]V$.

A. Practical comment: how common are these imbalances?

Note that it is not necessary to have an imbalance in the *abc* phase-angles in order to have a $\phi_n \neq 0$. Having differences in the voltage magnitudes is usually enough. This is an important clarification due to the fact that faults, which are a very important cause of voltage imbalances, usually provoke a significant drop in the magnitude of one or several phases, but not necessarily in the phase-angles.

Case B, for instance, could be a simplified example of a very common single-phase fault. In contrast, Case A is not a very common case. It is true that, with (10), it can be easily proven that if the voltages of phases b and c are equal to each other (and lower) than in phase a, the phaseangle of the negative sequence with respect to the positive sequence would be zero. Thus, if a two-phase fault would occur at the terminals of the converter in such a way that two phases would exactly have the same magnitude, then it is true that $\phi_n = 0$.

However, if the voltages in the two other phases are not exactly equal, $\phi_n \neq 0$; and, most importantly, if there is any element in between the fault and the terminals of the converter, and this element is not perfectly symmetrical, then it does not matter that at the fault point $\phi_n = 0$ because at the terminals of the converter $\phi_n \neq 0$. The case A defined in (9), is thus a mere academic exercise that is not very typical in real situations. Apart from this, other voltage configurations can also lead to $\phi_n = 0$, but in general they are even more arbitrary.

In relation to the magnitude of the imbalances proposed in Section III, it is worth to note that they really depend on the type of fault, the location of the fault, and other considerations. In here, [8] was used as a reference. This paper [8] is focused on studying the grid-side inverter behaviour against unbalanced faults for type IV wind turbines, and shows that a solid one-phase fault on the local bus bar (at the HV side of the wind turbine transformer) may lead to a 46.2% negative sequence voltage; a local onephase fault through impedance may lead to a 19.6% negative sequence voltage; whereas a remote solid one-phase fault (on the transmission line) may lead to a 44.7% negative sequence voltage at the local bus bar. Taking into account these values, imposing a voltage imbalance of around 30% in the simulations seemed a reasonable middle-point to illustrate the concept of this paper.

TABLE I: Main parameters of inverter

	Description	Value	Unit
$V_{\rm dc}$	DC Voltage	1500	V
V _{POC}	Rated AC Voltage	690	V
Prated	Rated Power	4.3	MW
L	Output Inductor	19	μH
RL	Resistance of Output Inductor	5	$m\Omega$

TABLE II: Control parameters of the inverter

	Description	Value	Unit
$f_{\rm sw}$	Switching Frequency	2500	Hz
f_{s}	Sampling Frequency	5000	Hz
$K_{\rm d}$	Current Coupling Compensation Gain	0.006	Ω
$K_{\rm p}$	Proportional Constant PI Current	0.018	Ω
K_{i}	Integral Constant PI Current	4.7	Ω/s
$K_{\text{p-PLL}}$	Proportional Constant PI PLL	0.32	rad/s
K _{i-PLL}	Integral Constant PI PLL	15.3	rad/s^2

IV. Simulation Results

Simulations for the case studies in Section III are presented here. Tables I and II show the inverter parameters.

For the sake of simplicity, and in order to have a more clear comparison, only the current control loop was considered in the simulation. This means that both the DC voltage and the current references were kept constant.

In reality, whenever an imbalance occurs at the terminals of an inverter, the typical consequence is to have a very high second-harmonic ripple in the DC power due to modulating interactions between the positive and negative sequence components of the AC voltage and current [8]. Thus, in a lot of applications the double SRF is used precisely so that, whenever there is an imbalance at the terminals of the inverter, the voltage ripple at the DC side is minimized. In order to achieve this, constant AC power needs to be injected. As the voltage is unbalanced, this means that the AC currents should be imbalanced too [8], and that very specific current references should be provided to the double SRF current control.

For the sake of this paper, however, the objective is to show that with the typical implementation of the double SRF, the obtained SRF for the negative sequence would be misaligned. In order to check this, the current references specified in (12) were fed to the inverter. The output power of the inverter due to the positive SRF and due to the negative SRF are described in (13) [8] ($P_{+\text{SRF}}$ and $P_{-\text{SRF}}$, respectively). Note that, due to the fact that in the simulations the current references are not properly updated (references are kept constant), an additional secondharmonic term in the power will appear (P_{2nd} as shown in (13)). Thus, the DC power P_{dc} would have a constant value due to $P_{+\text{SRF}}$ and $P_{-\text{SRF}}$ and a 100 Hz ripple.

$$i_{d+\text{ref}} = 5088 A ; i_{q+\text{ref}} = 0 A$$

 $i_{d-\text{ref}} = 0 A ; i_{q-\text{ref}} = 5088 A$ (12)



Fig. 4: Simulation results for Case A (a) voltage; and comparison of the phase-angles obtained with the typical- and the proposed implementation with the exact values for constructing (b) positive SRF (c) negative SRF.

$$P_{+\text{SRF}} = \frac{3}{2}(v_{d+}i_{d+} + v_{q+}i_{q+})$$

$$P_{-\text{SRF}} = \frac{3}{2}(v_{d-}i_{d-} + v_{q-}i_{q-})$$

$$P_{2\text{nd}} = \frac{3}{2}(v_{d-}i_{d+} + v_{q-}i_{q+} + v_{d-}i_{d-} + v_{q-}i_{q-})$$
(13)

 $P_{\rm dc} = P_{+\rm SRF} + P_{-\rm SRF} + P_{\rm 2nd}$

The key point in this simulation is to note that, if the negative SRF is perfectly aligned, then $v_{q-} = 0$ and, given that i_{d-} should be close to 0 (as it is following a zero reference as shown in (12)), then the $P_{\text{-SRF}}$ is close to zero. This means that, if the negative SRF is perfectly alligned with the negative sequence, the P_{dc} should have a constant value equal to $P_{+\text{SRF}}$, plus a 100 Hz ripple due to the cross-modulation of the positive and negative sequence. However, if the negative SRF dq-frame is not properly aligned, $v_{q-} \neq 0$, so then due to the non-zero i_{q-} , $P_{-\text{SRF}} \neq 0$, and P_{dc} and $P_{+\text{SRF}}$ would be more different.

The results for the case in which the voltage is described by (9) (case A, with $\phi_n = 0$) are shown in Fig. 4. As it can be seen, given the voltage in Fig. 4 a), the corresponding phaseangle signals produced by the typical and proposed implementation of the phase-angle tracking system are equal to each other, and are equal to the exact values. If the voltage at the output of the inverter is transformed into dq values with the typical implementation, Fig. 5 a) is obtained, which is equal to such of the proposed implementation (Fig. 5 b)). These values match the theoretical values found on Section III. As expected, then, the P_{dc} has a constant value due to $P_{+\text{SRF}}$ and a 100 Hz ripple, while $P_{-\text{SRF}} \simeq 0$. This can be seen in Fig. 6, where P_{dc} was properly filtered to eliminate the switching ripple and to reduce the 100 Hz ripple for clarity.

The results for the case in which at the output of the converter the voltage is described by (11) (case B, with



Fig. 5: Simulation results for Case A. dq-frame voltage obtained with (a) typical implementation; and (b) proposed implementation.



Fig. 6: Simulation results for Case A. Power waveforms obtained with (a) the typical implementation; and (b) the proposed implementation.

 $\phi_n = 60^\circ$) are shown in Fig. 7. As it can be seen, given the voltage in Fig. 7 a), the corresponding phase-angle signals produced by the typical and proposed implementation of the phase-angle system are equal to each other for the positive sequence, but not for the negative sequence. It can be seen in Fig. 7 c) that the typical implementation has a steadystate error when tracking the phase-angle of the negative sequence. This means that, with the typical implementation, the positive sequence voltage values in the dq-frame would be correct, but not for the negative sequence, as shown in Fig. 8 a). Whenever using the proposed implementation, the dq voltages for the negative sequence are correct. All these dq-values match those obtained in Section III. In this case study B, if the typical implementation of the phase-tracking system is used, the $P_{-SRF} \neq 0$, so P_{dc} differs from P_{+SRF} , as it can be seen in Fig. 9 a). This means that, as explained above, the negative sequence SRF is not properly aligned with the negative sequence voltage. In contrast, when using the proposed implementation (see Fig. 9 b)), $P_{-\text{SRF}} \simeq 0$, which means that the negative SRF is properly aligned.

V. Tracking the negative sequence: implementation issues

There are multiple ways in order to exclusively track the positive sequence phase-angle. In this paper, for the "typical implementation" approach, a standard SRF-PLL was used, shown in Fig. 10.

Tracking the negative sequence, however, is not an easy task. The main difficulty is that it is a very small signal in comparison to the dominant signal in the voltage, the positive sequence. Thus, in order to obtain θ_{1n} , one logic option would be to first filter the positive sequence from the negative sequence signal in order to obtain a clean $[v_{an}(t), v_{bn}(t), v_{cn}(t)]$, which can be introduced in a regular three-phase SRF-PLL as shown in Fig. 10. In order



Fig. 7: Simulation results for Case B (a) voltage; and comparison of the phase-angles obtained with the typical- and the proposed implementation with the exact values for constructing (b) positive SRF (c) negative SRF.



Fig. 8: Simulation results for Case B. dq-frame voltage obtained with (a) typical implementation; and (b) proposed implementation.

to filter the positive sequence signal from the negative sequence signal (and viceversa), a DDSRF-PLL could be used (more information on this type of PLL in [9]). This type of PLL uses a decoupling network to clean the positive sequence signal from the negative sequence signal, having in the end both signals separated. On the one hand, this approach has shown to properly operate in unbalanced situations, however, the performance of the DDSRF-PLL is also compromised in the case study B due to the fact that its decoupling network does not take into account ϕ_n . An improved version of this type of PLL, then, would be necessary for achieving the desired performance.

The phase-tracking system used in this paper, thus, is different. In this paper, three different PLLs, one per phase *abc*, were used. Once the phase-angle and RMS value of each phase are known, $[\theta_{PLL-a}(t), \theta_{PLL-b}(t), \theta_{PLL-c}(t)]$ and $[V_{RMS-a}(t), V_{RMS-b}(t), V_{RMS-c}(t)]$, then a sequence transformation similar to (10) can be performed. Note, however, that the calculation will give the phase-angle of the negative sequence defined by (2), which is $\omega_1 t + \phi_n$, although $-\omega_1 t - \phi_n$ must be used in (4).

Note that tracking the negative sequence is not only challenging due to the dominance of the positive sequence, but also because, in situations of small imbalances, noise and harmonics might have a comparable amplitude. Thus, careful implementation with proper filtering is necessary.



Fig. 9: Simulation results for Case B. Power waveforms obtained with (a) the typical implementation; and (b) the proposed implementation.



Fig. 10: Three-phase SRF-PLL.

VI. Conclusions

This paper has shown that, in order to properly implement a double SRF control structure, in which the AC power is properly controlled during imbalances, the negative sequence SRF needs to be properly aligned, for which the negative sequence phase-angle needs to be specifically tracked. This requirement comes from the fact that the negative sequence is typically not aligned with the positive sequence, and a steady-state phase-angle displacement usually exists between the two. In order to track the negative sequence phase-angle, different approaches can be taken. This paper has discussed several options, although further research is advised.

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