Boosted Gain Programmable OpAmp with Embedded Gain Monitor for Dependable SoCs

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Abstract—**SoCs used in safety-critical applications need to be dependable. However in the deep-submicron region, different kinds of aging effects like negative bias temperature instability (NBTI) make the SoCs, especially the analog/mixed-signal parts, undependable. In this paper, a dependability-improved Opamp is designed based on gain programmability and digital gain monitoring. To accomplish an extra gain range for tuning in 65nm technology, a new voltage-gain boosting method is proposed to provide a maximum 92dB gain in a single amplification stage. The NBTI influence is investigated using Cadence RelXpert and dependability properties for the Opamp are provided.**

Keywords-gain boosting; Opamp; dependability; NBTI.

I. INTRODUCTION

Reliability issues in CMOS have been around for more than 20 years. Although rarely noticed until recently by circuit designers, most of the reliability problems were solved at the manufacturing plants. With the technology entering the deep-submicron region, reliability issues cannot be easily solved in the old ways. In safety-critical applications, such as automotive, dependability is used instead, which concerns more than just reliability. Dependability research can answer many questions like when the circuits are expected to get out of the performance due to aging (reliability), how to repair the circuits at that time (maintainability), how long the circuit is not available due to this repair (availability), and whether the circuits will cause a safety problem or not due to their out-of-performance. Detailed definitions of dependability can be found in [1].

In order to prepare deep-submicron SoCs for safety-critical applications, the dependability of the SoCs, especially the analog/mixed-signal IP based SoCs, need to be improved. There are not many publications concerning the dependability of SoCs. Most of them are dealing with digital IP-based SoCs and use redundant components together with dynamic routing to improve the dependability. The same methods can be applied to analog/mixed-signal IPs. Yet the area and power cost will be very high. In addition, the rerouting of analog signals will cause additional problems like increased noise and parasitics. The usage of reliability-sensors based calibration could be another option. However, the research on reliability is still progressing and new discoveries, such as the stochastic of the aging, pop up frequently. This makes the reliability sensors now less confident to work with as the conventional calibration methods.

Our idea for improving the dependability of analog/mixed-signal IPs is making each block digitally observable and digitally controllable. By facilitating this, the system can check important performance parameters, like the gain of an Opamp, and detect potential dependability problems in advance. Then the corresponding maintenance can be chosen to take place at the IP level (like the conventional self-calibration method) or at system level [2]. Among different kinds of analog building blocks, Opamps are the most basic ones and at the same time, the most important ones. The negative bias temperature instability (NBTI) effect is the dominating aging issue in 65nm CMOS technology. It can cause a threshold increase and trans-conductance decrease in the PMOS transistors, and hence reduce the gain of the Opamp and increase the offset. To solve the aging problem and hence improve the dependability, an Opamp which uses a new gain boosting method with programmable gain and embedded digital gain monitor have been designed and simulated in this paper.

Normal gain programming methods are based on reducing the maximum achievable gain to create additional tuning range. In order to keep the gain performance in terms of frequency behavior while, at the same time, improving the dependability, a new gain boosting method will be proposed in section II. Based on this new gain boosting technique, an example 92dB single stage Opamp has been designed in 65nm low-power technology. Its gain programmability and digital gain monitoring are discussed in section III. The dependability simulation results, which include NBTI aging simulation, are shown in section IV. The conclusion is provided in section V.

II. NEW GAIN BOOSTING TECHNIQUE

The commonly used voltage gain-boosting method was introduced by Bult [3]. It can boost the output impedance and hence the gain to $(1+A_L)$ times the original one. Here A_L denotes the loop gain of the boosting feedback loop. If the term $(1+A_L)$ can be kept larger than one, the original gain can be boosted without sacrificing the unit-gain frequency. This means the single gain-stage loop approach is preferred, which has less than 90^o phase shift before the unit loop-gain frequency. However, the repeated usage of the same boosting technique [3] will cause stability problems, and hence require frequency compensations. The combined usage of different gain-boosting techniques which use a single gain stage in each gain boosting loop is a good choice to accomplish a high gain [4]. Thus new gain boosting methods are required, which can combine with the old ones and accomplish the gain margin for the programmability as well as keeping the high gain.

Our new gain-boosting method is shown in Fig. 1, in which all NMOS and PMOS transistors are supposed to be matched.

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The gate voltage of the NMOS transistor N1 is controlled by the circuit in the square box of Fig. 1 to boost the gain. The operation can be explained as follows.

The output impedance can be evaluated by measuring the small-signal current at the output while shifting the output voltage. For example, in Fig. 1, assume at the DC operation point, no current will flow into the output node, $I_{out}=0$. Next, shift the voltage from V_{out} to $V_{out}+\Delta$. The current flow into the output can now be used to detect the output impedance.

If the voltages at the B and C nodes can be set to:

$$V_B = V_{out} - \Delta \qquad V_C = V_{out} + \Delta \tag{1a/b}$$

then, the currents in the two branches I_1 and I_2 will be as shown in Fig. 1. Suppose I_0 is the quiescent current if the output voltage is at its DC operation point V_{out}. The g_n and g_p are the drain-source conductances of the NMOS and PMOS transistors. Since $I_X = I_2$ (same V_{gs} and V_{ds}), the output current I_{out} will be:

$$I_{out} = I_0 + \Delta g_n + I_X - 2(I_0 - \Delta g_p) = 0 \tag{2}$$

Equation (2) shows that the output current is zero and hence does not change with the output voltage shifting which means infinite gain.

The two voltage amplifiers VA1 and VA2, indicated in Fig.1, are used to provide feedback loops and set the required voltages at nodes B and C. Since the loop gain cannot be infinite in reality, the voltages at B and C will be close to the required ones but will still have small errors:

$$V_B = V_{out} - \Delta A_{LP}/(1+A_{LP}) \quad V_C = V_{out} + \Delta A_{LN}/(1+A_{LN}) \tag{3a/b}$$

where A_{LN} and A_{LP} are the loop gains as shown in Fig. 1. The actual output impedance Z_{out_GB} and voltage gain A_{G_B} will be:

$$Z_{out\_GB} = \Delta / I_{out} = [(1+A_{LP})//(1+A_{LN})] / (g_n + g_p) \tag{4}$$

$$A_{G\_B} = [(1+A_{LP})//(1+A_{LN})] A_{orig} \tag{5}$$

In (4) and (5), the symbol "//" follows the same calculation means of resistors in parallel. For clarity, suppose the loop gain A_{LN} and A_{LP} are both equal to A_L. Then (5) can be simplified to:

$$A_{G\_B} = 0.5 \cdot (1+A_L) A_{orig} \tag{6}$$

From (6), the gain is boosted to $(1+A_L)/2$ times the original one, which is similar to other gain-boosting methods.

The new gain-boosting method shown in Fig. 1 is suitable for fully differential Opamps since it requires the negative output signal. The advantage of this method over others is that it does not need cascode transistors, which make it possible to be used in low-power supply and pseudo-differential systems. In addition, the voltages at the B and C nodes are copies of the differential output voltages. Hence they could be used as another pair of outputs and are very suitable for driving class AB output stages. The gain programmability feature can be realized by tuning the gain of the voltage amplifiers VA1 or VA2, which will not influence the operating conditions of the original circuits.

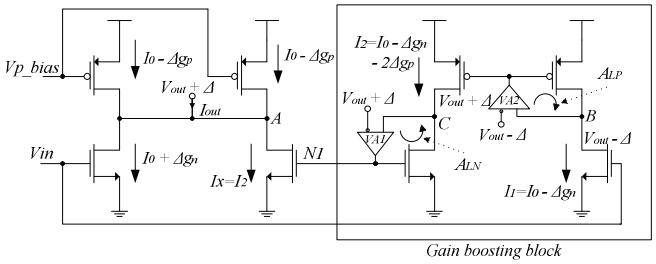

Figure 1. New gain boosting configuration

III. PROGRAMMABLE GAIN BOOSTING OPAMP WITH EMBEDDED DIGITAL GAIN MONITOR

In this section, a single-stage Opamp is shown which uses both the new gain-boosting technique and the one in [3] to provide more than 90 dB gain. It will be using gain programmability together with a digital gain monitor to result in a highly dependable Opamp IP [2].

A. Gain-Boosted Programmable Opamp

Fig. 2 shows a single-stage Opamp designed in 65nm low-power CMOS technology. The gain boosting technique from [3] is used to boost the cascode output impedance, and our new gain boosting technique is employed to boost the overall output. In Fig. 2.a, the boosting feedback loops include VA1-P1-P2, VA3-P3-P4, VA2-N2-N1 and VA4-N4-N3. They are designed to be single-gain stage loops. Hence VA1~VA4 are all voltage amplifiers with low gain, as shown in Fig. 2.b, c. Among them, VA2 and VA4 have gain programmable functions, which are realized by current attenuation mirrors containing 3-bits resistor strings, as shown in Fig. 2.c. The DC offsets at the inputs of VA1~VA4 need to be minimized, otherwise the Opamp will become unstable under high gain situations. To minimize the DC offsets, replica biases for Vn_bias and Vp_bias are applied, which are shown in Fig. 2.d, e. Two 400fF load capacitors Cload are used for both load and frequency compensation. Another four capacitors (should below 400fF/2, which are not shown in Fig.2) could be added at the locations X, W, Y and Z to enlarger the phase margin. All transistors have a gate length of 130nm.The power supply use 1.2V.

B. Embedded Gain Monitor

The embedded gain monitor configuration is shown in Fig. 3. It uses a digitally controllable voltage attenuator together with the Opamp to form a positive feedback system. By controlling the 4-bits voltage attenuator, one can control the positive feedback loop gain [5]. In the case the loop gain is larger than 1, the whole system becomes unstable and will enter the bifurcation state [5]. By checking whether the system enters this bifurcation state, it can be determined whether the loop gain is larger or smaller than 1. Since the gain of the attenuator is already known in advance, the Opamp gain can be detected. The digital logic part in Fig.3 is designed to provide the diagnosis and controllability at system level [2]. It can also be configured to operate as a self-calibrating Opamp if required.

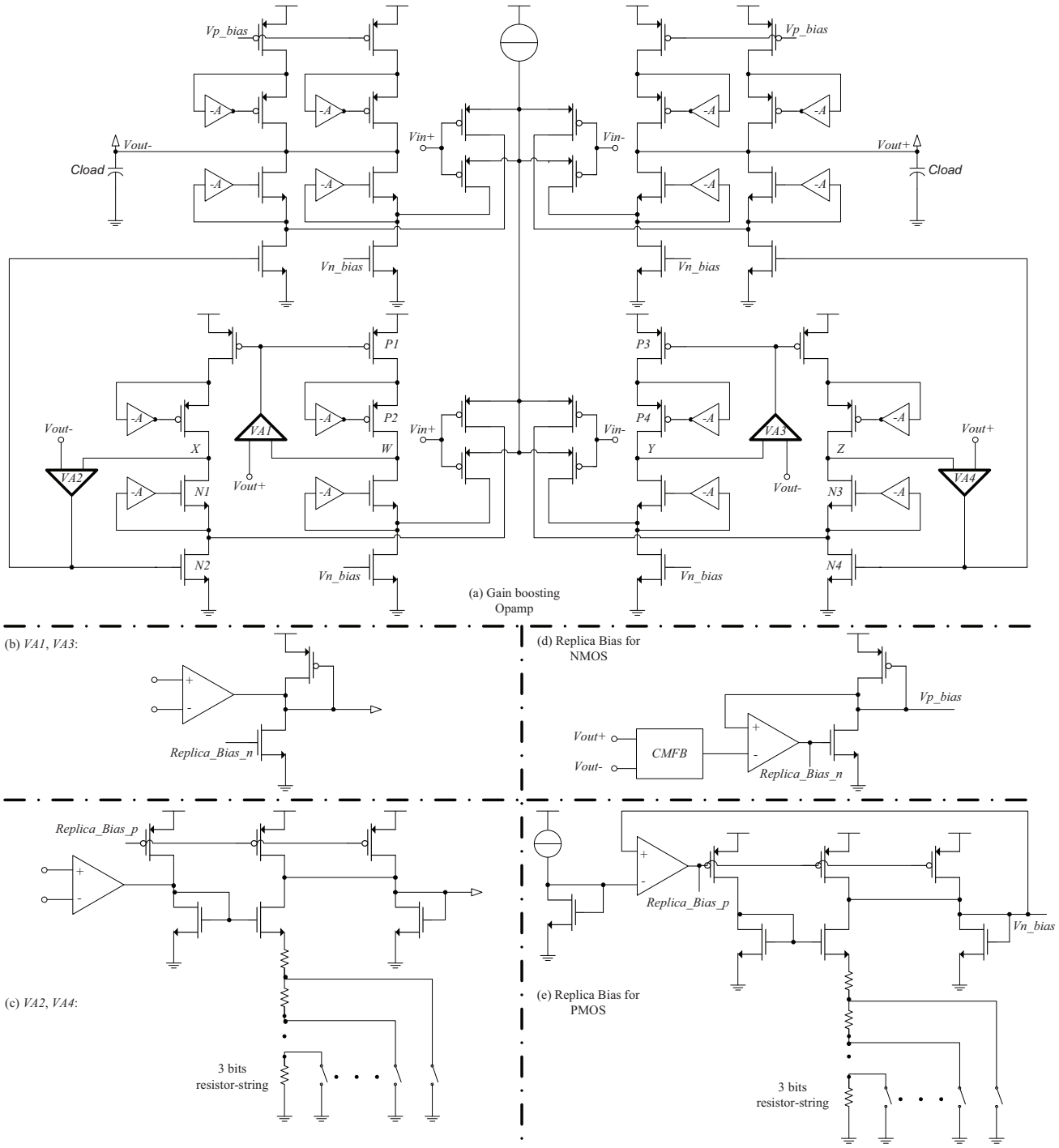

Figure 2. Gain boosting programmable Opamp. a) Gain boosting Opamp. b) Gm1, Gm3. c) Gm2, Gm4. d) Replica bias for NMOS. e) Replica bias for PMOS

Two potential problems have to be solved for this gain monitor in order to measure the open loop gain of the Opamp. The first one is the DC offset. Since the Opamp DC gain can be more than 90 dB, the input DC offset is preferred to be smaller than 10µV to avoid saturation. Fortunately, this gain monitor has the capability to detect DC offset too [5], where a 16-bits DAC is used for offset compensation. In our design, a 12-bits offset compensation current source has been designed, which is able to compensate the offset below 40mV with a 9µV minimum step. The second problem is the noise. The preferred input noise amplitude should also be smaller than 10µV. In this design, the last stage in the attenuator is designed to have the largest voltage attenuation ratio, which minimizes the Opamp input noise amplitude. The accuracy of the monitor has been found to be within 6dB by means of simulation.

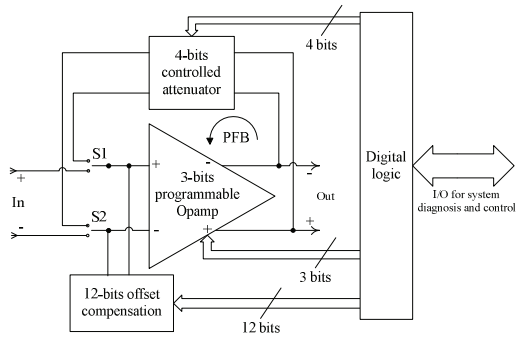

Figure 3. The embedded gain monitor and offset compensation configuration

IV. DEPENDABILITY SIMULATIONS

The 3-bits programmable Opamp (fresh without aging) gain and phase shift simulations are shown in Fig. 4. The other performance parameters are shown in Table I. The Opamp has also been simulated under all process corners and temperature range from -40℃ to 200℃(enhanced automotive). The results show that the range of the gain is between 50dB and 150dB and that the Opamp is always stable.

The dominating aging effect in 65nm is NBTI. By using the Cadence RelXpert with Agemos models, the NBTI effects on circuit have been examined. In our paper, the NBTI parameters are only for threshold voltage aging, not for mobility aging .

Three situations have been simulated with RelXpert and Spectre. All situations followed the same procedure: first simulate the fresh circuit performance at 27℃ using Spectre, and then start aging at 200℃ for 20 years by RelXpert. Finally simulate the aged circuit performance at 27℃ with Spectre again. In the first case, a 1mV@1MHz differential input signal with 0.2V common mode was applied to the input of the Opamp, which evaluates the normal operational situation. In the second case, a 0.6V@1MHz differential input signal with 0.6V common mode (rail-to-rail input) was used as the input, which evaluates the overdrive situation. In the third case, a DC input with one 1.2V and the other 0V was applied, which represents an extreme aging situation. The NBTI aging simulation results are shown in Table II. These dependability parameters of the Opamp IP can be used at system level to make optimal choices for a SoC with regard to dependability [2].

As can be seen from Table II, for the fully differential Opamp used in the aging simulations, the gain is insensitive to NBTI aging under normal operation and rail-to-rail input cases. Since both the circuit and the input are symmetric, the threshold voltage shifts resulting from aging are also symmetric. Hence

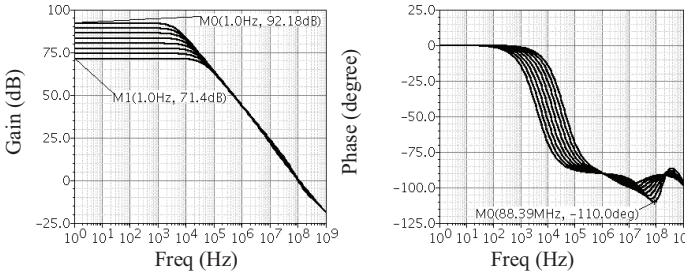

Figure 4. The gain and phase behaviour of the 3-bits programmable Opamp

TABLE I. PERFORMANCE CHARACTERISTICS OF OPAMP

Circuits	Gain range (dB)	Phase Margin (degree)	Area approx.* (μm^2)	Current consump. (uA)	Unit gain freq. (Hz)
Opamp	71~92	Min. 70	500	1200	100M
Monitor	65~101	N.A.	600	800	N.A.

*: The area values are approximate ones since no layout was made.

TABLE II. DEPENDABILITY CHARACTERISTICS OF OPAMP

NBTI Reliability				Maintain-ability	Non-availability
Fresh	*Case 1*	*Case 2*	*Case 3*	(repair range)	(repair time)
83dB	82dB	80dB	25dB	Offset: 40mV Gain: ±10dB	32ms

the gain is hardly influenced by the aging (if no statistics).

However in the extreme aging case, the gain reduces from 83dB to 25dB. This reduction is due to the Opamp entering the saturation region. The unsymmetrical operational condition of the two branches in the fully differential Opamp makes the aging also unsymmetrical. In theory, it causes a differential offset at the Opamp input. This offset caused by aging saturated the Opamp. The gain monitor can detect the offset caused by aging and adds around 3.9mV compensation to the input. After the offset compensation, the gain is recovered to 82dB.

The NBTI effect also degrades the transconductance of the PMOS, which was not yet be modeled in our aging simulations. So in real world, the Opamp gain could still be lower than the fresh one even after offset compensation. That part of reduced gain could be detected by the gain monitor and also be recovered by the gain programmable function.

V. CONCLUSIONS

A new gain boosting method has been described. Based on the method, a single stage 92dB programmable Opamp has been designed in 65nm. This digitally programmable Opamp, together with a digital gain monitor, have been used to construct a highly dependable Opamp IP. The NBTI effect has been verified by Cadence RelXpert and finally the dependability properties of the IP have been provided to be used at SoC level.

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