Low Power Near-sensor Coarse to Fine XOR based Memristive Edge Detection

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***Abstract*—In this paper, we propose XOR based memristive edge detector circuit that is integrated into a near sensor log-linear CMOS pixel. Memristor threshold logic was used to design NAND gates, which serve as a building block for XOR gates. For validation of proposed circuit functionality hardware simulation of logic gates with a pixel pair was conducted using TSMC 0.18um technology and system-level simulation of the proposed circuit using SPICE models. The proposed method operates in low power and takes a small area on chip. The power consumption of one pixel is 1.16uW and total area 36.72 um^2 without photosensing component. The power consumption of NAND circuit is 1.11pW and total area 32.4um^2.**

I. Introduction

In this work, we propose analog circuit implementation of near-sensor edge detection which provides faster computation without the need for analog-to-digital conversion. The core of the edge detection engine is based on XOR operation that was described in [1]. The proposed neuromorphic analog design presents novel use of memristive threshold logic gates for image processing. In the following section, the proposed architecture of the circuit that consists of image sensing circuit and memristive XOR logic gates are presented. Further, the simulation results of these components are discussed, comparing to the competing approaches of edge detection operation.

II. Proposed architecture

A. Active pixel sensor circuit

Depending on configuration, CMOS active pixel sensors (APS) is capable of yielding either linear or logarithmic output characteristics. Standard 3T linear APS has good sensitivity at low light illumination with DR about 80dB. While logarithmic 3T APS show better performance at high illumination with wider DR about 100dB. One of the approaches to extend pixel dynamic range is to combine log-linear response.

Fig.1 shows a wide dynamic range 5T active pixel with log-linear output characteristic proposed by [2]. n-type MOSFET transistors N_1 and N_2 in the circuit are used to convert generated photodiode current into voltage producing logarithmic or linear responses respectively. PMOS transistor P_1 serves as a switch to control the operation mode depending on illumination intensity. At low illumination conditions pixel operates as linear APS, whereas with high light intensity it produces logarithmic output. The resulting voltage at floating diffusion node V_{fd} is amplified by source follower N_3 and N_4 and read by transistor N_5.

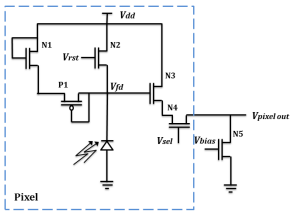


Fig. 1. Schematic of the log-linear pixel circuit

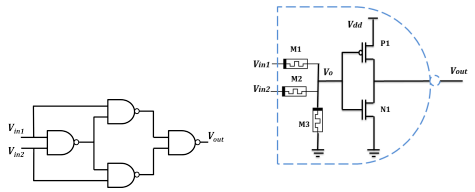
B. Memristive XOR gate

XOR logic can be implemented using NAND gates as in Fig 2a. In [3], authors proposed a configuration of resistive memory threshold logic gate cell circuit as in Fig. 2b, that can be adjusted to operate as NAND or NOR gates. The gate was set up in the voltage divider configuration followed by a CMOS inverter. In this circuit memristors are used instead of resistors due to its small size and low leakage current. The mode of logic gate depends on the input of the third M_3 memristor: If the input is grounded then it is NAND, while driving it to High Voltage sets the mode to NOR. But the same NAND mode of the gate can also be used as NOR gate if the threshold of inverter will be adjusted to specific level. In Table I the analog output V_o of the resistive divider component of the gate are shown. To set the gate to NAND mode it is required to set the threshold of the inverter $V_{low} + (V_{high} - V_{low})/2$, while for NOR it is sufficient to set it $V_{low} + (V_{high} - V_{low})/4$.

TABLE I
Analog output V_o of Memristive Logic gate

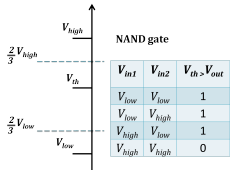
V_{in1}	V_{in2}	V_{out}
V_{low}	V_{low}	$2V_{low}/3$
V_{low}	V_{high}	$(V_{low}+V_{high})/3$
V_{high}	V_{low}	$(V_{high}+V_{low})/3$
V_{high}	V_{high}	$2V_{high}/3$

Fig. 2b shows the NAND logic gate. To operate in NAND mode memristors are set to the same values R_1=R_2=R_3=R and the inverter is utiilized to convert V_o to binary state V_{out} as in Fig 3.



(a) (b)

Fig. 2. Building (a) XOR Logic gate using (b) memristive NAND gates



V_{in1}	V_{in2}	$V_{th}>V_{out}$
V_{low}	V_{low}	1
V_{low}	V_{high}	1
V_{high}	V_{low}	1
V_{high}	V_{high}	0

Fig. 3. Setting the threshold value for NAND operation

III. Results and Discussion

A. Hardware simulation

Fig. 4 shows output voltage variation of the CMOS pixel for photocurrent between 2.5fA to 250nA. Corresponding generated voltage range varies from 50mV to 650mV. DR of the given pixel is of the order of 140dB and utilization of five transistors allows to keep high fill factor.

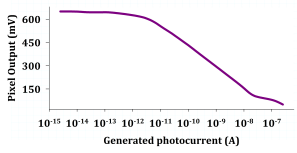


Fig. 4. 5T Pixel sensor output

The output response of memristive XOR circuit for the two pixels outputs is shown in the Fig.5 which demonstrates functionality of XOR gate for analog input values.

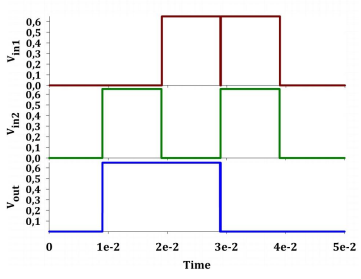


Fig. 5. Output response of XOR circuit

Simulations were performed in SPICE using 0.18 μm TSMC CMOS technology model and HP memristor model [4]. The power consumption of one pixel is 1.16μW and total area 36.72 μm^2 without photosensing component. The power consumption of NAND circuit is 1.11pW and total area 32.4 μm^2.

TABLE II
COMPARISON OF QUALITATIVE MEASURES OF EDGE DETECTION OPERATORS AT DIFFERENT NOISE CONDITIONS

Measure	XOR		Canny		Sobel	
	Noise type					
	Speckle	Salt and Pepper	Speckle	Salt and Pepper	Speckle	Salt and Pepper
PSNR	17.2840	25.4213	18.2223	24.1921	15.9374	15.8522
MSE	0.0187	0.0029	0.0151	0.0038	0.0255	0.0260

(a) (b) (c) (d) (e) (f)

Fig. 6. Original image (a); binarized images with a shift of 15 pixels (b) and 3 pixels (c) detected edges of original b and c with proposed XOR circuit (d) detected edges of b and c with added $Speckle$ noise (e) detected edges of b and c with added *Salt and Pepper* noise (f)

To demonstrate the functionality of memristive XOR circuit for edge detection operation the system simulation was performed in MATLAB. In Table II the comparison of qualitative measures for memristive XOR circuit and conventional edge detection operators are given. As it can be seen, near-sensor hardware edge detection circuit based on XOR operation demonstrates competitive results compared to Canny and Sobel operators, outperforming both of the approaches in edge detection of images with *Salt and Pepper* type of noise. Figs.6 (a-g) illustrate performance of XOR circuit for edge detection task with different noise types.

IV. Conclusion

In this paper, XOR-based edge detecting circuit design is proposed. The edge detection was performed with CMOS active pixel sensor array with log-linear response followed by XOR memristive circuits that were constructed from memristive NAND threshold logic gates. Presented approach provides near-sensor decision making which enables fast computation at low power cost and small on-chip area due to use of hybrid CMOS-memristor devices. Comparison of experimental results show that presented circuit design provides competitive performance compared to conventional operators. Although XOR operation stands behind some of the conventional edge detecting filters, its straightforward implementation on hardware and usability for data processing in analog domain make it more attractive compared to digital filters.

References

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