A Software-based Low-Jitter Servo Clock for Inexpensive Phasor Measurement Units

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Abstract—This paper presents the design and the implementation of a servo-clock (SC) for low-cost Phasor Measurement Units (PMUs). The SC relies on a classic Proportional Integral (PI) controller, which has been properly tuned to minimize the synchronization error due to the local oscillator triggering the on-board timer. The SC has been implemented into a PMU prototype developed within the OpenPMU project using a BeagleBone Black (BBB) board. The distinctive feature of the proposed solution is its ability to track an input Pulse-Per-Second (PPS) reference with good long-term stability and with no need for specific on-board synchronization circuitry. Indeed, the SC implementation relies only on one co-processor for real-time application and requires just an input PPS signal that could be distributed from a single substation clock.

Index Terms—Servo clock, time synchronization, syntonization, Phasor Measurement Units, smart grid.

I. INTRODUCTION

Time synchronization is a crucial part of every distributed measurement system. Synchrophasor measurement in transmission and distribution systems is a well-known application field in which time synchronization plays a key role, e.g. for power system state estimation [1], topology detection [2] or loss-of-mains protection [3]. Phasor Measurement Units (PMU) are complex instruments, requiring usually high-end hardware that perform timestamped measurements of voltage and current amplitude, phase, frequency and rate of change of frequency (ROCOF) synchronized to the Coordinated Universal Time (UTC). From a functional point of view, PMUs can be decomposed into component parts: an acquisition subsystem, a synchronization module, and finally a digital signal processing subsystem. Several scientific contributions about the impact of PMU synchronization uncertainty in power systems have already been proposed in the literature [4]. For instance, analytical methods for mitigating the effect of time synchronization on the grid state estimation are presented in [5], [6]. Some insight from a real network can be found in the work by Della Giustina et al. [7], who analyze the timing requirements for power quality measurements. The IEEE Standard C37.242-2013 on PMU synchronization, calibration, testing, and installation highlights that the main contributors to estimation uncertainty can be identified in (i) synchronization issues, (ii) noise and distortion in the input channel and acquisition circuitry, (iii) intrinsic accuracy limits of the adopted digital signal processing algorithm and, finally, (iv) possible communication problems [8]. In general, no information on the weight of these contributions on overall PMU accuracy is available. The IEEE Standard C37.118.1-2011 and its Amendment IEEE C37.118.1a-2014 express the overall synchrophasor measurement accuracy with a single parameter, namely the Total Vector Error (TVE), which depends on both amplitude and phase estimation uncertainties. While both documents prescribe various TVE boundaries in different testing conditions [9], [10], no specific limits for time synchronization uncertainty or jitter are explicitly reported. Under the overoptimistic assumption that the amplitude measurement uncertainty is negligible, time errors within $\pm 31 \ \mu s$ or $\pm 26 \ \mu s$ for 50 Hz or 60 Hz systems, respectively, are small enough to keep phase estimation accuracy below 10 mrad and, consequently, TVE < 1%, which is the strictest limit reported in [9], [10]. However, since amplitude and phase estimation uncertainties are usually both significant in practice, "a time source that reliably provides time, frequency, and frequency stability at least 10 times better than the values above is highly recommended" [9]. Thus, as a rule of thumb, synchronization accuracy within $\pm 1 \ \mu s$ is currently considered to be adequate in most power systems applications, as the corresponding maximum phase errors (in the order ± 0.4 mrad) are usually much smaller than those due to other uncertainty contributions. However, the evolution of smart active distribution grids as well as the emerging need to measure phasor angle differences smaller than 1 mrad (e.g. over short lines) could demand more accurate synchrophasor measurements than those possible nowadays [11]-[13]. As a result, tighter synchronization accuracy might be needed in the future. It is worth emphasizing that PMUs require not only synchronization (i.e. time offset compensation with respect to UTC) to properly timestamp measurement data, but also syntonization (i.e. clock rate adjustment) to enable coherent sampling of voltage or current waveforms in ideal conditions. Commercial PMUs generally include specific hardware modules for time synchronization, most notably GPS receivers or IRIG-B (Inter-Range Instrumentation Group time codes) decoders, which are supposed to be used to discipline the sampling clock as well, e.g. through some hardware Phase Lock Loop (PLL) or other more sophisticated custom techniques. For instance, in [14] Yao et al. describe a way to compensate for the sampling time errors caused by the division remainder between the desirable sampling rate and the oscillator frequency. An alternative approach to achieve both synchronization and syntonization is through Servo Clocks (SC), e.g. based on Proportional Integral (PI) controllers [15], [16]. The most common examples of SCs are those developed for Ordinary and Boundary Clocks of IEEE 1588 devices [17]-[19]. In general, there are just a few comprehensive analyses of SCs. One of them, is provided by Chen et al. [20] who propose an optimized SC for distributed motion control systems based on EtherCAT. However, the design and implementation of SCs for PMUs is a topic seldom covered in the scientific literature. Even the recently released IEEE Standard C37.238-2017 dealing with a profile of the IEEE 1588 Precision Time Protocol (PTP) for power systems application does not report any indication about SC design [21]. This research work is part of the 'OpenPMU' project¹, an international project whose purpose is to develop a fully open-source PMU for power system analysis and research [22]. In particular, this paper deals with a SC for the 'OpenPMU' platform described in [23]. The SC has been designed and optimized to minimize the synchronization errors due to the local crystal oscillator (XO) and generates the signal to sample the input waveform as well. The main advantage of the proposed solution is that the SC relies only on a Programmable Real-Time Unit (PRU) available in the embedded platform, with no need for specific synchronization hardware except for an external Pulse Per Second (PPS) reference signal, which could be provided by a common GPS receiver (or substation clock) and shared among multiple PMUs. The rest of the paper is structured as follows. First, in Section II, the resources available to implement the SC for the 'OpenPMU' platform are described in brief. Then, in Section III, a mathematical model of the SC is defined and the related design criteria are explained. Finally, in Section IV the results of various experiments showing SC performance are reported. Section V concludes the paper and outlines future work.

II. SERVO CLOCK ARCHITECTURE

Unlike typical PMU implementations, the acquisition stage of the 'OpenPMU' platform described in [23] is fairly simple and relies on a Beaglebone Black (BBB) board. This is a low-cost commercial embedded system, which has been recently used in a variety of projects, including I/O signal synchronization [24] and PMU algorithm prototyping [25]. A distinctive feature of the BBB is its Sitara AM3358 microprocessor, that include a 1-GHz ARM Cortex-A8 microprocessors, called Programmable Real-time Units (PRU). The PRUs can be used to perform specific real-time tasks, since they can be programmed at a low-level, i.e. without using any operating system. The PRUs are provided with a rich set of peripherals (including timers), besides direct access to General-Purpose Input-Output (GPIO) pins. On the other hand,

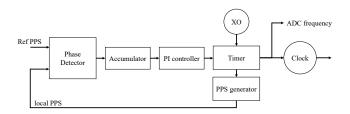


Fig. 1. Architecture of the SC implemented on the PRU of the BBB.

the PRU computational capabilities are limited: no Floating-Point Unit is present, local memory is guite small (only 8 KB plus a 12 KB of shared DRAM) and asynchronous interrupt handling is not possible. Despite such limitations, the basic idea of the solution proposed in this paper is to use one of the PRUs to fully implement a SC running in parallel to the main ARM core in order to synchronize and syntonize the data acquisition system described in [23]. The architecture of the proposed SC is shown in Fig. 1. A purely software indirect frequency synthesizer is used to generate the 12.8-kHz signal clocking the Analog-to-Digital Converter (ADC) of the acquisition stage. Since a real 12.8-kHz Voltage-Controlled Oscillator (VCO) is not available on the BBB, this is emulated by means of one of the timers of the PRU, clocked at 200 MHz and configured to be reloaded automatically. While the nominal timeout to be loaded into the timer is 15625 ticks, its actual value changes as a function of the corrective action performed by the internal controller. The 12.8 kHz signal is used to increment both the system clock (which is implemented as a software counter properly initialized with a UTC timestamp as soon as it is available) and a second counter (labeled as PPS generator in Fig. 1) that generates a PPS signal. The difference in time (measured with a resolution of 5 ns) between the external (i.e. reference) PPS signal and the local one is integrated by a digital accumulator in order to compute the time error, which finally drives a Proportional-Integral (PI) controller adjusting the clock rate, as customary in SC design. The equivalence between the system considered and a classic SC is demonstrated in Section III.

III. MODEL DESCRIPTION AND PI CONTROLLER DESIGN

The SC shown in Fig. 1 can be modeled as a discrete-time linear system discretized at 1 Hz, as shown in in Fig. 2(a). Let $\tau_m(k)$ and $\tau_c(k)$ be the periods of the PPS signals at the input and at the output of the SC, respectively, at the k-th sampling second. Since both signals are affected by phase and frequency noises and by a relative frequency offset, the time synchronization error e(k) between them is simply given by:

$$e(k+1) = e(k) + \tau_m(k) - \tau_c(k), \tag{1}$$

Therefore, the equivalent model depicted in Fig. 2(a) can be easily reduced to the classic SC model shown in Fig. 2(b), where symbols t_m and t_c denote the reference time and the time measured by the SC, respectively. Based on this

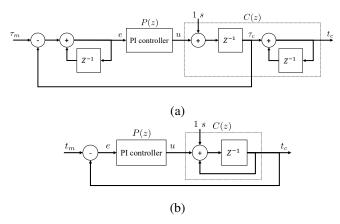


Fig. 2. Equivalent models of the implemented SC before (a) and after (b) reduction.

simplified model, the SC in the z-domain basically consists of two subsystems, i.e. the clock itself, whose transfer function is

$$C(z) = \frac{1}{z-1},\tag{2}$$

and the PI controller, which can be obtained from the classic backward Euler integration method, i.e.

$$P(z) = K_P + K_I \frac{z}{z-1},$$
 (3)

where K_P and K_I are the proportional and integral gains, respectively. Of course, SC stability depends on the position of the poles of the closed-loop transfer function

$$H(z) = \frac{P(z)C(z)}{1 + P(z)C(z)} = \frac{(z-1)K_P + zK_I}{(z-1)^2 + (z-1)K_P + zK_I}.$$
 (4)

Moreover, coefficients K_P and K_I in (3) should be tuned in order to meet given performance requirements, in terms of convergence time or output uncertainty. To this end, (2), (3) and (4) can be expressed using difference equations. Nevertheless, the control design formulation is slightly complicated by the fact that i) the resolution of the SC is $1/f_{XO}$ (with $f_{XO} = 200$ MHz), and ii) the nominal frequency of the emulated VCO is $f_0 = 12.8$ kHz. Therefore, all time quantities (as well as the controller output) have to be expressed in ticks of an ideal 200 MHz oscillator rather than in seconds. Thus, if $n_t = f_{XO}/f_0$ denotes the number of ticks in one nominal period, then the dynamic of the frequency of the disciplined emulated VCO is given by

$$f_c(k+1) = f_0(1+\alpha) + b\eta(k) + bu(k),$$

where $b = 1/n_t$, α is the relative frequency offset of the SC local oscillator with respect to the input reference signal when the SC is in open loop, $\eta(k)$ represents the jitter of the SC accumulated during one second and, finally, u(k) is the control action.

For what concerns the error, it follows immediately from (1) that

$$e_q(k+1) = e_q(k) + \tau_{m_q}(k) - \tau_{c_q}(k),$$

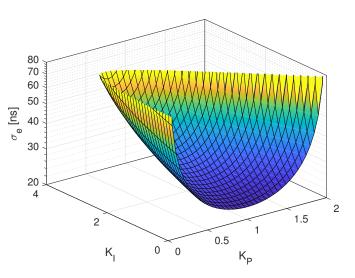


Fig. 3. Standard deviation of the synchronization errors given by the square root of (6), as a function of the values of gains K_P and K_I in the stability region of the SC.

where $e_q(k)$ is the time error e(k) expressed in ticks,

$$\tau_{m_a}(k) = n_t f_0 + \nu(k),$$

is the period of the PPS reference input signal expressed in ticks, $\nu(k)$ is the jitter of the input PPS signal and

$$\tau_{c_a}(k) = n_t f_c(k),$$

is the period of the PPS output of the SC, again expressed in ticks. The control action dynamics is instead given by

$$u(k+1) = u(k) + K_P(e_q(k+1) - e_q(k)) + K_I e_q(k+1).$$

If vector $q(k) = [e_q(k), f_c(k), u(k)]^T$ (with $q(0) = [0, f_0, 0]^T$) denotes the aggregated state of the system in

 $[0, f_0, 0]^T$) denotes the aggregated state of the system in closed loop, the previous equations we can be rewritten more compactly as

$$q(k+1) = Aq(k) + G\tau_{m_q}(k) + C\eta(k) + Ff_0,$$

where

$$A = \begin{bmatrix} 1 & -n_t & 0\\ bK_I & -(K_P + K_I) & b\\ K_I & -n_t(K_P + K_I) & 1 \end{bmatrix}, \quad G = \begin{bmatrix} 1\\ b(K_P + K_I)\\ K_P + K_I \end{bmatrix},$$
$$C = \begin{bmatrix} 0\\ b\\ 0 \end{bmatrix} \text{ and } F = \begin{bmatrix} 0\\ (1+\alpha)\\ 0 \end{bmatrix}.$$

Since q(k+1) is a random vector, its mean value is given by

$$E\{q(k+1)\} = AE\{q(k)\} + GE\{\tau_{m_q}(k)\} + Ff_0,$$

where $E\{\cdot\}$ denotes the expectation operator. To compute the uncertainty of q(k+1) generated by the joint effect of $\nu(k)$ and $\eta(k)$, to a first approximation, we assume that: $\nu(k) \sim \mathcal{N}(0, \sigma_{\nu}^2), \eta(k) \sim \mathcal{N}(0, \sigma_{\eta}^2)$. As a result, the covariance matrix of q(k+1) is given by

$$Q(k+1) = AQ(k)A^{T} + GG^{T}\sigma_{\nu}^{2} + CC^{T}\sigma_{\eta}^{2}.$$
 (5)

Of course, if $\nu(k)$ and $\eta(k)$ are not white or normally distributed, (5) holds just approximately. Notice that, by setting Q(0), (5) can be used to compute the uncertainty of the state vector in closed form.

If the controller gains are set so as to make (4) stable, (5) reaches a steady-state equilibrium, i.e., there exists a sufficiently large value \bar{k} such that Q(k + 1) = Q(k), $\forall k > \bar{k}$. Moreover, the steady-state variance of the time error with respect to the reference is equivalent to the entry (1,1) of Q(k). As a consequence, by computing the equilibrium of (5), it follows that the synchronization error variance is

$$\sigma_e^2 = \mathbf{E}\left\{ (e(k) - \mathbf{E}\left\{ e(k) \right\})^2 \right\} = \frac{2(\sigma_\nu^2 + \sigma_\eta^2)}{K_P(4 - K_I - 2K_P)}.$$
 (6)

Since $K_P > 0$, $K_I \ge 0$ and $\sigma_e^2 > 0$, it follows that the SC is stable for $0 < K_P < 2$ and $K_I < 4 - 2K_P$. Within this region, (6) is minimized once the denominator is maximized. Therefore, the values of K_P and K_I minimizing the variance of the synchronization error can be determined from Fig. 3, which shows the behavior of σ_e as a function of K_P and K_I for values of σ_{ν} and σ_{η} consistent with those of the system at hand and reported in Section IV. However, it is worth emphasizing that trend and position of the minimum do not depend on the variances of ν and η .

From this analysis it follows that if a prompt response is required, a dead-beat controller, with $K_P = K_I = 1$, works well. Otherwise, if the uncertainty has to be minimized, $K_P = 1$ and $K_I = \varepsilon > 0$ is the right choice, with ε being a sufficiently small constant. However, the smaller K_I , the longer the convergence time becomes.

IV. EXPERIMENTAL RESULTS

Based on the previous analysis, the SC behavior was tested for different values of K_P and K_I . The instrument used as a reference was a GPS-disciplined Meinberg M600 master clock. The overall phase noise of the generated PPS signal (estimated on the basis of the power spectral density reported in instrument's specifications) is about 30 ns. However, it is about one order of magnitude smaller over time intervals of a few hours, i.e. till when the effect of flicker phase noise, white frequency noise, flicker frequency noise and random walk frequency noise are negligible. In such conditions, the phase noise is mainly white, in accordance with the theoretical model described in Section III. The period fluctuations of the PPS signal generated by the SC in open-loop conditions (namely when no control action is applied) were measured by an Agilent DSO7032A with a 2-GHz sampling clock disciplined by the master clock. The systematic relative frequency offset of the emulated free-running DCO is about -82 ppm. The standard deviation σ_{η} of the corresponding phase noise in open-loop conditions instead ranges from about 25 ns over one hour (when the phase noise is still dominated by white contributions) till about 120 ns over two days (i.e. when the effect of the other low-frequency power-law noises becomes significant). Given that, as explained in Section III, the models adopted for the SC design rely on the inherent assumption

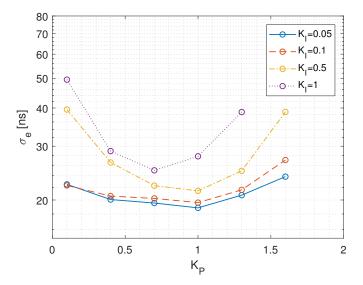


Fig. 4. Experimental values of the standard deviation of the synchronization errors for different settings of K_P and K_I .

that phase contributions are mainly white, $\sigma_{\eta} = 25$ ns was also used to simulate the behavior of the SC in closed loop for different values of K_P and K_I . The resulting standard deviation values σ_e are basically the same as those obtained from the square root of (6) and shown in Fig. 3.

The results of the theoretical analysis were also validated experimentally by estimating σ_e in steady-state conditions over 1-hour intervals for various pairs of K_P and K_I values within the SC stability region (i.e. with $K_I = \{0.05, 0.1, 0.5, 1\}$ and K_P ranging from 0.1 and 1.6). The corresponding standard deviation values are shown in Fig. 4. The experimental curves clearly confirm that σ_e exhibits a minimum value when $K_P =$ 1 and $K_I = \varepsilon > 0$. However, for $K_I < 0.05$ jitter reduction becomes negligible. Observe that even if experimental and theoretical results are generally quite consistent, significant deviations can be observed when both K_P and K_I tend to zero. The ultimate reason for this mismatch is not clear, but it is certainly related to some second-order difference between SC model and SC implementation. Nonetheless, it is worth noticing that the experimental results are smaller than those based on the theoretical analysis, which can be regarded as a conservative design policy in this respect.

The long-term stability of the SC with respect to the chosen reference PPS signal was determined by measuring the difference in time (over about two days) between the rising edges of the PPS signals at the input and at the output of the SC, respectively, for some of the K_P and K_I values considered in the design stage, i.e.

- 1) Using a dead-beat controller (i.e. $K_P = K_I = 1$) that is chosen for its fast response, albeit the jitter reduction with this controller is not the best;
- 2) Using a purely proportional controlled with unit gain (i.e. $K_P = 1$ and $K_I = 0$);
- 3) And, finally, with $K_P = 1$ and $K_I = 0.05$ for the reasons explained above.

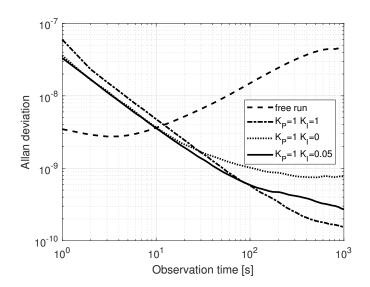
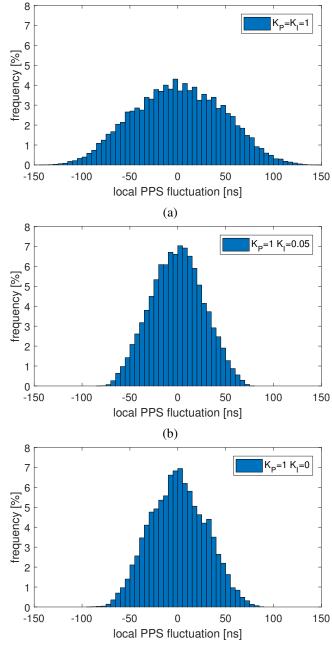


Fig. 5. Allan deviation curves of PPS signals generated by the SC running on the BBB for different values of the PI controller parameters K_P and K_I . For the sake of comparison, also the Allan deviation of the PPS signal generated in open-loop conditions is shown.

The Allan deviation values of the waveforms generated by the SC are shown in Fig. 5 for different observation intervals. The open-loop (i.e. free-running) case is also shown for the sake of comparison. It is worth noticing that the short-term stability of the PPS in open-loop conditions over 1 s is approximately $3.4 \cdot 10^{-9}$, but it tends to degrade over longer intervals, as customary of low-quality crystal oscillators. Of course, in closed-loop conditions, the systematic relative frequency offset with respect to the input reference signal is well adjusted by the PI controller. Therefore, if the input reference oscillator is particularly accurate, the systematic relative frequency offset of the SC can be reduced to less than 0.1 ppm. Observe that the short-term SC stability is clearly worse than in openloop conditions, particularly when the dead-beat controller is used. However, in the long term, stability with respect to the input reference drastically improves as a result of the control action. Some test were performed also using different input PPS signal, i.e. the PPS from a u-blox NEO-6M. Such device produce a poorer quality PPS signal, hence in the long-term the performance is worse. Nevertheless it was possible to confirm the design choices discussed so far. On the whole, the configuration based on the criterion described in Section III provides a very good trade-off between short-term and longterm stability.

In order to complete the analysis, Fig. 6(a)-(c) shows the histograms of the PPS period fluctuations with respect to the Meinberg M600 clock using (a) the dead-beat controller; (b) the quasi-optimal controller with $K_P = 1$ and $K_I = 0.05$ and (c) a purely proportional controller ($K_P = 1$ and $K_I = 0$). Observe that in the second case, the jitter is almost halved (i.e. 25 ns vs. 50 ns). The jitter associated wit the proportional only controller is instead just slightly worse than the optimal one, whereas in theory it should be much larger. Such a



(c)

Fig. 6. PPS period fluctuations of the signal generated by the SC with respect to the Meinberg M600 using (a) a dead-beat controller ($K_P = 1$ and $K_I = 1$), (b) a quasi-optimal controller for time uncertainty minimization ($K_P = 1$ and $K_I = 0.05$) and (c) a proportional-only controller.

difference is due to the mismatch between theoretical model and SC implementation explained before. In any case, the proportional-only controller is not able to correct possible sudden time offsets perfectly.

V. CONCLUSION

This paper describes the design criteria of a Servo Clock (SC) implemented on a single-board computer to discipline the data acquisition stage of a low-cost Phasor Measurement

Unit (PMU). The SC has been developed in the context of the 'OpenPMU' project. The SC implementation relies on a BeagleBone Black (BBB) embedded platform. In particular, the SC runs mainly in one of the Programmable Real-time Units (PRUs) of the BBB microprocessor, with no need for additional hardware. The PPS input reference signal could be provided by a common master clock shared among multiple PMUs within the same substation. The experimental results are quite consistent with the theoretical ones and highlight the correct operation of the SC based on a PI controller correcting possible frequency offsets between the local oscillator of the BBB and the input reference. The controller has been optimized in order to minimize the standard deviation of the short-term synchronization error. In the future, other and more sophisticated (e.g. adaptive) techniques will be adopted to further optimize the controller parameters on-line, e.g. to handle changes in environmental or processing load conditions.

REFERENCES

- [1] J. D. L. Ree, V. Centeno, J. S. Thorp, and A. G. Phadke, "Synchronized phasor measurement applications in power systems," *IEEE Transactions* on Smart Grid, vol. 1, no. 1, pp. 20–27, Jun. 2010.
- [2] G. Cavraro, R. Arghandeh, G. Barchi, and A. von Meier, "Distribution network topology detection with time-series measurements," in 2015 IEEE Power Energy Society Innovative Smart Grid Technologies Conference (ISGT), Washington, DC, USA, Feb. 2015, pp. 1–5.
- [3] D. M. Laverty, "Loss-of-mains protection system by application of phasor measurement unit technology with experimentally assessed threshold settings," *IET Generation, Transmission & Distribution*, vol. 9, pp. 146– 153, Jan. 2015.
- [4] J. A. Bazerque, U. Ribeiro, and J. Costa, "Synchronization of phasor measurement units and its error propagation to state estimators," 2016, pp. 508–513.
- [5] M. Todescato, R. Carli, L. Schenato, and G. Barchi, "PMUs Clock De-Synchronization Compensation for Smart Grid State Estimation," no. Cdc, 2017, pp. 793–798.
- [6] P. Yang, Z. Tan, A. Wiesel, and A. Nehorai, "Power system state estimation using PMUs with imperfect synchronization," *IEEE Transactions* on Power Systems, vol. 28, no. 4, pp. 4162–4172, 2013.
- [7] D. D. Giustina, P. Ferrari, A. Flammini, and S. Rinaldi, "Synchronization requirements of a Power Quality measurement system for the distribution grid," 2014, pp. 245–250.
- [8] "IEEE guide for synchronization, calibration, testing, and installation of phasor measurement units (pmus) for power system protection and control," *IEEE Std C37.242-2013*, pp. 1–107, Mar. 2013.
- [9] "IEEE standard for synchrophasor measurements for power systems," 2011.
- [10] "IEEE standard for synchrophasor measurements for power systems – amendment 1: Modification of selected performance requirements," *IEEE Std C37.118.1a-2014 (Amendment to IEEE Std C37.118.1-2011)*, pp. 1–25, Apr. 2014.
- [11] A. Borghetti, C. A. Nucci, M. Paolone, G. Ciappi, and A. Solari, "Synchronized phasors monitoring during the islanding maneuver of an active distribution network," *IEEE Transactions on Smart Grid*, vol. 2, no. 1, pp. 82–91, Mar. 2011.
- [12] M. H. F. Wen, R. Arghandeh, A. von Meier, K. Poolla, and V. O. K. Li, "Phase identification in distribution networks with microsynchrophasors," in *Proc. IEEE Power Energy Society General Meeting*, Denver, CO, USA, Jul. 2015, pp. 1–5.
- [13] G. Barchi, D. Fontanelli, D. Macii, and D. Petri, "On the accuracy of phasor angle measurements in power networks," *IEEE Transactions on Instrumentation and Measurement*, vol. 64, no. 5, pp. 1129–1139, 2015.
- [14] W. Yao, L. Zhan, Y. Liu, M. Till, J. Zhao, L. Wu, Z. Teng, and Y. Liu, "A Novel Method for Phasor Measurement Unit Sampling Time Error Compensation," *IEEE Transactions on Smart Grid*, vol. 9, no. 2, pp. 1063–1072, 2018.
- [15] R. Exel and F. Ring, "Improved clock synchronization accuracy through optimized servo parametrization," 2013, pp. 65–70.

- [16] J. C. Eidson, "An overview of clock synchronization using ieee 1588," in *Measurement, Control, and Communication Using IEEE* 1588. Springer, Jan. 2006. [Online]. Available: http://dx.doi.org/10. 1007/1-84628-251-9{_}3
- [17] K. Correll, N. Barendt, and M. Branicky, "Design considerations for software only implementations of the IEEE 1588 precision time protocol," in *Proc. Conference on IEEE 1588 Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*, Winterthur, Switzerland, Oct 2005.
- [18] A. Machizawa, T. Iwawma, and H. Toriyama, "Software-only implementations of slave clocks with sub-microsecond accuracy," 2008, pp. 17–22.
- [19] B. Ferencz and T. Kovácsházy, "Hardware assisted COTS IEEE 1588 solution for x86 Linux and its performance evaluation," 2013, pp. 47–52.
- [20] X. Chen, D. Li, S. Wang, H. Tang, and C. Liu, "Frequency-Tracking Clock Servo for Time Synchronization in Networked Motion Control Systems," *IEEE Access*, vol. 5, pp. 11606–11614, 2017.
- [21] "IEEE standard profile for use of IEEE 1588 precision time protocol in power system applications," *IEEE Std C37.238-2017 (Revision of IEEE Std C37.238-2011)*, pp. 1–42, June 2017.
- [22] D. M. Laverty, R. J. Best, P. Brogan, I. A. Khatib, L. Vanfretti, and D. J. Morrow, "The OpenPMU platform for open-source phasor measurements," *IEEE Transactions on Instrumentation and Measurement*, vol. 62, no. 4, pp. 701–709, apr 2013.
- [23] X. Zhao, D. M. Laverty, A. McKernan, D. J. Morrow, K. McLaughlin, and S. Sezer, "GPS-disciplined analog-to-digital converter for phasor measurement applications," *IEEE Transactions on Instrumentation and Measurement*, vol. 66, no. 9, pp. 2349–2357, Sep. 2017.
- [24] A. Alanwar, F. M. Anwar, Y. F. Zhang, J. Pearson, J. Hespanha, and M. B. Srivastava, "Cyclops: PRU programming framework for precise timing applications," 2017.
- [25] P. Tosato, D. Macii, M. Luiso, D. Brunelli, D. Gallo, and C. Landi, "A tuned lightweight estimation algorithm for low-cost phasor measurement units," *IEEE Transactions on Instrumentation and Measurement*, vol. 67, no. 5, pp. 1047–1057, may 2018.