# Automated Test Generation and Test Point Selection for Specification Test of Analog Circuits

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# Abstract

In this paper, a new automated test generation and concurrent test point selection algorithm for specification based testing of analog circuits is presented. The proposed approach co-optimizes the construction of a multi-tone sinusoidal test stimulus and the selection of the best set of test response observation points. The circuit specifications are predicted accurately from the test response using a prior algorithm. This prediction is based on a statistical regression based mapping of the test response waveform to the specifications of the circuit under test. The test generation and test point selection process tries to maximize the accuracy of specification prediction using the above mapping. Pass/fail test decisions are made using the predicted specifications. Simulation results show excellent performance of the proposed algorithms.

Index terms: specification testing, automated test generation, parametric failure, test point selection.

#### 1. Introduction

Failures in analog and mixed signal circuits are broadly classified into two categories [1], viz. catastrophic, where the analog circuit fails to operate correctly due to internal shorts and opens and other manufacturing defects and parametric, where, after IC fabrication, one or more specifications of the circuit deviate from the respective design values due to random variations in the manufacturing process. Different fault-models [3,4] and test approaches [5-8] have been proposed with the objective of detecting catastrophic and parametric failures (DOT [2]). In this paper, a new specification oriented test (SPOT [2]) approach is presented which aims to accurately test the specifications of analog circuits under parametric (multi-parameter) failure conditions.

In the proposed test approach, the circuit is stimulated with DC and large signal multi-tone waveforms under parametric failure conditions (multi-parameter circuit/process perturbations). The test response waveforms at one or more circuit nodes are observed. The circuit specifications are computed using multi-variate nonlinear regression analysis of the test response waveforms [10-12].

The efficiency of the test approach lies in accurate determination of critical parametric failure modes and in concurrent test-point selection and multi-tone test stimulus generation. In this test approach, a set of critical parametric perturbation modes is first computed. AC analyses are carried out in order to compute the observability vectors corresponding to the critical perturbation modes. Then, a fast, greedy algorithm is used to compute the amplitude and delays of the different tones and select the optimal test response observation points by minimizing the specification prediction error in the regression models.

In comparison with the test point selection approach in [8], where the controllability and observability are maximized, in the proposed approach, specification prediction accuracy is maximized. In a similar way, the objective of the test generation approach is different from the other multi-frequency test generation approaches in [5,7,15], where the fault coverage under a parametric fault model is maximized. Hence, the primary objective of the spoosed approach is to maximize the accuracy of the SPOT in terms of test observation point selection and multi-tone test generation.

The paper is organized as follows. Section 2 discusses basic concepts. Section 3 describes the test architecture. In Section 4, the test approach is explained in detail. Simulation results for different analog circuits are presented in Section 5 with conclusions discussed in Section 6.

# 2. Basic Concepts

As shown in the literature [9-12], variation of any process or circuit parameter, such as width of a FET, value of a resistor, etc., in the process or circuit parameter space **P** affects the circuit specification S by a corresponding sensitivity factor. Let M be the space of measurements (voltage and current values) made on the circuit under test. The variation in the parameters also affects the measurement data in the measurement space M of the circuit by a corresponding sensitivity factor. Figure 1 illustrates the effect of variation of one such parameter in **P** on the specification S and the corresponding variation of a particular measurement data in M. The measurement space, in this case, consists of the test response waveforms observed at different test points. Given the parameter space **P**, for any point in **P**, a mapping function (nonlinear) onto the specification space S,  $f: P \rightarrow S$ , can be computed. Similarly, for the same point, another mapping function (nonlinear) onto the measurement space in  $M, f: P \rightarrow M$ , can be computed. Therefore, for a region of acceptance in the circuit specification space, there exists a corresponding allowable "acceptable" region of variation of parameters in the parameter space. This in turn defines a region of



acceptance of the measurement data in the space M. A circuit can be declared faulty if the measurement data lies outside the acceptance region in M.

Alternatively, as shown in [11], a mapping function  $f: M \rightarrow S$  can be constructed for the circuit specifications S from all the measurements in the measurement space M using nonlinear statistical multivariate regression. Given the existence of the regression model for S, an unknown specification of a CUT can be predicted from the measured data.

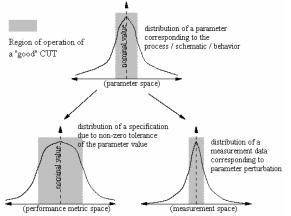


Figure 1. Variation in process or circuit parameter and its effect on specification and measurement.

In the proposed approach, Multivariate Adaptive Regression Splines (MARS) [13] are used to construct the regression model and estimate the test specifications of an embedded analog module from the reconstructed test response waveforms. The objective of the proposed test approach is to synthesize the measurement space M in order to construct regression models for accurate prediction of any circuit specification S. This is achieved by the means of:

- (1) modeling the parameter space
- (2) selecting critical (multi-parameter) perturbation modes in the parameter space
- (3) selecting the optimal test stimulus signal, and test response observation points concurrently

## 3. Test Architecture

The test architecture relies on application of a multi-tone test stimulus designed to maximize the ability to predict the circuit-under-test specifications from the observed test response measurements (Figure 2). An analog multiplexer is used to isolate the test stimulus in test mode from the functional input of the circuit corresponding to its normal operational mode. The test stimulus can be generated internally by an on-chip multi-tone signal generator or externally by a mixed-signal ATE. The test response waveforms are observed by the external ATE or an on-chip processor at one or more circuit nodes in the test mode. It is assumed that appropriate design-for-testability (DFT) circuitry is used to facilitate test stimulus application and test response observation. The test stimulus consists of DC and sinusoidal multitones (large signal). The test stimulus and the test response observation points are selected efficiently using an automated process, which is described in the following section.

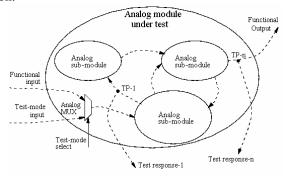


Figure 2. Test architecture.

# 4. Test Approach and Algorithms

The core algorithm consists of the following steps:

1. Identify critical single-parameter and dual-parameter perturbations that have the maximum contribution to the nonlinear relationship between test measurements and circuit specifications. This assumes that the nonlinear relationship is approximated by a quadratic function. This assumption is made to reduce simulation complexity.

2. Perform a simultaneous dual search for the optimal set of test frequencies and test points for a specified number of test points. For nonlinear circuits, the small-signal transfer function corresponding to an assumed DC bias is used for reference. Simulations performed in the process of iterative test stimulus selection are large signal, for both linear and nonlinear circuits. The "goodness" of a candidate waveform is determined by simulation of the process perturbations determined in Step 1.

#### 4.1 Computing Critical Parameter Perturbations

Specification failures due to parametric deviations are modeled in terms of the parameters and their tolerances as follows. Let, P be the collection of N process, circuit, and behavioral parameters for an analog CUT, denoted by the set  $\{P_{10}, P_{20}, ..., P_{N0}\}$  representing the nominal values of the parameters. The statistical distribution of each parameter and its correlation coefficient w.r.t. the distribution of every other parameter in **P** is known from prior wafer test structure measurements. In absence of the above data, each parameter in **P** is assumed to vary independently (*i.e.* no two parameters are correlated). This represents the worst scenario of all possible independent perturbation modes in the parameter space. If  $x_i$  represents the percentage deviation of the parameter  $P_i$  corresponding to its  $\pm 3\sigma$ deviation from its mean, then  $P_i \in [(P_{i0} - x_i P_{i0}), (P_{i0} +$  $x_i P_{i0}$ ]. The normalized deviation for  $P_i$  is given by  $p_i = (P_i)$  $(-P_{i0})/x_iP_{i0}$ ; where,  $p_i \in [-1, 1]$ , for all i=1...N and  $P_i \neq 0$ .



On the other hand, if,  $S_0$  is the design value of the specification, the normalized deviation *s* is given by,  $s = (S - S_0) / S_0$ . Assuming that the specification limits are two-sided, *i.e.* the specification has both the upper and lower limits, normalized limits  $s_u$  and  $s_l$  can be computed as:  $s_h = (S_H - S_0) / S_0$ , and  $s_l = (S_0 - S_L) / S_0$ . The normalized deviation in specification is modeled as:

$$s = A p^{T} + p B p^{T} + p C p^{T}$$
(1)  
where,  $\mathbf{A} = \{a_{1}, a_{2}, ..., a_{N}\}, \mathbf{B} = \text{diag}(\{b_{1}, b_{2}, ..., b_{N}\}),$   
$$\begin{bmatrix} 0 & C_{12} & C_{13} & \cdots & C_{1N} \end{bmatrix}$$

and		0	0	$C_{23}$	 $C_{2N}$	
	$C = \langle$	:	÷	÷	 ÷	}
		0	0	0	 $C_{N-1,N}$	
		0	0	0	 0	

The elements  $a_i$ 's A and  $b_i$ 's in B are computed using circuit simulation, where the parameter  $P_i$  is perturbed keeping other parameters at their respective nominal values and s is computed for each perturbation (Figure 1a,b). The  $a_i$  and  $b_i$  are computed by fitting the quadratic regression curve  $s = a_i p_i + b_i p_i^2$  in Eqn. (1).

A specification S is considered insensitive to a parameter variation in  $P_i$ , if

$$|a_i| \le \alpha \min(s_u, s_l), i=1...N$$
<sup>(2)</sup>

where, the threshold value  $\alpha$  is a constant,  $0 < \alpha < 1$ . The higher the value of  $\alpha$ , the more sensitive is the specification to parametric perturbation model.

After *A* and *B* are computed, the circuit is simulated using the joint parameter perturbations of the parameter pair  $(P_i, P_j)$ , while keeping other parameters at their respective nominal values and computing *s* each time (Figure 1c). The  $c_{ij}$ 's in *C* are computed by fitting the linear regression curve  $s - (a_i p_i + b_i p_i^2 + a_j p_j + b_j p_j^2) = c_{ij}(p_i p_j)$  of Eqn (1).

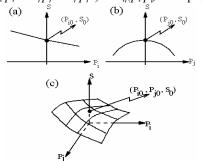


Figure 1. Effect of (a,b) single and (c) joint parameter perturbations on circuit specification

Since the parameter deviations in the model are normalized w.r.t. their worst case tolerance values, the computed coefficients in A (or B or C) are directly compared with each other to find the *relative importance* of the parameter deviations in terms of how they affect the circuits specification. The sensitivity-based analysis presented in [3] correspond to the particular case of B=0 and C=[0] in the present analysis. The assumption of B=0 and C=[0] is less accurate for modeling parameters such as device mismatch, where any deviation in either the +ve orve direction from the nominal value exhibits decrease (or increase) in the specification value as shown in Figure 1b. The slope of the sensitivity of the circuit specification to the parameter value around the nominal parameter value is however zero or small. The computation of A, B and C is simulation intensive. However, this incurs a one-time simulation cost.

Any iterative algorithm based test generation scheme requires that the CUT be simulated repeatedly. The simulation cost is high if **A**, **B** and **C** have a large number of coefficients. Therefore, to reduce the simulation cost during test stimulus generation, a subset of parameter perturbations (of all the prior simulated parameter perturbation modes) is selected for use during test generation and is based on the relative values of the coefficients in **A**, **B** and **C**. The specification test corresponding to performance metric S of the CUT is therefore relatively more susceptible to the selected critical parameter perturbations than to others. More specifically, a single or joint perturbation mode in the parameter space **P** is said to be critical for accurate computation of the specification in a specification based test if the following are satisfied,

$$|a_i| \ge \beta \min(s_u, s_i), i=1... N$$
(3)

$$|b_i|, |c_{ij}| \ge \gamma \min(s_u, s_l), i=1... N$$
(4)

The higher the value of  $\beta$ , the less parameter sensitive the fault model, whereas, the higher the value of  $\gamma$ , the more linearized the fault model. For multiple specifications, the overall set of critical perturbation modes consists of the union of the individual critical perturbation modes (sets of perturbations) for each of the specifications.

# 4.2 Test Generation and Test Point Selection Algorithm

The goal of the test generation algorithm is to determine the best multisine test stimulus waveform and a set of test response observation points and corresponding response measurements from which the CUT test specifications can be predicted as accurately as possible (see Figure 1). The core test generation algorithm consists of the following steps:

- (a) Preliminary small signal AC simulation and sensitivity analysis to determine an initial choice of test points and test frequencies
- (b) Large signal transient AC simulation of candidate test waveforms to handle nonlinear circuits during test stimulus generation

A multi-tone sinusoidal waveform is the transient test stimulus of choice. The test stimulus X(t) is of the form:

$$X(t) = V_0 + \sum_{m}^{N_m} u(t - t_{0m}) V_m \sin(w_m(t - t_{0m}))$$
<sup>(5)</sup>

where,



 $V_0$  = overall DC offset,

 $V_m$  = amplitude for m-th tone,

 $t_{0m}$  = initial delay for m-th tone,

 $N_m$  = maximum number of tones to be present in X(t).

The selection of the test waveform parameters and the concurrent selection of the test response observation points is performed by the algorithm discussed below.

For each critical perturbation mode  $P_k$ , at each circuit node *n*, the frequency response of the CUT,  $\Delta H_k(jw)$ 's, are computed using ac simulation, where,  $\Delta H_k(jw, n) = H_k(jw, n) - H(jw, n)$ ,  $H_k(jw,n) =$  amplitude response for single or joint perturbation  $P_k$ , (small signal analysis for nonlinear circuits) and H(jw, n) = amplitude response for nominal parameter values in **P** (small signal analysis for nonlinear circuits).

At the circuit node n, for a test-response frequency w, the observability vector for all the critical perturbation modes from the parameter set p is defined as:

 $\mathbf{O}(n,w) = \{\Delta H_1(jw,n) \ \Delta H_2(jw,n) \ \dots \ \Delta H_k(jw,n) \ \dots\}$ 

The higher the value of  $||\mathbf{O}(n,w)||$ , the more sensitive is the test response waveform of frequency *w* at the given node *n* to all the critical perturbations. The candidate test response observation point and the candidate test stimulus frequencies are chosen such that  $||\mathbf{O}(n,w)||$ 's are large and  $\mathbf{O}(n,w)$ 's have an orthogonal relationship with each other as follows:

- (1) For the given set of critical parameter perturbation modes and the test response frequency *w*, a circuit node  $n_1$  is better candidate than the circuit node  $n_2$  for being selected a test-response observation point, if  $||\mathbf{O}(n_1,w)|| \ge ||\mathbf{O}(n_2,w)||$ .
- (2) For the given set of critical parameter perturbation modes and circuit node *n*, the test response frequency  $w_1$  is a better selection than  $w_2$ , if  $||\mathbf{O}(n,w_1)|| > ||\mathbf{O}(n,w_2)||$ .

Based on (1) and (2), once an observability vector  $O(n_1, w_1)$  is selected, the selection criteria is extended over multiple test points and test response frequencies as follows. The vector  $O(n_2, w_2)$  is deemed a better candidate than  $O(n_3, w_3)$  when used along with  $O(n_1, w_1)$  for test generation, if

$$\frac{\left\|\hat{O}(n_{1},w_{1}).\hat{O}(n_{2},w_{2})\right\|}{\left\|O(n_{1},w_{1})\right\|.\left\|O(n_{2},w_{2})\right\|} < \frac{\left\|\hat{O}(n_{1},w_{1}).\hat{O}(n_{3},w_{3})\right\|}{\left\|O(n_{1},w_{1})\right\|.\left\|O(n_{3},w_{3})\right\|},$$

where  $\hat{O}(n, w)$  is the unit vector in the direction of  $\mathbf{O}(n, w)$ . Hence, the more orthogonal the observability vector to  $\mathbf{O}(n_1, w_1)$ , the better chance it has to be combined with  $\mathbf{O}(n_1, w_1)$  during test generation.

Applying the criteria in (1) to (2), a list of candidate test points and associated test-stimulus frequencies are obtained. A fast greedy algorithm is used for final selection of the number of frequencies. In this algorithm, *large signal* simulation is performed for both linear and nonlinear circuits.

Begin Test Stimulus Generation and Test Point Selection Algorithm

selected test-points:= the first candidate test-point in the list

# do

```
begin
```

frequency list  $\{w_m \ s\}$  in Eqn (5) := the first frequency in the list for the given test-points

```
do
begin
```

```
initialize [V_0, \{V_m, t_{0m}\}'s] of Eqn (5) as

V_0 := 0; t_{0m} := 0; V_m := (V_{DD} - V_{SS}) / (2*N_m)
```

do begi

```
begin
         Simulate netlist for all critical perturbation vectors
         Create statistical regression model representing
                  f: M \rightarrow S, where, M is the test-response
                  waveforms at the selected test points
         Simulate netlist for a set of random perturbation
                                                     vectors
         Compute specification, evaluate f: M \rightarrow S and
                  compute their differences (error in
                  specification prediction) for the
                 random perturbation vectors
         error = max (absolute values of prediction errors)
         Select another [V_0, \{V_m, t_{0m}\}'s] in its vicinity based
                 error values in previous iterations using
                 the following constraints:
                 V_{SS} < V_m, V_0 < V_{DD}; 0 < t_{0m} < 2\pi/w_m
     while(local minimum for error is found);
     if(error < input-error-threshold) then
         break outer loop;
     else
         include another frequency from the list
     end
  while (no. of frequencies test stimulus < N_m)
   include another test point from the list
until(all candidate test points are utilized)
```

end

The search for the minimum prediction error implemented in the algorithm is a fast, greedy search and may converge to a local minimum. However, sinusoids with new frequencies are included in X(t) in successive iterations in order to achieve lower specification prediction error. Unlike in [16], instead of behavioral models of the circuit, the final netlist is simulated for test generation.

In contrast to [8], where the test point selection approach attempts to maximize the controllability and observability, the final test observation points are selected in conjunction with the test generation algorithm and the algorithm attempts to increase the accuracy of the test using an iterative search technique.

# 5. Experimental Results

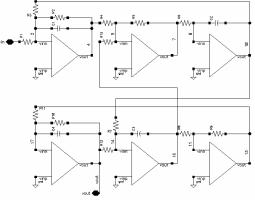
In this section, case studies on which the proposed test generation and test point selection method has been applied are presented.

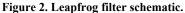
The first example is a low-pass leapfrog filter [14]. The circuit component values are:  $R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R_7 = R_8 = R_9 = R_{10} = R_{11} = 10 k\Omega$ ;  $C_1 = C_4 = 10 nF$ ;  $C_2 = C_3 = 20 nF$ . The op-amps are assumed to be fault free, in this example. The tolerance is assumed to be 10% around the nominal value of the resistors and the capacitors. In the



circuit performance metric space, the 3dB bandwidth of the filter is chosen as the specification of interest. The circuit is fault-free if the cut-off frequency lies within 1.4 kHz  $\pm$ 50Hz.

The test generation and test point selection approach is verified by injecting parametric failures in the form of random variations of the components around their nominal values. The specifications for these circuits are predicted with the regression model and pass/fail decisions are made. The predicted 3dB bandwidth specifications are compared against the 3dB bandwidth specification information available from ac analysis. The predicted values exhibit close agreement with the specifications obtained from ac analysis and all of the predicted specification data lie in the vicinity of the straight line with slope +1, which represents the locus of "ideal" predictions. When using single test response observation point 'vout' (the primary output), the proposed approach is able to distinguish between faulty and fault-free circuits if the actual bandwidth specification values do not lie within the prediction error of ±2.9% around the upper and lower limits of the acceptance region in the test-specification. For two test points selected (primary output and one optimal internal test point), the above prediction error reduces to  $\pm 1.9\%$ . The results are summarized in Table 1.





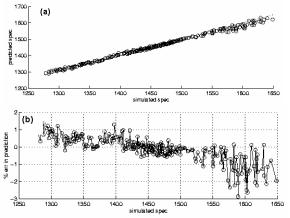


Figure 3. Prediction of the 3-dB bandwidth specification of Leapfrog filter; single test-point = 'vout'; (a) prediction tracking (b) prediction error < 2.9%

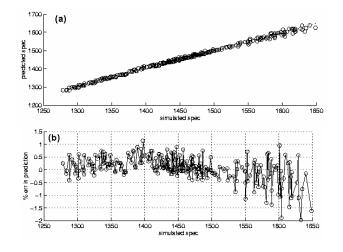


Figure 4. Prediction of the 3-dB bandwidth specification of Leapfrog filter; 2 optimal test-points '10' and 'vout'; (a) prediction tracking (b) prediction error < 1.9%

The second example is a continuous-time state-variable filter [14]. 3dB cut-off frequencies of the high-pass and lowpass functions and the center-frequency of the band-pass function were selected as the specification of interest. The circuit component values are:  $R_1 = R_2 = R_3 = R_4 = R_5 = R_6 =$  $10k\Omega$ ,  $R_7 = 12k\Omega$ ;  $C_1 = C_2 = 20nF$ . The nominal specification values are 610 Hz, 1.07 Hz and 800 Hz respectively. The circuit is said to be fault-free if the frequency specification lie within  $\pm$  50Hz of the respective nominal values.

I able I	. Su	mma	ry o	t the si	mula	tion re	esults.		
Circuit	#	of	#	of	test	Max.	error	in	s
nder test	criti	cal	obse	ervation		predict	tion		

Circuit under test	# of critical param. perturba tions	# of test observation points	Max. error in spec prediction		
Leapfrog filter	15	1 (vout)	LP 3dB <i>f</i> : 2.89%		
		2 (node 10 & vout)	LP 3dB <i>f</i> : 1.97%		
State-	11	1 (band-pass out)	LP 3dB <i>f</i> : 4.2%		
variable			BP center <i>f</i> : 5.8%		
filter			HP 3dB <i>f</i> : 3.0%		
		2 (low-pass & high-pass out)	LP 3dB <i>f</i> : 2.0%		
			BP center <i>f</i> : 2.1%		
			HP 3dB <i>f</i> : 1.8%		

In Figure 6 and Figure 7 the tracking of the 3dB low-pass cut-off frequency and band-pass center frequency is shown as examples. While selecting the optimal single test response observation point, the band-pass function output node was converged at. However, selecting two optimal test points for the same specifications, the low-pass and highpass function output nodes were picked by the algorithm. Test accuracy improves for more number of optimal test points selected. The results presented are for single-tone  $(N_m)$ = 1) test stimulus waveforms with non-zero DC offset.



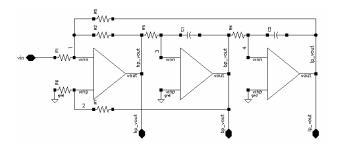


Figure 5. State-variable filter schematic.

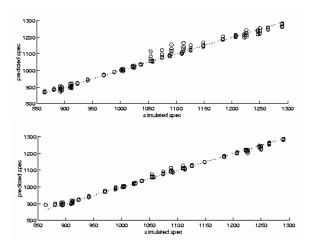


Figure 6. low-pass 3dB cut-off frequency specification tracking for state-variable filter; (a) 1 optimal test point 'bp\_vout', prediction error < 4.2%; (b) 2 optimal test-points 'lp\_vout' and 'hp\_vout', prediction error < 2.0%

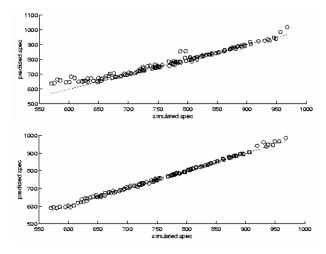


Figure 7. band-pass center frequency specification tracking for state-variable filter; (a) 1 optima test point 'bp\_vout', prediction error < 5.8%; (b) 2 optimal test-points 'lp\_vout' and 'hp\_vout', prediction error < 2.1%

#### 6. Conclusion

In this paper a new automated test generation and test point selection approach is presented for specification oriented testing analog circuits. The approach is based on co-optimization of transient multi-tone test stimuli construction and test response observation node selection for maximum specification prediction accuracy. The simulation results on different case studies exhibit significant tracking of the circuit specifications by the regression models generated using the presented approach.

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