Cost Model Analysis of DFT Based Fault Tolerant SOC Designs

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Abstract

A lot of emphasis has been placed on the test cost of chips and a variety of models have been proposed in the literature. However, they do not include the fault tolerance consideration. Existing models are incomplete with the fact that most do not take into account the costs involved once the chip reaches the market. This paper addresses these limitations by introducing the cost model for a fault tolerant system taking into account the reliability factor of a system. This model will help designers analyze the need for a fault tolerant system and its feasibility in the industry. This paper models the costs involved during the life cycle of a chip. Two case studies using the proposed model are presented in order to substantiate the need to put fault tolerant designs into chips.

1   Introduction

In this work, we model the cost of a fault tolerant chip with DFT embedded in it. The industry is slowly realizing the need for fault tolerance in systems due to the increased susceptibility of designs to internal disturbances such as switching conditions and external disturbances like atmospheric radiation (soft errors) [7]. These disturbances result in a need for life-long testing of chips. The primary reasons to go for fault tolerant designs would be to ensure reliability of the product for a longer duration with the customer thus ensuring his satisfaction and also lower after-sales services.

A study of whether DFT techniques are required for a chip is given in [8],[9]. But addressing the issue related to the need for fault tolerance for a chip involves certain parameters which are not discussed in those models. Also, these models do not deal with the costs arising during the lifecycle of the chip in the market which would certainly form a major cost parameter. With the advent of SOCs, self repairable chips and rising test costs, we need models to ensure that there is absolute need for fault tolerant features

on chip which would ensure cost effectiveness and also its success in the market.

In this paper, we propose our cost model and break it down further into sub-systems which are considered as factors contributing to the cost. In Section 2, we give a description of our basic model proposed for fault tolerant designs. Section 2.1 goes into the details of the silicon cost involved. Escape cost is dealt with in detail in Section 2.2. Section 2.3 deals with the personnel cost involved in designing the chip. Section 3 presents a qualitative analysis of the need to keep track of the time to market factor. Section 4 deals with an economic factor called NPV (which is not considered much while performing cost modeling though it is equally important as the other parameters described in our model). In Section 5, we present two case studies, one of a generic chip and the other for a fault tolerant core. In the final section, we discuss the psychological issues which come into consideration due to the problems arising out of the failure of the product with fault tolerant features. The presented model clearly identifies system tradeoffs. A major highlight of this model is its flexibility. This model can predict the cost of a fault tolerant design and also that of a simple DFT based design without any fault tolerance by simply excluding certain parameters in the model equation. Hence, the same model can be used in two different design environments for modeling costs.

2   Basic Model

In this section, we present an overview of the model. When fault tolerance is adapted in designs, the increase in cost due to the overhead of redundant hardware is compensated by the savings obtained in field operations. This is achieved due to increased reliability of the system. The following equation characterizes this fact.

$$C_{excess} = C + \alpha N_{FT} P - (M N_{NFT} + T') \qquad (1)$$

where C_{excess} − Excess cost imposed on a system with fault tolerance, C − Cost of the units with fault tolerant feature, α − Probability of Failure, N_{FT} − Number of units with Fault Tolerant feature, N_{NFT} − Number of units with

no Fault Tolerant feature ($N_{FT}=N_{NFT}$), P – Manufacturing Cost of a chip with fault tolerant features, M – Cost of a chip without any fault tolerant feature, T' – On field replacement cost for chips without fault tolerance.

The excess cost can be positive or negative depending on certain parameters which will be described now. The first term in the above expression is the manufacturing cost of the chip which includes the design cost, test cost etc. The second term in eq (1) is the most significant one. Not all the chips with fault tolerance need to work successfully during the period of operation. This term would give the cost of those chips which failed on-site in spite of being fault tolerant and resulting in the replacement of the chip. The third parameter has the cost of the chip without fault tolerance along with the on-field testing cost, when the chip fails on-site.

A positive value for C_{excess} tells the designer that he might have to change the fault tolerant architecture design or go for a design with no fault tolerance in it. This would help the designer evaluate different fault tolerant architectures on a cost basis. When C_{excess} is negative then the designer is ensured of a cost effective system with a good reliability to survive in the field.

α is modeled along the lines of system reliability (R) as $\alpha = 1 - R$. This parameter would give us the probability of survival of a system on field. The parameter is dependant on the architecture used to achieve fault tolerance. Higher the reliability of the system the lower would be the cost of replacing any parts on field and hence less of on-field activity by the personnel. But this would also result in an increase in the manufacturing cost through an increase in area of redundant parts and other factors.

In the following sections, we will model the cost of a chip with fault tolerant features. This will include the cost arising out of silicon area, personnel cost and escape cost as given in [8]. The tester cost is already modeled in [8] and we will use this result in our model.

2.1   Cost Due to Increase in Chip Area

It is shown in [2] that yield decreases strongly with chip area which results in the increase in silicon cost as a function of area. We will adopt the model of [8] and modify it to include the area increase brought about by the extra hardware due to fault tolerance apart from the area consumed by the DFT and the chip design.

$$C_{silicon} = Q_{wafer} * (A_{redundant} + A_{test} + A_{chip})/(\Pi R_w^2 \beta_{wafer\_die}) \quad (2)$$

where $C_{silicon}$ – Cost due to silicon, Q_{wafer} – Cost of the wafer, $A_{redundant}$ – Area to be redundant on the chip, A_{test} – Area increase due to DFT features, A_{chip} – Area of the basic chip design, R_w – Radius of the wafer, β_{wafer_die} – Percentage utilization of the dies from the wafer ignoring those which get formed around the circumference of the wafer.

The yield (Y) is modeled based on Seeds equation [6] given as $Y = (1 + AD)^{-1}$ where D is the defect density and A the area of the chip.

We model the area parameter in the above equation as

$$(A_{redundant} + A_{test} + A_{chip}) \text{ as } A_{logic} + A_{memory}$$

where

$$A_{logic} = (1 + \gamma_{r\_area})A \quad (3)$$

$$A_{memory} = A(1 + (\log_2(m_{size}) * 1.33)/m_{size}) \quad (4)$$

where γ_{r_area} – Area overhead of DFT and redundancy, m_{size} – Memory capacity. This model was taken from [5]. The increase in area results in increased logic in the circuit. This increases the time spent on the ATE which is also modeled in [8].

2.2   Test Escape Cost

The second term in eq (1) contributes to what is called escape costs which is further examined in more detail in this section. The escape test cost arises from the fact that we are not able to achieve 100% fault coverage and in our case 100% reliability. The escape rate is given in [10] as

$$E_r = (1 - Y)^{(1-f)} \quad (5)$$

where f is the fault coverage. The escape cost which results due to bad fault coverage for a fault tolerant system is given as

$$C_{escape} = \alpha N_{FT}P + M E_r \alpha_{escape} N_{FT} - RPN_{FT} \quad (6)$$

where α_{escape} is given as the factor representing the risk incurred in accepting a defective IC, P is the manufacturing cost of one chip. The first parameter comes in eq (1) as the second term while the other two terms are covered in the C parameter of eq (1). The second term above refers to the escape cost arising due to the test coverage [8]. The third parameter refers to the cost reduction by reconfiguring around those parts which failed during testing with the spares. The net effect of the above equation takes into consideration the escape cost arising from the failure of fault tolerance.

2.3   Increase in Personnel Cost

The cost increase in personnel is essentially due to the extra effort placed in design and test. One must take care of essential parameters like area and power while designing such circuitry. The cost arising from this is given as

$$C_{personnel} = N_{wh} * N_{wp} * C_D \quad (7)$$

where
N_{wh}=Time for Design+Test, N_{wp}=Number of people working on the design and C_D is the personnel cost per unit time.

However, one should not forget that the excess cost, which arises here due to increase in man hours, will be compensated later once the product reaches the market due to its longer life without service time. Due to the additional features, the chip will have a higher probability of survival without any form of error or human intervention. This will lead to cost reduction of field engineers who might need to replace parts if the chip fails.

This is included in the following equation

$$C_{per\_sav} = R * N_{FT} * P_{personnel} \qquad (8)$$

where $P_{personnel}$ – Personnel Cost in fixing in-field problems. However, there is a personnel cost arising from fixing the units which have failed due to the poor reliability of the system in spite of fault tolerance being added to it. This cost is added to the cost of the good units and is given as

$$C_{per\_loss} = \alpha * N_{FT} * P_{personnel} \qquad (9)$$

The effective spending by the company due to added features is given below.

$$C_{effective} = C_{personnel} - C_{per\_sav} + C_{per\_loss} \qquad (10)$$

where $C_{effective}$ is the net expense incurred in terms of personnel cost. The cost models in general do not take into account the C_{per_sav} factor into account while deciding the costs, but since our model relies on how long the chip will operate with the customer without defaulting, we included this parameter.

3   Time to Market

The factor which would increase the time to market is the increase in time for design and test due to added components. The key to reducing this increase would be to reduce the development and test time. It is estimated that a 6 month delay in releasing the product to the market would lead to a 33% profit loss [1]. The more time is spent by the designers with the product in the labs, the greater would be the loss in revenue. The semiconductor industry is still governed by Moore's law and as technology changes, the products have to be updated with the new one's. Mismatch between the new technology and the older design would result in the chip going back to the design house for revamp and hence further delay in reaching the market [7]. Where does fault tolerance come into the picture? It is important for the designer to understand the need to keep adding new features to the chip. He would have to ensure that consumer needs are met and also stave off competition by getting to the market first. Now fault tolerance along with DFT would come to help in testing issues. One could reduce the time spent with the tester through DFT. By improving the fault tolerance of the chip through redundancy, we could easily reconfigure the spare when a fault is found in the manufacturing phase or in the field. Fault tolerance would help

us to ensure that we can meet the required supply of perfectly working chips. Say it takes n months to design and fabricate a chip. Now when errors are found, we will have to spend some extra time in fabricating new chips to replace those that failed in order to keep the production volume constant. This would in essence delay the arrival of the chips to the market and also increase the manufacturing cost due to the addition of extra chips which is covered in eq (1) under the second half of the model. Implementing fault tolerance would thus help us to significantly reduce the above factors which delays the time to market. There are two models which help us estimate the time to market of a chip. One of them is the Simplified triangular time-to-market model [4] and the other is Growth-Stagnation-Decline (GSD) time to market model [3].

4   Net Present Value

A factor which contributes to the loss in revenue due to a delayed entry into the market, in economics, is called the Net Present Value (NPV). NPV compares the value of a currency today versus the value of that same currency in the future, after taking inflation and return into account. If the NPV of a prospective project is positive, then it should be accepted. However, if it is negative, then the project probably should be rejected because cash flows are negative. Now it is a common economic sense that the value of money today is not going to be the same in 6 months or a year from now. So whatever money is spent today will be of far less value. Now, if we are going to spend x dollars in R&D, design test and fab as per estimate of releasing it on day Y to meet the on-time to market, but due to certain delays are forced to release it 6 months later, then it essentially shows that the value of the money spent and the amount which could have been recovered by early release due to a higher value of the currency would be stupendous especially if the volume is large. This is covered in eq (1) implicitly. There are models for NPV estimates which are not presented in this work, but should be noted while taking the time to market factors.

5   Case Study

A study was done on a generic chip with data obtained from [1],[8]. Though a few parameters were not available to us, we have made some calculated assumptions which are verified through the obtained results. In Fig. 1, we see that as reliability increases, so does the silicon cost since increase in reliability is brought about by the spares added into the logic as redundant devices. Also, note the drop in escape costs due to a higher degree of reliability. The third cost is the personnel cost. Though this cost does increase due to increase in design time, it is fairly compensated by the limited amount of work required to be done in the form of service/repair. Hence, there seems to be a dip in the graph due to increased benefits of fault tolerance and hence an increase in the savings.
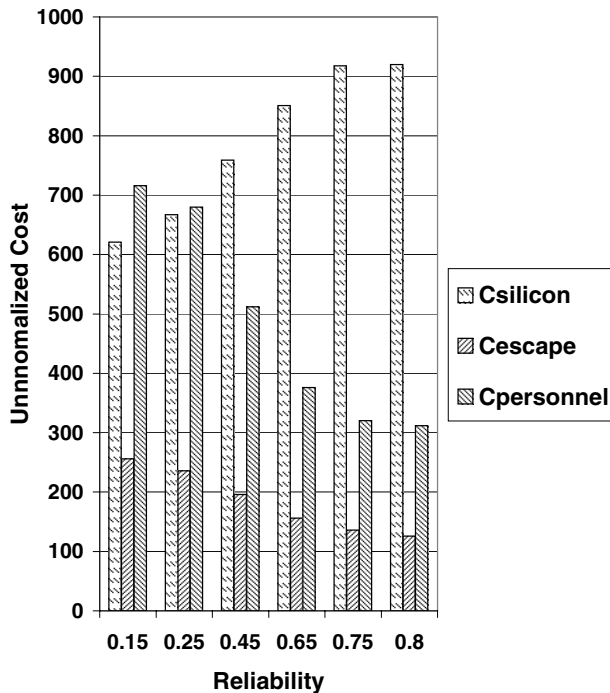
Figure 1. Cost vs Reliability

Figure 2. Excess Cost vs Reliability

Figure 3. Cost vs Reliability

In Fig. 2, we do a net calculation of the cost with fault tolerance and without it. The tester cost is a variable parameter in the cost model equation since it depends on the amount of redundant logic we need to test and would essentially vary with the reliability of the system. It is seen that with high reliability the unit with fault tolerance has a far greater cost advantage than the unit without fault tolerance while with lower reliability the reverse trend can be observed. The conclusion from the above plot is that for this particular chip, it is better to go for a high reliability system in order to save on after sales services and also ensure good customer relationship.

We have performed a case study of another SOC chip and found some interesting results. For this chip, we estimated the area for a wide range of reliability values. In Fig. 3, we can see the trend of increasing silicon costs due to increase in the area of the chip. The escape cost drop is also on expected lines since we have increased the reliability. But there is a slight dip in the personnel costs due to the lesser interaction of the service personnel with the chip on-site. This is because of the optimum reliability offered by the chip that the chance of it failing is minimized and the area cost overhead is also bearable. At high reliability the cost of the silicon is too high to be compensated by the high reliability. We would thus be able to strike a good balance between the cost of silicon as well as reliability and the other cost involved by studying the data before hand, before going on to make any critical decisions with respect to the chip design.

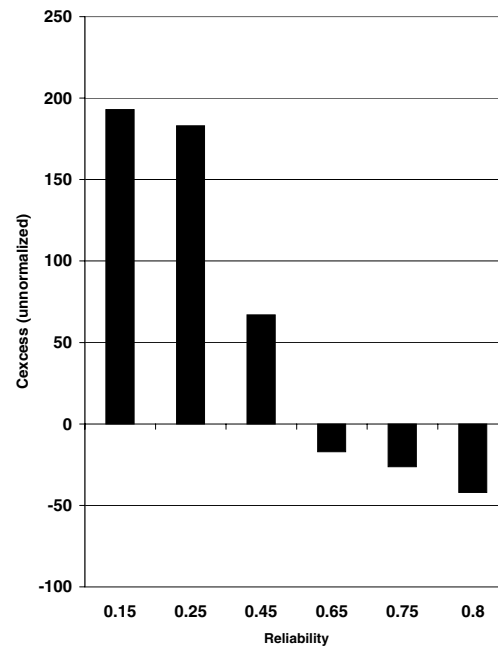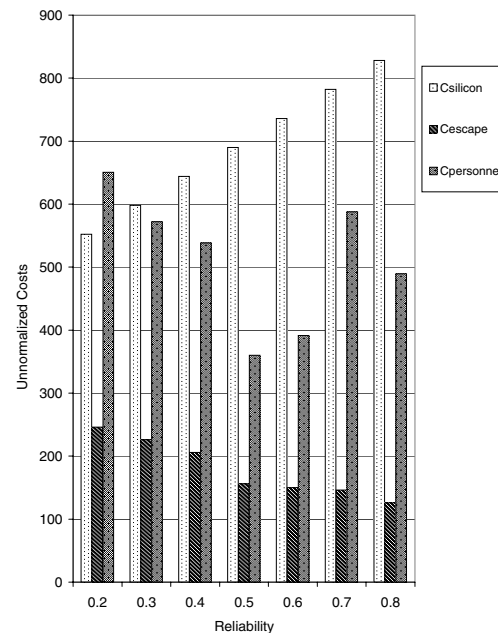Fig. 4 is a reflection of what has been said above. It shows that with a reliability of around 0.5-0.6 we are guaranteed of a cost effective chip. Thus our cost model would help in modeling design issues by factoring the reliability of the chip into the cost model.
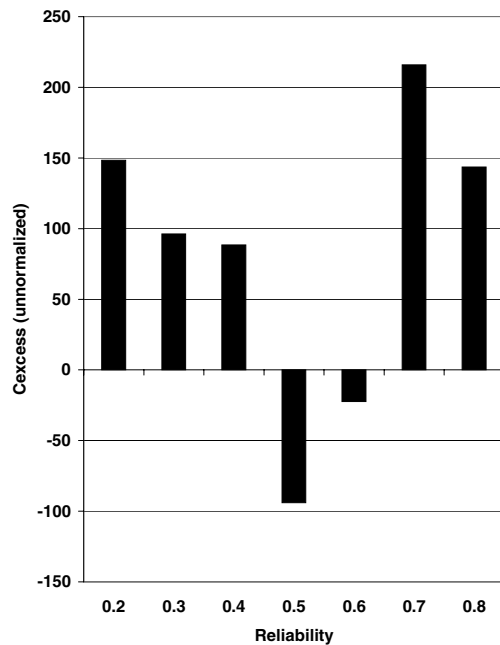
Figure 4. Excess Cost vs Reliability

6 Psychological Issues - A Discussion

Eq (1) is proposed on the assumption that the customer, if faced with a problem, would come back to the same vendor that sold him the product. If he/she encounters a problem during the warranty period, then he/she is most likely to do so. But the failure of the product to meet its desired life by the customer would result in customer dissatisfaction which can result in a loss of customer base. The warranty period of the product would have to be chosen wisely for this nature of problems that should satisfy both the customer as well as the producer. Such problems go deeper into economic aspects which are beyond the scope of this paper.

Once the chip does fail after the warranty period, the company needs not to worry about servicing the chip at any added cost to the economic model of the chip since this would be an extraneous event to the life of the chip as far as the cost goes. But the psychological factor to be dealt with here would prove quite expensive. If the customer is not satisfied with the working of the product during its actual life cycle then the chances of him/her changing vendors is quite high. This would result in a loss of business for the vendor. Another factor one needs to be worried about is Moore's Law. If the vendor is not updated with the latest technologies and he/she goes obsolete, then there is no place for him in the market and there is no way he/she can attract customers. A factor not considered in cost models is the amount of engineering effort going into a design. Though the personnel cost does take into account the duration of work hours spent by a designer for a product, it does not take into account the actual effort (in psychological terms)

put in by a designer. Designers would definitely not opt for complex designs which would require a lot of effort to be put in, unless the expected results are really high. This issue from the designers perspective could be studied as a future work.

7 Conclusion

A cost model for a fault tolerant chip taking DFT into account, is proposed. The model provides flexibility to handle different types of cost that may arise during the life cycle of a chip. It focuses on tying together issues on design, test and time to market in order to decide on a chip's features. Bringing the reliability factor into the model ensures that we are able to study the cost of the chip through its life cycle. Its flexibility can be seen from the fact that we can model not only fault tolerant chips, but also DFT based systems by excluding the required factors in eq (1). The model is intended to aid the project team managers to make certain decisions on a chip before initiating work.

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