An Arbitrary Stressed NBTI Compact Model for Analog/Mixed-Signal Reliability Simulations

Jinbo Wan and Hans G. Kerkhoff
Testable Design and Testing of Integrated Systems Group, CTIT, University of Twente
Enschede, the Netherlands
j.wan@utwente.nl, h.g.kerkhoff@utwente.nl

Abstract

A compact NBTI model is presented by directly solving the reaction-diffusion (RD) equations in a simple way. The new model can handle arbitrary stress conditions without solving time-consuming equations and is hence very suitable for analog/mixed-signal NBTI simulations in SPICE-like environments. The model has been implemented in Cadence ADE with Verilog-A and also takes the stochastic effect of aging into account. The simulation speed has increased at least thousands times. The performance of the model is validated by both RD theoretical solutions as well as silicon results.

Keywords

Reliability, NBTI, RD model, Reaction-Diffusion solution, analog, mixed-signal, simulation

1. Introduction

Recent progress in advanced deep-submicron CMOS technologies make circuits faster, smaller, and operate at lower power. However, behind these benefits, the reliability becomes a major concern. The reliability issues significantly reduce the product yield and lifetime. In order to apply new CMOS technologies, especially in some highly dependable mixed-signal areas like the analog front-ends in the automotive arena [1], reliability problems need to be considered during the circuit design period. Accurate reliability simulations are in high demand to assure design success.

One of the problems for analog/mixed-signal reliability simulation is the lack of accurate aging models. This is especially true for the negative bias temperature instability (NBTI), which is probably the most critical aging effect in advanced deep-submicron CMOS technologies nowadays. The dominant degradation due to NBTI is threshold shift with time in PMOS transistors under stress. Moreover, the NBTI degradation can partly recover after the stress has been removed, which make both the measurements as well as the modelling very difficult. In fact, until now, there is still no proper solution to accurately measure the NBTI degradations [2]. The present measurement limitations block the insight into the physical cause, and hence the modelling theories for the NBTI degradation are still under debate [3], [4].

Despite much effort spent in NBTI modelling theories, there is a big gap between modelling and implementation in SPICE-like environments which are familiar to analog/mixed-signal circuit designers. In addition, the NBTI modelling publications are mainly focused on DC stresses and square-wave stresses (AC stress or dynamic NBTI in some publications), which are not typical cases in analog/mixed-signal circuits. Now, many simulation tools apply a simplification by using the *average DC stress* instead of the *real stress* to evaluate the NBTI degradations. This approach will dramatically underestimate the NBTI degradation and cause a large error in long-time extrapolation [5].

In order to apply the NBTI aging simulation to analog/mixed-signal circuits, the NBTI model should be able to:

1. Handle arbitrary stress conditions, like arbitrary voltage stress waveforms and arbitrary temperature stress waveforms.
2. Be easy to implement in SPICE-like environments and embed in existing design flows.
3. Take into account the stochastic effect of aging and enable the combination with process-variation simulations.
4. Realize short simulation times, even for large circuits.

Instead of proposing new NBTI theories, this paper shorts the gap between NBTI theories and SPICE-like environments. A new compact NBTI model will be introduced which satisfies the above four requirements and is suitable for analog/mixed-signal NBTI simulations in the Cadence Analog Design Environment (ADE). The new model is based on completely solving the reaction-diffusion (RD) equations [6] in a smart way. It can achieve high accuracy with only a small computational effort.

The paper is organized as follows. Section 2 briefly reviews the existing NBTI modelling theories. Section 3 demonstrates the derivation of the new compact model from the original RD theory. Section 4 evaluates the performance of the model. The model implementation is discussed in section 5 as well as simulation times and stochastic aging simulation. Section 6 provides the conclusions.

2. Brief review of existing NBTI models

Currently there are several NBTI models used in published papers. The most simple NBTI model is based on fitting the DC stress measurements in the logarithmic domain, which could be referred to as the “power model” [7]. The power model is not based on any physical meanings but is simple to extract from measurements and easy to implement in simulation software. In fact, many commercial EDA companies and silicon foundries, like Cadence and TSMC, provide NBTI simulation by means of power models. However, the power model can only handle DC stresses because it cannot model the recovering phenomenon of NBTI.

Another NBTI model is the reaction-diffusion (RD) model, which has first been discussed by Jeppson in 1977 [8]. From 2003 on, Alam [6] reviewed many old NBTI experiments and

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new on-the-fly (OTF) measurements. He claims that the NBTI degradation is mainly because of the generation and annealing of interface traps N_{IT}, which can be modeled by the classical RD theory. Based on that explanation, he proposed a set of RD equations and showed the possibility to model the stress and relaxation of NBTI by solving those RD equations. In principle, the RD model can work under arbitrary stress waveforms, like a sine waveform and triangular waveform. However, it is very difficult to solve those RD equations, and commonly used mathematical solvers are too complicated to be implemented in circuit simulation software. Hence the normal approach for the simulation with the RD model is using some linear approximation for particular stress waveforms, like DC and square waves [9].

Although the RD model is the most accepted NBTI model, there are many papers that claim the RD model has limitations. For example, the RD model cannot explain the NBTI log-like recovery transient and the shape of AC duty-cycle dependence [10]. Based on these observations and new measurement techniques, a number of new NBTI modelling theories have been proposed in recent years. Grasser proposed a "well-based" model [10], Velamala proposed a "trapping/de-trapping" model [11], and Kufluoglu proposed a "parallel diffusion pass way" model [12].

Despite the debate of different NBTI modelling theories, the latest studies [3], [13], [14] show that the RD model is the only one which agrees with long-time measurements (>100 hours). They show the RD model dominates in long-time degradation, and together with the hole trapping de-trapping, dominate in short time; it saturates after around thousand seconds, and can be grouped to accurately model both short-time fast change NBTI behaviour as well as the long-time one-over-six (0.16) power law behaviour.

3. Model details

The new compact NBTI model for analog/mixed-signal reliability simulations is based on the RD theory. The reason is that the analog/mixed-signal circuits are working in moderate stressed condition and suffer less hole trapping/de-trapping problems as compared to heavy-stressed digital circuits. In addition, for studying the life-time of the circuits, it is more interesting to investigate the long-time degradation instead of heavily stressed, instant recovery behaviour.

The classic RD equations will be reviewed first. Different from other papers, our model is based on directly solving the RD equations in a simple way. It will be introduced in the second part of this section.

3.1. Classic RD equations

According to the RD theory, the NBTI degradation can be explained as the generation of dangling bonds in the region close to the Si/SiO2 interface [6]. There are two steps involved during the process of NBTI being reaction and diffusion, as shown in Figure 1.

During the reaction phase, some Si-H bonds at the Si/SiO_2 interface are broken under the electrical stress. The generated "Si-" dangling bonds are remaining at the interface and are responsible for the threshold shift. The H atoms will combine into neutral H_2 and diffuse away from the Si/SiO_2 interface into the gate-oxide and eventually into the gate poly-silicon.

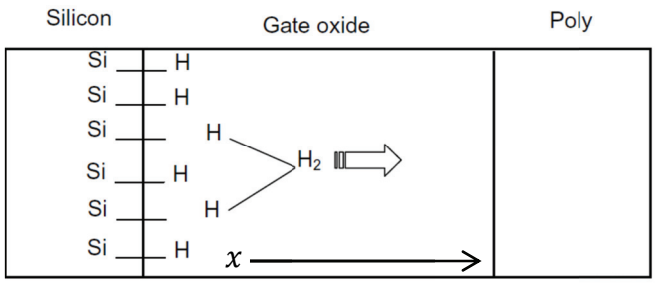

Figure 1: Schematic description of the RD model used to interpret interface-trap generation during NBTI stress [6].

$$\frac{dN_{IT}}{dt} = k_F(N_0 - N_{IT}) - k_R N_H(0,t) N_{IT} \quad (1)$$

$$N_{H_2} = k_H N_H^2 \quad (2)$$

$$\frac{dN_{H_2}}{dt} = D_{H_2}\frac{d^2 N_{H_2}}{dx^2} \quad (3)$$

This process is referred to as diffusion. The classic RD equations can be expressed in (1)~(3) from [6], where N_{IT} is the number of interface traps at any given instant, N_0 is the initial number of unbroken Si-H bonds, $N_H(0,t)$ is the concentration of hydrogen atoms at the Si/SiO_2 interface at any given instant, k_F is the oxide-field dependent forward dissociation rate, and k_R is the backward combination rate [6]. Equation (1) describes the generation rate of interface traps, which is the same as the generation rate of hydrogen atoms. In equation (2)~(3), N_{H_2} is the concentration of the neutral H_2, k_H is the combination rate of H atoms, D_{H_2} is the H_2 diffusion coefficient, and x is the location perpendicular to the silicon oxide interface, as shown in Figure 1.

3.2. Our solution for RD equations and the compact NBTI model

The reaction-diffusion equations (1)~(3) describe the process of NBTI and could be used to obtain the aging degradations, for example, in terms of the threshold-voltage shift. However, they are very difficult to solve in a general form. In order to find a solution which is suitable for analog applications, one needs to simplify the conditions and make some assumptions as discussed in the following. Based on the research in [9], the trap generation is slow from the initial period of the stress till the end of the product life and the broken Si-H bonds during NBTI are just a very small part of the total Si-H bonds. Hence $dN_{IT}/dt \approx 0$ and $N_{IT} \ll N_0$. Under these assumptions (1) and (2) can be combined and reduced to:

$$\sqrt{N_{H_2}(0,t)} \cdot N_{IT} \approx \frac{\sqrt{k_H} \cdot k_F}{k_R} N_0. \quad (4)$$

The number of interface traps (N_{IT}) is equal to the total number of H atoms diffused from the Si/SiO_2 interface ($x = 0$) [6]. As a result, the relationship between N_{IT} and N_{H_2} can be expressed as:

$$N_{IT} = 2\int_0^\infty N_{H_2}(x,t)dx. \quad (5)$$

In fact, most RD theory-based NBTI models use equations (3)~(5) to obtain the threshold shift. The difference is that the

various authors use different approaches to approximate the solution under DC or square-wave stress cases [8], [9], or employ complicated solvers to solve the equations in a time-consuming way to accurately evaluate the RD theory [3], [6].

Compared to other papers, we will directly solve the equation set (3)~(5) in a simple, fast way. Since in submicron CMOS technologies, the gate oxide is by far thinner than the gate poly-silicon and the H_2 diffusion much faster in the gate oxide [9], the number of H_2 in the gate dioxide can be ignored while calculating long stress-time situations. The diffusion coefficient D_{H_2} in the poly-silicon is treated as a constant. Applying the Laplace transform for (3) to solve the differential equation, the solution for N_{H_2} in the Laplace transform can be derived as:

$$\widetilde{N_{H_2}}(x,s) = \widetilde{N_{H_2}}(0,s) \cdot exp\left[-\left(\frac{s}{D_{H_2}}\right)^{\frac{1}{2}} \cdot x\right] \quad (6)$$

In (6), the superscript $\widetilde{\ }$ is referred to as the Laplace transform of corresponding functions. By substitution of (6) into (5), the solution for N_{IT} in the *s*-domain can be written as:

$$\widetilde{N_{IT}}(s) = 2 \cdot \int_0^{\infty} \widetilde{N_{H_2}}(x,s)dx = 2 \cdot \widetilde{N_{H_2}}(0,s) \cdot \left(\frac{D_{H_2}}{s}\right)^{\frac{1}{2}} \quad (7)$$

Using (4) and (7) to eliminate N_{H_2} and applying the inverse Laplace transform, one obtains the time-domain equation. The final result can be simplified to an equation with only physical parameters:

$$L^{-1}\left\{\sqrt{s} \cdot \widetilde{N_{IT}}(s)\right\} \cdot N_{IT}^2(t) = 2 \cdot \sqrt{D_{H_2}}\left(\frac{\sqrt{k_H}k_F}{k_R}N_0\right)^2 \quad (8)$$

In (8), the symbol $L^{-1}\{\cdot\}$ denotes the inverse Laplace transform. It can be alternatively written as a convolution form in the time domain:

$$\left(\frac{1}{\sqrt{t}} * \frac{dN_{IT}(t)}{dt}\right) \cdot N_{IT}^2(t) = 2\sqrt{\pi D_{H_2}}\left(\frac{\sqrt{k_H}k_F}{k_R}N_0\right)^2 = M(t) \quad (9)$$

The symbol "$*$" inside the brackets at the left side of (9) represents the convolution operator. At the right side, k_F is proportional to the inversion-hole density, the vertical electrical field and temperature. Parameters k_H, k_R and D_{H_2} are proportional to the temperature only, as shown in (10), in which E_R and E_D are constant parameters. So the right side of equation (9) is a function of stress voltage, temperature, oxide thickness and unit gate capacitance. Basically, they are a function of time and can be defined as $M(t)$.

$$\begin{cases} k_F \sim \sqrt{C_{ox}(V_{gs} - V_{th0})} \cdot exp\left(\frac{E_{ox}}{E_0}\right) \\ k_R \sim \exp\left(-\frac{E_R}{kT}\right) \\ D_{H_2} \sim \exp\left(-\frac{E_D}{kT}\right) \end{cases} \quad (10)$$

If the stress voltage and the temperature remain constant with regard to time, e. g. DC stress, $M(t)$ will be a constant and can be written as M. In this situation, (9) will degrade to the well-known closed-form solution for the number of interface traps N_{IT}:

$$N_{IT}(t) = R \cdot t^{\frac{1}{6}}. \quad (11)$$

In (11), R is a constant and can be expressed as

$$R = \left(\frac{M}{\left(\sqrt{\pi}\right)^3} \cdot 3 \cdot gamma\left(\frac{2}{3}\right) \cdot gamma\left(\frac{5}{6}\right)\right)^{\frac{1}{3}} = 0.94 \cdot M^{\frac{1}{3}} \quad (12)$$

where the *gamma* function has been employed [15].

However, if the stress condition changes with time, it will be difficult to derive a closed-form solution. An alternative way is to modify (9) into a discrete form and find an iterative solution. Suppose the timing points are separated uniformly by Δt seconds. The discretization of (9) can then be written as:

$$\left(\sum_{i=0}^{n-1} \frac{N_{IT}(i+1) - N_{IT}(i)}{\sqrt{\Delta t} \cdot \sqrt{n-i}}\right) \cdot N_{IT}^2(n) = M(n) \quad (13)$$

In (13), parameter n is the discrete time index. Rearranging (13) and using the solution of the so-called Cubic equation [16], the iterative solution for N_{IT} can be expressed as in Table I. The parameters b and d of (14) in Table I are given in (16) and (17) of Table I. $M(n)$ which is given in (15) and (18) of Table I is a function of time, stress voltage, temperature and other process parameters.

Table I: The new compact NBTI model with *uniform* time step Δt.

$$N_{IT}(n) = \begin{cases} 0 & n = 0 \\ \left(M(1)\sqrt{\Delta t}\right)^{\frac{1}{3}} & n = 1 \\ -\frac{b}{3} + \left(-\frac{b^3}{27} - \frac{d}{2} + \sqrt{\left(\frac{b^3}{27} + \frac{d}{2}\right)^2 - \frac{b^6}{729}}\right)^{\frac{1}{3}} + \left(-\frac{b^3}{27} - \frac{d}{2} - \sqrt{\left(\frac{b^3}{27} + \frac{d}{2}\right)^2 - \frac{b^6}{729}}\right)^{\frac{1}{3}} & n > 1 \end{cases} \quad (14)$$

$$M(n) = 0.94^{-3} \cdot A^2 C_{ox}\left[V_{gs}(n) - V_{th0}\right]\exp\left(-\frac{E_a}{2kT(n)}\right) exp\left(\frac{2E_{ox}}{E_0}\right) \quad (15)$$

$$b = \sum_{i=1}^{n} N_{IT}(i)\left(\frac{1}{\sqrt{n-i+1}} - \frac{1}{\sqrt{n-i}}\right) \quad (16)$$

$$d = -M(n)\sqrt{\Delta t} \quad (17)$$

$$E_{ox} = \frac{\left(V_{gs}(n) - V_{th0}\right)}{t_{ox}} \quad (18)$$

$$\Delta V_{th}(n) = \frac{q t_{ox}}{\varepsilon_{ox}} \cdot N_{IT}(n). \quad (19)$$

Table II: The new compact NBTI model with *non-uniform* time step Δt_n.

$$N_{IT}(n) = \begin{cases} 0 & n = 0 \\ \left(M(1)\sqrt{\Delta t_1}\right)^{\frac{1}{3}} & n = 1 \\ -\frac{b}{3} + \left(-\frac{b^3}{27} - \frac{d}{2} + \sqrt{\left(\frac{b^3}{27} + \frac{d}{2}\right)^2 - \frac{b^6}{729}}\right)^{\frac{1}{3}} + \left(-\frac{b^3}{27} - \frac{d}{2} - \sqrt{\left(\frac{b^3}{27} + \frac{d}{2}\right)^2 - \frac{b^6}{729}}\right)^{\frac{1}{3}} & n > 1 \end{cases} \quad (20)$$

$$b = \sum_{i=1}^{n} N_{IT}(i)\sqrt{\Delta t_n}\left(\frac{1}{\sqrt{\sum_{x=i}^{n}\Delta t_x}} - \frac{1}{\sqrt{\sum_{x=i+1}^{n}\Delta t_x}}\right) \quad (21)$$

$$d = -M(n)\sqrt{\Delta t_n} \quad (22)$$

The parameters of the equations in Table I are explained as follows. C_{ox} is the gate capacitance per unit area. $V_{gs}(n)$ is the stress voltage applied between gate and source, which may change with discrete time index n. V_{th0} is the unstressed threshold voltage, while t_{ox} is the equivalent oxide thickness (EOT) of the gate oxide. Constant k is the Boltzmann constant and $T(n)$ is the temperature in Kelvin at discrete time index n. Parameters A, E_0 and activation energy E_a are model fitting parameters which need to be extracted from NBTI degradation measurements. The actual threshold shift as function of time due to NBTI can be derived from $N_{IT}(n)$ as (19) in Table I, in which q is the charge of a single electron and ε_{ox} is the dielectric permittivity of the gate oxide.

Compared to other compact NBTI models, our compact model requires three fitting parameters, A, E_0 and E_a in Table I, which can be extracted from NBTI measurements. This is less than the seven parameters in [9] and ten parameters in [5].

In order to implement the model in Cadence ADE, the compact model needs to handle the Spectre transient simulation results, which is using non-uniform time steps [12]. Applying the same derivation approach, the compact model with non-uniform time steps is presented in Table II. Here, Δt_n is the specified time step between time point t_n and time point t_{n-1}. The expression of $M(n)$ is the same as provided in Table I.

4. Model evaluation

The compact model will be evaluated in two ways. First, since the model is actually a solution of the RD equations, the comparison with the RD theoretical solutions will be made. Second, the model will be validated with published silicon results.

4.1. Comparison with the RD theoretical solutions

It is difficult to get the closed-form solution of the RD equations except with the situation of DC stress, which is shown in expression (11) and (12). Our new model was implemented in Matlab and compared with the accurate closed-form solution under the same DC stress. The resulting threshold shifts are compared in Figure 2. The relative errors in percentage are shown in Figure 3. The timing points are separated by one second in both figures. Figure 3 shows that the maximum error is about 6.7% at the initial timing point. With the number of timing points increasing, the error reduces dramatically and converges to zero. So the error introduced by the time discretization can be neglected in the real case. This is because normally the number of the timing points will be large.

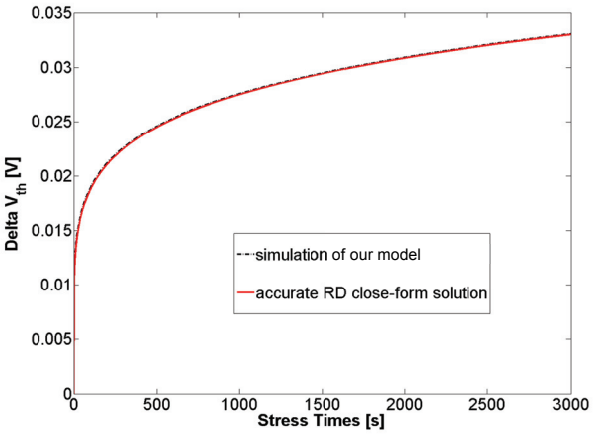

Figure 2: Comparison of our iterative solution with the closed-form solution (DC voltage-stressed situation).

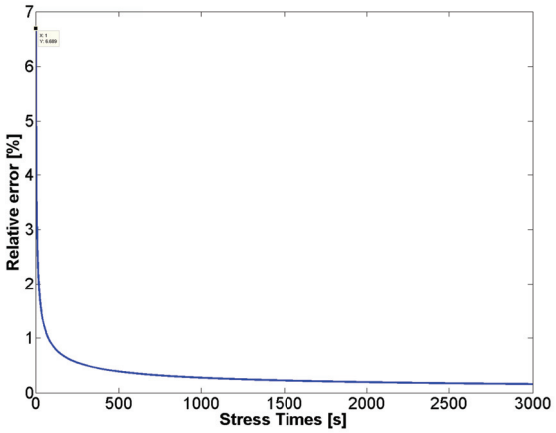

Figure 3: Relative error of our iterative solution in Figure 1 (DC voltage stressed situation).

Figure 4 shows the comparison between our model and one of the RD theory based models in [9] under the same square-waveform stress. Both models using the same parameter setting and the results match well. Since the RD equations are too difficult to be solved, paper [9] just provides solutions at two time points per square-wave cycle under the linear approximation. Compared to [9], our model can give the solution as detailed as possible, while the results are very accurate.

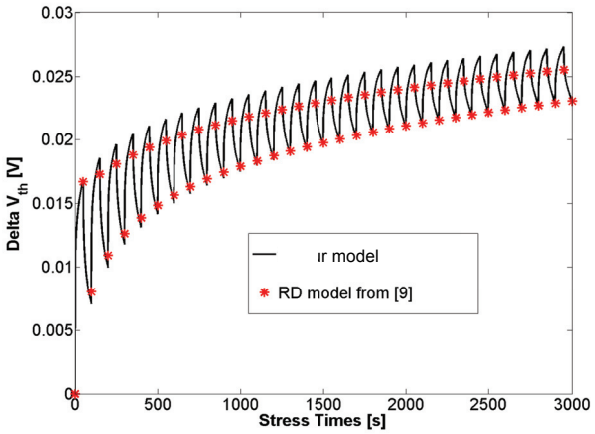

Figure 4: Comparison of our model with the model in [9] for square-wave voltage stress.

4.2. Comparison with the published silicon results

The RD theory for modelling NBTI degradation has been validated by silicon results in many publications [3], [6], [9], [13], [14], [17–19] using DC and square-wave stresses. Since our compact model use the same RD theory and has been validated by RD theoretical solutions in section 4.1, the published silicon data in [3], [6], [9], [13], [14], [17–19] can also be used to support our compact model under DC stresses and square-wave stresses. An example for a square-wave stress is shown in Figure 5, in which the compact model simulation results agree with silicon measurement data [19] under the square-wave stress.

In addition to DC stresses and square-wave voltage stresses, the compact model can handle more arbitrary stress waveforms, like sine-wave and triangular-wave stresses. They also need to be validated by silicon data. Unfortunately, there is only one publication [5] which shows the silicon measurement results for NBTI degradation under a triangular wave stress. No publication for NBTI under sine wave stresses could be found. Here the comparison under triangular-wave stress between the compact model simulation results and the measurement results from [5] are shown in Figure 6. The parameter settings are extracted from the model and measurements results in [5]. From Figure 6, it can be seen that the model correctly predicts the maximum degradation (up-limits) in each cycle, which is important for circuit life-time prediction. The degradation changes at stress-up and stress-down are also agreeing well with the measurements. However the parts which do not agree are the bottom parts in every cycle, which are predicted to increase faster by our

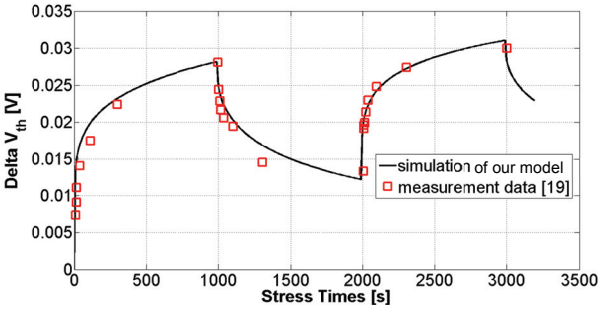

Figure 5: Comparison of our model with the measurement results [19] for square-wave stress.

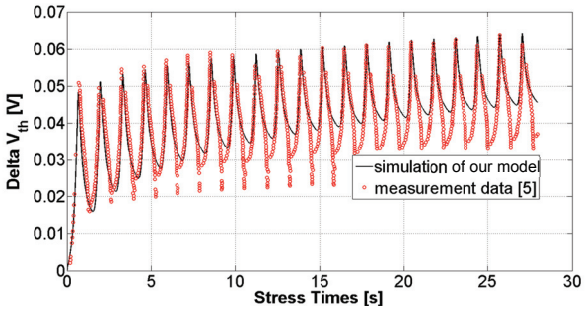

Figure 6: Comparison of our model with the measurement results [5] for triangle-wave voltage stress.

model than measurements shown. In fact, this kind of mismatch in the relax region has been reported for square-wave stress in many publications [10–12] and have become a hot research topic recently. However, based on the latest research, it can be explained by extra holes in addition to interface traps [3], [13], [14], The hole trapping/de-trapping will tend to saturate after around thousands seconds, and the long-time degradation will be dominated by interface-traps generation (RD theory).

5. Implementation in Cadence ADE

The compact model proposed in this paper can be easily incorporated with transient simulations in SPICE simulators. One problem could be the simulation time. In fact it is impossible to simulate several years in both transient and aging simulations. So the results need to be extrapolated to the required aging time from the short-time detailed simulations. The new compact model has the possibility to incorporate such an extrapolation because the trend of the degradation results in a simple power function of time. Hence a simulation strategy has been implemented in Cadence ADE using Verilog-A, which is shown in Figure 7.

The strategy will now be explained using the block numbers in Figure 7:

1) Transient simulation is carried out on a non-aged fresh netlist by Cadence Spectre.
2) With the stress voltage waveforms on each PMOS transistor obtained from Spectre, the detailed threshold degradation is calculated using the compact model in Table II .
3) Since both the transient simulation as well as the detailed degradation calculation are done in the time range of a few seconds, not for years, an extrapolation is required. For each PMOS transistor, there are only two parameters in the extrapolation function that need to be extracted from the detailed degradation simulation: A and n, as shown in Figure 7. These parameters are fitted using the least-square-error (LSE) method and stored in separated files.
4) The aged netlist is generated by adding a voltage source in series with the gate of each PMOS transistor to model the threshold degradations.
5) The value of each voltage source is calculated by the power function as shown in Figure 7 with the parameters from stored files. Now the aged netlist is ready to be used in any kind of simulation in Spectre with regard to a specified number of aging years.

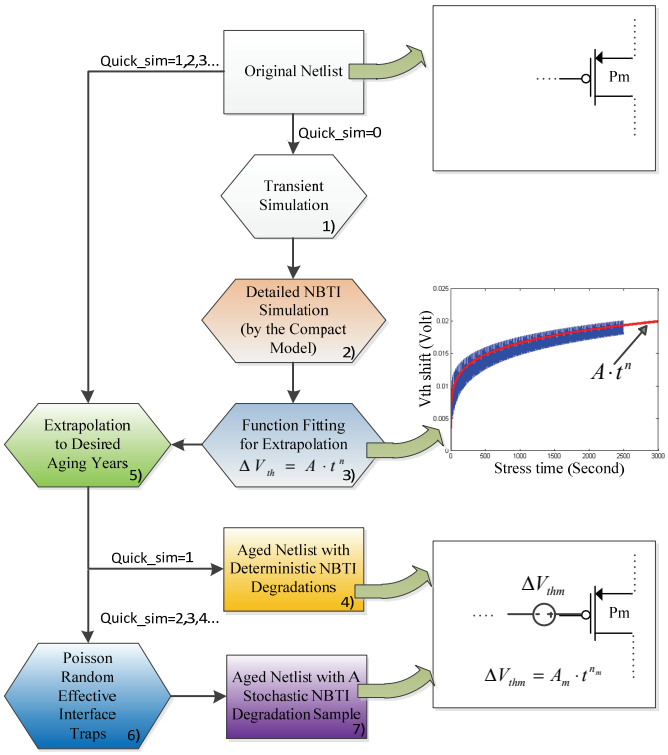

Figure 7: NBTI simulation strategy for analog/mixed-signal applications.

6) The stochastic effect of NBTI degradation is taken into account by randomizing the total effect interface traps under the gate area assuming a Poisson distribution [20]:

$$Var(N_{IT\_tot\_eff}) = Mean(N_{IT\_tot\_eff}) = \frac{Mean(\Delta V_{th}) \cdot \varepsilon_{ox} WL}{2.7 \cdot qt_{ox}} \quad (23)$$

7) The aged netlist with a stochastic NBTI degradation sample is generated using the same approach as 4). Except the threshold-voltage shift is now calculated from a sampled stochastic number of interface traps.

$$sample(\Delta V_{th}) = \frac{2.7 \cdot qt_{ox} \cdot sample(N_{IT\_tot\_eff})}{\varepsilon_{ox} WL} \quad (24)$$

The $Mean(\Delta V_{th})$ in expression (23) is the deterministic threshold degradation which is calculated by the model in Table I and II. The W and L are the transistor gate length and width. The constant 2.7 is used to take into account both the random number of interface traps and the random spatial distribution of the traps [20]. This is also the reason of the name "effect interface traps", $N_{IT\_tot\_eff}$. The $sample(\Delta V_{th})$ and $sample(N_{IT\_tot\_eff})$ in expression (24) are the stochastic samples.

The whole process in Figure 7 has been implemented using Verilog-A in Cadence ADE. A variable "*Quick_sim*" is used in ADE to determine the different choices: detailed NBTI simulation to extract power-function fitting parameters, deterministic threshold aging calculation, or stochastic threshold aging calculation. The parameter sweep for "*Quick_sim*" in ADE can be used to run a batch process, which makes the NBTI aging simulation very easy to combine with normal process variations in Mont-Carlo simulations.

Table III: The proposed compact model simulation times in Cadence ADE vs. Ref. [12].

Circuit	**Num. of PMOS**	**Stress waveform**	**Num. of time steps**	**Total time consumed** (including Transient simulation)
Opamp	11	Sine	55	0.888 seconds (this paper)
Single Test PMOS	1	Square	<100	Several minutes (Ref. [12])

The total simulation time is in the same order of Spectre transient simulations, which is much faster as compared to normal RD solvers, e. g. several minutes for only one PMOS transistor [12]. An example run on our server with one CPU core occupation is shown in Table III.

6. Conclusions

A compact NBTI model based on directly solving the RD equations has been proposed. The model can accurately handle arbitrary stress waveforms for the up-limits and is thus very suitable for analog/mixed-signal simulations. The model has been implemented in Cadence ADE with Verilog-A, and can simulate both deterministic as well as stochastic NBTI aging effects. The simulation speed is thousand times faster as compared to other RD based models. The model is validated by both original RD theory solutions and silicon measurement results.

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8. References

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