True Random Number Generation using Latency Variations of Commercial MRAM Chips

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Abstract—The emerging magneto-resistive RAM (MRAM) has considerable potential to become a universal memory technology because of its several advantages: unlimited endurance, lower read/write latency, ultralow-power operation, high-density, and CMOS compatibility, etc. This paper will demonstrate an effective technique to generate random numbers from energy-efficient consumer-off-the-shelf (COTS) MRAM chips. In the proposed scheme, the inherent (intrinsic/extrinsic process variation) stochastic switching behavior of magnetic tunnel junctions (MTJs) is exploited by manipulating the write latency of COTS MRAM chips. This is the first system-level experimental implementation of true random number generator (TRNG) using COTS toggle MRAM technology to the best of our knowledge. The experimental results and subsequent NIST SP-800-22 suite test reveal that the proposed latency-based TRNG is acceptably fast ($\sim 22Mbit/s$ in the worst case) and robust over a wide range of operating conditions. Index Terms—MRAM, TRNG, MRAM-based TRNG.

I. INTRODUCTION

True random number generator (TRNG) plays an important role in cryptographic applications such as random key generation, cryptographic nonces, session keys, one-time-pad, initial seeds of pseudo-random number generator (PRNG), challenges for authentication, hardware metering, etc. [1]-[3]. A TRNG translates random physical phenomena (i.e., physical entropy) into digital sequences. Thermal noise of resistors and capacitors [3], [4], meta-stability [5], [6], random telegraph noise in dielectrics [7], [8], oscillator jitter [3], [9], chaos [3], quantum phenomena [10], random spintronic [11]–[13] and memristive [14], [15] properties, atmospheric-, shot-, radio- and flicker-noise [2], [16], etc. are the most common high-quality physical entropy sources that are harvested to generate random numbers. Furthermore, the process variation during integrated circuits (ICs) fabrication is also responsible for random noise [17]. In most cryptographic applications, the quality of system's security relies on the quality of random numbers. A poor TRNG can always be a target to an adversary for attacking the whole system. A TRNG can be a discrete or an integral part of the system (e.g., on-chip TRNG). Usually, an on-chip TRNG has several advantages: low-overhead (area and energy), non-deterministic, high-throughput, simple design, robust against a wide range of operating conditions, etc.

Continual scaling down in technology introduces enormous challenges such as substantial process variation, crucial transistor's sensitivity with different operating conditions, significant power consumption, etc. to the existing memory chips. Current mainstream volatile memory chips, i.e., static RAM (SRAM) and dynamic RAM (DRAM), suffer from scalability, density, memory persistency, and leakage issues. On the other hand, existing non-volatile memory (NVM) chips (e.g., Flash) suffer from performance and endurance problems. Due to these limitations, existing memory chips are incompetent in delivering ever-increasing demands of power-efficient, smaller, and high-performance systems [18]. Thankfully, MRAM can turn into a dominant universal memory (cache and main memory) technology due to its promising scopes such as non-volatility, scalability, unlimited endurance, high speed, and fast read access, ultralow-power operation, CMOS compatibility, reliability, high density, thermal robustness, and radiation hardness [19]. Because of these advantages, most of the systems are expected to include

MRAM chips. Therefore, MRAM can be an attractive candidate for low-power TRNG.

There have been several high-quality and robust memorybased TRNGs, but most of them suffer from high-overhead and low-throughput [1], [3], [8], [20]–[22]. Therefore, several emerging memory-based TRNGs, capable of providing high density and throughput, have been proposed to overcome existing challenges [8], [12], [15], [22], [23]. Furthermore, MRAM-based TRNGs have gained attention because of their capability of generating significantly high quality and robust random numbers [12], [21], [24], [25]. However, the existing MRAM-based TRNGs are mostly simulation-based or need modification in standard MRAM structures [21], [25], [26]. Furthermore, some MRAM-based TRNGs can not be easily integrated into the existing computing system due to the strict requirement on operating conditions (e.g., precise control over current/voltage pulse width/magnitude/waveform). [12], [24], [27].

The previous contributions inspirit the need for real memory implementation and build the foundation of proposed MRAM-based TRNGs generated from COTS MRAM chips, which require minimal or no additional hardware, are robust against environmental fluctuations and provide considerably high throughput. In this work, we propose a technique of generating random numbers that meet the aforementioned requirements by exploiting write latency variations of COTS MRAM chips. In summary, the major contributions of this work are as follows.

- We reduce the write enable (\overline{W}) time from the manufacturer recommended value during the write operation to introduce errors. Errors from some of the cells at the reduced timing parameter are entirely random and can be used as a source of randomness. However, some of the cells exhibit deterministic behavior. Therefore, we further propose an algorithm to select the most suitable memory cells that exhibit proper randomness to generate robust and high-quality random numbers.
- We demonstrate the system throughput and robustness of our proposed TRNG in multiple COTS Everspin toggle MRAM chips ([28]) under a wide range of operating conditions.

The rest of the paper is organized as follows. Sect. II briefly overviews the organization and operating principle of MRAM chips. Sect. III presents the proposed technique of generating true random numbers, including cell characterization and suitable bit-selection algorithm. Sect. IV explains the experimental setup and exhibits obtained results to verify the quality and robustness of the proposed TRNG. Finally, Sect. V concludes the paper.

II. MRAM ARCHITECTURE AND OPERATION

Magnetic tunnel junction (MTJ) is the core element of toggle MRAM that uses the Savtchenko switching [29], [30] property by creating a rotating field with the sequential identical write current pulses to store both (high and low) data states. The bit cell of 1T-1MTJ MRAM architecture comprises two ferromagnetic layers separated by a thin dielectric tunnel oxide (AlOx or MgO) layer (shown in Fig. 1a). One layer's magnetic orientation is always fixed, known as the reference (or fixed) magnetic layer (RML). Depending on the magnetic field, another layer's magnetization can freely be oriented, and this layer is known as the free magnetic layer (FML). The FML is composed of NiFe synthetic antiferromagnet (SAF). The considerably higher magnetic anisotropy of RML compared to FML ensures stable magnetization direction of FML during memory (read/write) operation. Storing bits in the memory array is determined by the resistance states. When both the FML and RML are aligned in the same direction (current passed from SelectLine (SL) to BitLine (BL)), the MTJ produces low electrical resistance. On the other hand, when their magnetic field orientation is opposite, the MTJ exhibits high electrical resistance.

Writing bits in the magnetic field-driven toggle MRAM array requires passing a high write current (I_w) for changing FML's magnetic orientation [30]. The applied I_w to the write lines, placed on top and bottom of the MTJ devices (see Fig. 1a) creates an auxiliary magnetic field that changes FML direction. On the other hand, the direction of RML is strongly coupled with an anti-ferromagnet [30]. During the write operation, the memory circuit performs a pre-read operation to determine the state of the target bit and execute a toggle pulse (if required) to change the state of the bit if the desired state is not the same as the target state. Consequently, it reduces the overall power consumption and improves power efficiency. However, this increases the total write cycle time (including an additional read operation).

During the read cycle, a small bias voltage (far below the breakdown voltage of the device) is applied across the MRAM cell. Depending on parallel (R_{Low}) or anti-parallel (R_{High}) orientation, a current sensing circuitry (attached with the MRAM cell) experiences different current and latches the appropriate logic ('0' or '1') comparing with the reference resistance (R_{Ref}) shown in Fig. 1b. Fig. 1b illustrates the random resistance variation effect of the read circuitry of a larger-sized MRAM array. Those bits are considered acceptable if their statistical separation is greater than 5σ from the mean, where σ is the standard deviation. The accuracy of the read circuitry depends on determining the actual resistance state in the tail region (useable resistance change, ΔR_{Use}) of the distribution. For robust, less noise-sensitive, and high-speed read operation with normal process variation, large $\Delta \tilde{R}_{Use}$, and significantly more than 12σ separation are essential [30]. Furthermore, the width of resistance distribution varies from cell to cell because of manufacturing process variations. Besides, the quality, size, and level of in-homogeneity of the MTJ tunnel barrier have a significant impact on larger relative bit-to-bit resistance variation [30], [31]. Therefore, a thicker tunnel barrier ($\sim 1nm$) is essential to maintain the resistance level of the MTJ in the kilo Ω range for minimizing the series resistance effect from the isolation transistor [30], where Ω is the SI unit of resistance.

Storing data in a magnetic state has several benefits over charge-based storage such as non-destructive read operation, unlimited read/write endurance, no leakage during magnetic polarization, no wear-out due to no movement of electrons/atoms during the switching process of magnetic polarization [32], etc. Moreover, Savtchenko switching based MRAM arrays possesses several important performance characteristics such as lower write error rate and fast read/write cycle (35ns). They are also less sensitive to external fields, and therefore they are less sensitive to manufacturing process variations [33].

For all commercial memory chips, manufacturers define a set of timing parameters for reliable read/write operation of the chips against a wide range of operating conditions. The write operation of the MRAM chip can be governed by three different control parameters: write enable (\overline{W}) , chip enable (\overline{E}) , and upper/lower byte enable $(\overline{UB}/\overline{LB})$ signals. A simplified version of the write enable (\overline{W}) controlled write operation of the MRAM chip is shown in Fig. 1c.

Here,

 t_{WC} = write cycle time, i.e., the time period to complete full write operation in a particular address.

 t_W = write pulse width, i.e., the time period for which the \overline{W} pin is kept activated.

 t_{WR} = write recovery time, i.e., the time to complete the write operation after the \overline{W} pin is deactivated.

 t_{DV} = valid data to end of write, i.e., the time for which the valid data need to be available in the data I/O before the \overline{W} pin is deactivated.

If the output enable (\overline{G}) becomes active at the same time, or after \overline{W} is activated, the output will remain in the high impedance state. After all three write control parameters $(\overline{E}, \overline{W}, \text{ or } \overline{UB}/\overline{LB})$ become disabled, the \overline{G} signal must remain in the steady-state high for at least 2ns. Reducing any of these timing parameters can improve the speed and reduce power consumption but may lead to faulty operation. The write timing parameter t_W is manipulated in this work to introduce errors during \overline{W} controlled write operation.

III. GENERATING RANDOM NUMBERS USING COTS MRAM

In our proposed methodology, we exploit the random Savtchenko switching at the reduced (manufacturerrecommended) timing parameter for generating true random numbers. When the write pulse width, t_W , of toggle MRAM (see Fig. 1c) is reduced, it does not get sufficient time and write current to toggle into the desired stable state. Due to the process variation and the non-uniform distribution of current pulse within the chip, random variations are created in the MTJ storage element. Therefore, all of the memory cells are not capable of performing an appropriate write operation. That is the reason that a manufacturer specifies a set of timing parameters for reliable read/write operations. Violation in any of these manufacturerrecommended timing parameters may cause erroneous/faulty outputs during the read/write operation. If the t_W is not sufficient, there is a chance that FML is not aligned perfectly with the RML (either the same or in the opposite direction) and might settle on an intermediate position. This arrangement may lead the cell resistance to be halfway between R_{Low} and R_{High} [34]. Therefore, at reduced t_W , if the resultant cell resistance falls around the ΔR_{Use} region of the resistance distribution (see Fig. 1b) curve, the cell will show indeterministic characteristics and generate random bits.

In our proposed scheme, several steps are involved in generating true random numbers. At the reduced t_W , MRAM chips create errors, and the total number of errors differ at different reduced t_W values. At first, we select the most suitable reduced t_W value. This selected t_W aims to maximize the number of cells that can be used for TRNGs. Second, we propose a cell selection algorithm to characterize all of the temporally unbiased MRAM cells from a set of measurements to identify the most appropriate memory cells for generating robust random numbers. The mentioned two steps must be performed only once to choose the appropriate number of random MRAM cells. Finally, we collect data from multiple measurements from the selected MRAM cells and use a low-overhead post-processing technique to generate high-quality random numbers.

A. Appropriate Reduced Time Selection

The experimental results show that some of the memory cells provide erroneous outputs if the data is written at the reduced timing parameters. The number of these error-prone cells varies within the write pulse activation time range $t = [0, t_W]$. We change the t_W and count the total number of erroneous bit cells. Our main objective is to find a suitable t_W for which the maximum number of erroneous bits is achieved. The number of erroneous cells is calculated from all achievable reduced write timing parameters in the next step. Finally, we propose an algorithm to characterize the memory cells among those



Fig. 1: (a) Toggle MRAM cell structure with MTJ. (b) Schematic representation of Gaussian resistance (R_{Low} and R_{High} states) distribution of larger-sized MTJ array [30], and (c) Write enable (\overline{W}) controlled write cycle of MRAM chip.

erroneous cells to generate random numbers for any system using the timing parameter for which the maximum number of random cells is obtained. Details about the cell characterization technique are described in Sect. III-C.

B. MRAM Cells Characterization

Our experimental result manifests that all of the memory cells are not suitable to generate robust random numbers. To locate these random cells, at first, we characterize MRAM memory cells by writing different intuitive (solid) and nonintuitive (random, checkerboard, and striped) input data patterns to the entire memory cells at the reduced write enable time, t_W , and read back the full memory contents with appropriate timing parameters a total of N times. Larger N provides better characterization results but increases the computation time for characterization.

Theoretically, reduced write operation reduces the current flowing through the MTJ storage elements [35]. Hence, the magnetic orientation switching (parallel (P) \rightarrow anti-parallel (AP) or vice versa) time increases significantly [35]. Switching from P to AP is more vulnerable to reduced write operation due to enhanced switching delay, leading to the write failure. Our experimental results also manifest that the write operation at the reduced t_W produces erroneous data. Moreover, these error patterns depend on the input data pattern to be written and vary with different memory chips. Based on the error patterns from the sample measurements, the MRAM cells can be classified into the following two categories-

Persistent Cells: These cells produce stable output from measurement to measurement. These stable cells are excellent candidates to generate memory-based Physically Unclonable Function [24], [25] but not competent for true random number generation because of manifesting consistent behavior at the reduced t_W .

Noise-prone Cells: These cells provide inconsistent output for different measurements. However, we also observe that most noise-prone cells are biased toward '0' or '1'. Therefore, to avoid producing deterministic random numbers, we propose a cell selection technique to exclude those biased cells from the noise-prone cells (described in Sect. III-C).

C. Appropriate Cell Location Selection

To generate a robust TRNG, unbiased cells need to be filtered because all cells do not provide the same amount of entropy. At first, we discover all erroneous cells at the reduced t_W from (N) measurements. At the reduced t_W , some cells will not create any errors; we define them as the correct state (S_C). On the other hand, the other cells will create erroneous outputs; we define them as the error state (S_E). Next, we record the change of state $(\mathcal{S}_C \to \mathcal{S}_E \text{ or } \mathcal{S}_E \to \mathcal{S}_C)$ or flip of all cells comparing to the two consecutive measurements from each of N measurements. This forms a $(1 \times M)$ array containing the total number of flips in each cell location from N measurements, where M is the total number of memory cells. Second, to select the random cells, we need to determine the appropriate threshold, Th. Theoretically, the expected value of Th is $p \times (N-1)$, where $p (=\frac{1}{2})$ is the probability of state change (flip). However, in reality, a fixed Th might not provide sufficient random cells. Hence a specified bound $(Th_L \leq Th \leq Th_U)$ needs to be defined, where Th_L and Th_U are the lower- and upper-bound of the threshold range. Cells within this boundary are considered as TRNG candidates. The silicon results show that the obtained random cells above Th_U are significantly negligible. Therefore, we only choose those cells for which the $(1 \times M)$ array contents are above Th_L . The locations of these unbiased noisy cells are stored in data-set \mathcal{F}_C . The step-by-step procedure is shown in Algorithm 1. A true random number must be highly temporal variant, which is the basis of our proposed algorithm. Therefore, the selected random cells with the proposed algorithm are capable of generating high-entropy random numbers.

Algorithm 1 Pseudo-code for Random Cell Location Selection

- **procedure** $rand_cell_loc(N, input_data, Th_L)$
- 1: /* N = Number of total measurements */
- 2: /* $input_data = (1 \times num_cell)$ matrix containing input data stored to each memory cell at reduced $t_W^*/$
- 3: /* Th_L = Lower threshold bound to choose true random cells */
- 4: *num_cell* = Total number of memory cells
- 5: /* *flip_count* matrix stores total number of state change (flip) from consecutive N measurements */
- 6: $flip_count = zeros(1 \times num_cell)$
- 7: for i = 1 to N 1 do
- $x = bitwise_xor(input_data(i), input_data(i+1))$ 8:
- $flip_count = bitwise_add(x, flip_count)$ 9:
- 10: end for
- 11: /* rand loc matrix stores random cell locations */
- 12: $rand_loc = zeros(1 \times num_cell)$
- 13: $num_randcell = 0$ /* Total number of random cells */
- 14: for i = 1 to num_cell do
- if $flip_count(i) \ge Th_L$ then $rand_loc(i) = 1$ 15:
- 16:
- $num_randcell + +$ 17:
- end if 18:
- 19: end for

20: return rand_loc

end procedure

D. Low-overhead Post-processing

However, the raw random sequence that apparently seems unbiased might provide biased results under extreme operating conditions. Therefore, several post-processing techniques such as Von Neumann corrector, XORing multiple bits, cryptographic hash function, etc. are used to generate a fully non-deterministic random sequence [36]. Secure Hash Algorithm (SHA)-256 is area efficient, fast, and fewer input bits are required to generate the same entropy level [37], [38]. Therefore, we chose SHA-256 as a post-processing technique and applied over the bit sequence obtained from \mathcal{F}_C . To generate a random number of the required length, at first, we accumulate the obtained random cells at the selected reduced t_W . The value of the measurements is a function of the required length and the used post-processing technique. Next, the bit sequence is split into appropriate chunks to feed into the SHA-256 hash algorithm. Finally, the multiple output chunks gathered from the SHA-256 hash function are concatenated to produce truly unbiased random numbers and are denoted as \mathcal{H}_C .

IV. EXPERIMENTAL RESULTS AND ANALYSIS

The primary analysis is performed over ten (2 chips from each MR0A16ACYS35, MR0A16AYS35, MR1A16AYS35 MR2A16ACYS35, MR2A16AYS35 models) 16-bit parallel interfaced differently sized (1Mb-4Mb) memory chips manufactured by Everspin technologies. Among them, five chips are selected randomly to perform extensive analysis for TRNG. We have used our own custom memory controller implemented on Xilinx Artix 7 (XC7A35T-1C) FPGA to manipulate different timing latency of a couple of emerging memories [39]. As discussed in Sect. III-B, the generated error is pattern dependent at reduced operation. Hence to determine the suitable pattern that is capable of generating high-entropy true random numbers, we collected a total of 5-set measurement data with seventeen different intuitive (solid) and non-intuitive (random, checkerboard, and striped) 16bit input data patterns: (0xFFFF, 0xAAAA, 0x5555, 0x0000) from each ten memory chips. We observed that the *solid* 0x0000pattern produces comparatively high erroneous bits than other patterns. Therefore, we can conclude that parallel (anti-parallel) configuration is the logic state '1' (state '0'). Next, to characterize the MRAM cells (discussed in Sect. III-B), we collected a total of 50-set measurement data with only solid 0x0000 input pattern from the selected five memory chips. We chose the smallest possible achievable (due to experimental limitation) value of t_W , 16.6% of the recommended t_W , for this work. However, our selected value of t_W can generate a sufficient number of incorrect outputs to generate high-quality random numbers.

A. Selection of t_W

To compare the behavior of the faulty/erroneous outputs at different reduced t_W values using *solid* 0x0000 data pattern, an analysis is performed to determine the cell types (i.e., noisy or persistent). We reduce the t_W value from 15ns (manufacturer's recommended) to 10ns, 5ns, and 2.5ns, respectively. Due to the experimental set-up limitations, we are incapable of reducing the t_W value any further. At $t_W = 5ns$ and 10ns, the obtained total failed bits are almost negligible (< 5% and < 1%, respectively) for all ten chips. However, at $t_W = 2.5ns$, the total number of failed bit count falls within 25.59% - 37.30%, which is sufficient for TRNG analysis. Hence, we choose $t_W = 2.5ns$ (considering the number of failed bit count) to characterize erroneous cells.

B. Characterization of Temporally Unbiased Cells

The MRAM cell characterization is performed according to Sect. III-C with N = 50 measurements. Table I shows a summary of random MRAM addresses and cells after performing cell characterization. The results show that the total number of random cells obtained at reduced t_W (2.5ns) varies from chip to chip. The results also show that different memory modules may have different thresholds. We also observe that only a few addresses hold these random cells. In Table I, the first row shows the cell selection threshold, Th_L , used for different chips. As we need to perform characterization so different thresholds for different models will be acceptable- the reason for choosing different thresholds to ensure higher throughput. However, the same threshold is used for the same model, i.e., C1 & C2 are from the same model. We can determine a unique threshold for simplicity for all models considering the highest threshold value (in our case, 23); however, at that point, we will get lower throughput as a lower threshold provides higher throughput (see Sect. IV-E). The second row represents the percentage of addresses that contain random cell(s). Note that we only consider those addresses which have at least one cell that lies into \mathcal{F}_C . As the percentage of random addresses is very small (~ 1%) regardless of memory size, we will need to store only those few memory cells' information. Finally, the last row presents the average number of random bits per random addresses.

TABLE I: Cell statistics after applying cell characterization algorithm.

Sample Chip ¹	C1	C2	C3	C4	C5
Threshold (Th_L)	16	16	15	23	21
#(Rand Addr) (%)	1.16	1.5	1.23	0.63	0.94
#(Rand Bits)/#(Rand Addr)	9.71	10.71	13.19	11.39	12.76



Fig. 2: The characteristics of memory cells of C4: most of the cells are purely invariant (stuck at '0'/'1').

Fig. 2 illustrates the number of flips ($S_C \rightarrow S_E$ or $S_E \rightarrow S_C$) of memory cells with N = 50 temporal measurements for a randomly chosen memory chip. Solid 0x0000 is used as the write data pattern. Note that to erase the trace of previously written data, we reset the entire memory with the solid 0xFFFFdata pattern before every measurement. The results show that a larger number of cells ($\sim 40 - 60\%$) are purely invariant (stuck at '0'/'1'logic state), which is not desirable for highentropy random number generator. To filter out those temporally persistent cells using the proposed algorithm (described in Sect. III-C), we only chose those cells (set \mathcal{F}_C) that are above the lower threshold range $Th_L = [15, 23]$ (see Table I) for different chips used in the experiment. Although the number of eligible cells decreases after performing our proposed cell selection algorithm, the filtered cells are enough to generate high-quality random numbers.

C. Evaluation

Data collected from different FPGAs verify that the memory controllers do not influence the randomness of the generated random number from MRAM chips. Furthermore, to evaluate the quality, randomness, and effectiveness of the obtained binary sequence, set \mathcal{H}_C (after performing low-overhead postprocessing technique, as discussed in Sect. III-D, over the test data sequence), the most frequently used and well-accepted NIST statistical test suite (STS) [40] is used. Tables II and III show the worst-case (i.e., from multiple similar test categories, the worst one is exhibited) NIST test results considering different memory models and extreme operating conditions. In the tables, the higher p-value $(\mathcal{P} - val.)$ (calculated from the chi-squared (χ^2)) test) indicates a purely random sequence and vice versa. Besides, *Prop.* is the proportion of the binary sequence that passes the corresponding test. However, for passing the randomness test, the minimum value of $\mathcal{P} - val$. should be 0.0001, and *Prop*.

¹C1&C2: MR0A16ACYS35, C3: MR0A16AYS35, C4: MR2A16ACYS35, C5: MR2A16AYS35

Sample Chip	C1		C2		C3		C4		C5	
Result Type	$\mathcal{P}-val.$	Prop.								
Frequency	0.122325	14/14	0.637119	20/20	0.141256	21/21	0.534146	11/12	0.991468	20/20
BlockFrequency	0.350485	14/14	0.350485	20/20	0.980883	21/21	0.534146	12/12	0.834308	20/20
CumulativeSums	0.066882	14/14	0.275709	20/20	0.105618	21/21	0.350485	11/12	0.534146	20/20
Runs	0.213309	14/14	0.637119	20/20	0.311542	21/21	0.534146	12/12	0.437274	20/20
LongestRun	0.066882	14/14	0.534146	19/20	0.392456	21/21	0.739918	12/12	0.122325	20/20
Rank	0.534146	14/14	0.275709	19/20	0.875539	21/21	0.739918	12/12	0.534146	20/20
FFT	0.534146	14/14	0.275709	20/20	0.105618	21/21	0.350485	12/12	0.534146	19/20
NonOverlappingTemplate	0.017912	12/14	0.122325	18/20	0.311542	19/21	0.213309	11/12	0.350485	18/20
OverlappingTemplate	0.213309	14/14	0.275709	20/20	0.021262	21/21	0.534146	12/12	0.275709	20/20
Universal	0.017912	14/14	0.739918	20/20	0.311542	21/21	0.213309	12/12	0.637119	18/20
ApproximateEntropy	0.035174	14/14	0.637119	20/20	0.585209	21/21	0.213309	12/12	0.017912	20/20
RandomExcursions	0.991468	10/12	0.213309	11/12	0.534146	11/12		7/7	0.006196	13/13
RandomExcursionsVariant	0.017912	11/12	0.017912	11/12	0.122325	11/12		6/7	0.048716	12/13
Serial	0.350485	13/14	0.739918	19/20	0.105618	21/21	0.350485	12/12	0.437274	19/20
LinearComplexity	0.350485	14/14	0.534146	20/20	0.689019	21/21	0.739918	12/12	0.534146	20/20
*NB —- test not performed due to insufficient data [40]										

TABLE II: The worst-case NIST test results at the reduced t_W .

needs to be greater than a specified value, which depends on the number of sample sizes (i.e., minimum of 18 tests need to be passed for 20 binary test sequences). The proposed MRAMbased binary sequences pass all (15) of the NIST tests; thus, it can be considered purely random.

D. Robustness Analysis

Chip Variations: The silicon results from four different memory models of two different sizes show that our proposed TRNG is robust. However, the statistics of random cells are different for different memory models, shown in Table I. These sources of variations come from architectural as well as both inter- and intra-chip dissimilarities. As the random process variation is the key source of any memory chips' randomness, the proposed scheme can generate random numbers.

Environmental Variations: Robustness against a wide range of operating conditions is one of the requirements of high-quality TRNGs. To verify the robustness of our proposed random number under temperature variation and external magnetic field (M-Field), we collected four sets of test data sequence at different operating conditions: i) room temperature $(26^{\circ}C)$, ii) high temperature $(65^{\circ}C)$, and iii) low temperature $(20^{\circ}C)$ without external M-Field. The fourth set is collected at room temperature with an $\sim 8mT$ external M-Field. The temperature range is chosen within the manufacturer's recommended value, which is $[0^{\circ}C - 70^{\circ}C]$ for all memory models. The total number of random cells is observed comparatively less for low temperatures than the other operating conditions. The write latency of MRAM increases significantly at the lower temperature, which results in the reduction of the number of random cells at the reduced write operation [31]. Besides, we applied a constant rare earth magnetic source (generated from the permanent magnet) in six different orientations of 3D coordinates to observe the effect of external M-Field. However, we did not notice any significant change in the total number of random cells with (8mT) external M-Field. Therefore, we can conclude that our proposed random numbers are robust against extreme operating conditions. To further evaluate the robustness of the cell selection threshold, we deliberately select those two models (C3 & C4) with the lowest and highest Th_L values (see Tables I and III). Table III shows the worst-case NIST STS results in extreme operating conditions, signifying that our proposed TRNG can produce high-quality random numbers.

E. Throughput Analysis

Cell characterization and registration are performed once during a full life cycle. Therefore, the registration phase is not considered during throughput calculation. The TRNG throughput of our proposed technique is the function of the average time required to perform read/write operation from one memory cell at the reduced t_W and the average time required to execute the SHA-256 hash function. The throughput of our proposed TRNG is calculated as follows:

$$\mathcal{T}_{avg,worst} = \frac{\mathcal{D}_{len}}{t_{RW,avg} + t_{hash,avg}} \tag{1}$$

where,

$$\boldsymbol{t}_{RW,avg} = \frac{\boldsymbol{t}_{RW} \times \mathcal{B}_{len}}{\left(\frac{\#RandBits}{\#RandAddr}\right)}$$
(2)

Here, $\mathcal{B}_{len}(=512\text{-}bit)$ and $\mathcal{D}_{len}(=256\text{-}bit)$ are the length of the input and hashed output (message digest) block size of the hash function, respectively, $t_{hash,avg}$ is the average time required to hash the input bit sequence of length \mathcal{B}_{len} , $t_{RW,avg}$ is the average time required to generate raw random bits of size $\mathcal{B}_{len}, t_{RW}$ is the average time required to perform a complete read/write operation from one memory address, and '#(Rand Bits)/#(Rand Addr)' (see Table I) is the average number of random bits per random addresses. The cryptographic hash function, SHA-256, is used in this work due to the low-overhead post-processing. Nowadays, almost all modern processors have dedicated instruction set architecture to provide hardware support for performing the secure hash algorithm [37]. We found $t_{hash,avg} = 802.6ns$ using Intel i7-8700 processor. Note that we use a high-level language (Python API) to hash the complete 512-bit block message; hence, the obtained average time (802.6ns) includes the function overhead. Ideally, MRAM has a comparatively fast (35ns) read/write cycle considering the nominal operation [28]. However, using our evaluation board, the obtained t_{RW} considering reduced write operation is 239.76ns (much higher than 70ns), which signifies the inclusion of the communication overhead between the FPGA interfaced with a computer to acquire the data from memory for analysis. Furthermore, Table I shows the different '#(Rand Bits)/#(Rand Addr)' values for different memory chips. According to Eq. 1, our system-level worst-case throughput values are around 18.17, 19.95, 24.12, 21.10, and 23.47 Mbit/s for C1 - C5 chips, respectively, considering all of the communication and function overhead. The obtained throughput values are significantly higher compared with the performance of many popular (non) volatile memory-based TRNGs [2], [20], [23]. An efficient implementation of a memory controller can further improve the overall performance of our proposed TRNG.

V. CONCLUSION

This paper demonstrated an efficient technique to generate high-throughput and high-quality true random numbers from

Sample Chip	C3						C4						
Operating Condition	$T_{High}(65^{\circ}C)$		$T_{Low}(20^{\circ}C)$		M-Field $(8mT)$		$T_{High}(65^{\circ}C)$		$T_{Low}(20^{\circ}C)$		M-Field $(8mT)$		
Result Type	$\mathcal{P}-val.$	Prop.	$\mathcal{P}-val.$	Prop.	$\mathcal{P}-val.$	Prop.	$\mathcal{P}-val.$	Prop.	$\mathcal{P}-val.$	Prop.	$\mathcal{P}-val.$	Prop.	
Frequency	0.788728	21/21	0.585209	21/21	0.242986	21/21	0.739918	12/12	0.534146	12/12	0.122325	11/12	
BlockFrequency	0.311542	20/21	0.585209	21/21	0.392456	21/21	0.534146	12/12	0.739918	11/12	0.066882	12/12	
CumulativeSums	0.078086	21/21	0.105618	21/21	0.311542	21/21	0.213309	12/12	0.002043	12/12	0.017912	10/12	
Runs	0.689019	21/21	0.875539	21/21	0.392456	21/21	0.122325	12/12	0.739918	12/12	0.213309	12/12	
LongestRun	0.311542	21/21	0.242986	21/21	0.242986	20/21	0.213309	12/12	0.008879	12/12	0.066882	12/12	
Rank	0.311542	21/21	0.186566	21/21	0.057146	21/21	0.122325	11/12	0.534146	12/12	0.534146	12/12	
FFT	0.585209	21/21	0.392456	21/21	0.186566	21/21	0.911413	12/12	0.000439	11/12	0.122325	12/12	
NonOverlappingTemplate	0.311542	19/21	0.186566	19/21	0.242986	19/21	0.008879	11/12	0.017912	11/12	0.122325	11/12	
OverlappingTemplate	0.242986	21/21	0.392456	20/21	0.585209	21/21	0.350485	12/12	0.213309	12/12	0.008879	11/12	
Universal	0.689019	20/21	0.875539	20/21	0.242986	21/21	0.350485	11/12	0.739918	12/12	0.534146	12/12	
ApproximateEntropy	0.141256	20/21	0.141256	20/21	0.029796	21/21	0.534146	12/12	0.213309	11/12	0.911413	12/12	
RandomExcursions	0.004301	14/14	0.066882	12/12	0.066882	11/12		9/9		6/7		5/5	
RandomExcursionsVariant	0.213309	13/14	0.066882	11/12	0.213309	11/12		9/9		6/7		4/5	
Serial	0.392456	21/21	0.392456	20/21	0.186566	21/21	0.350485	12/12	0.213309	11/12	0.350485	12/12	
LinearComplexity	0.311542	20/21	0.057146	21/21	0.186566	21/21	0.534146	11/12	0.035174	12/12	0.213309	12/12	

TABLE III: The worst-case NIST test results verify the robustness of our proposed TRNG.

*NB. --- test not performed due to insufficient data [40].

non-volatile COTS MRAM chips by utilizing its internal write latency variation. The NIST SP-800-22 suite results validate that our proposed technique is purely random and robust at extreme operating conditions. The throughput is also considerably higher than most of the available TRNG techniques implemented using existing or emerging volatile or NVM chips.

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