Metal Inter-layer Via Keep-out-zone in M3D IC: A Critical Process-aware Design Consideration (Accepted in ISQED 2023)

Madhava Sarma Vemuri Department of Electrical and Computer Engineering North Dakota State University Fargo, North Dakota 58105 Umamaheswara Rao Tida Department of Electrical and Computer Engineering North Dakota State University Fargo, North Dakota 58105

Abstract-Metal inter-layer via (MIV) in Monolithic threedimensional integrated circuits (M3D-IC) is used to connect interlayer devices and provide power and clock signals across multiple layers. The size of MIV is comparable to logic gates because of the significant reduction in substrate layers due to sequential integration. Despite MIV's small size, the impact of MIV on the performance of adjacent devices should be considered to implement IC designs in M3D-IC technology. In this work, we systematically study the changes in performance of transistors when they are placed near MIV to understand the effect of MIV on adjacent devices when MIV passes through the substrate. Simulation results suggest that the keep-out-zone (KOZ) for MIV should be considered to ensure the reliability of M3D-IC technology and this KOZ is highly dependent on the M3D-IC process. In this paper, we show that the transistor placed near MIV considering the M1 metal pitch as the separation will have up to $68,668 \times$ increase in leakage current, when the channel doping is $10^{15} cm^{-3}$, source/drain doping of $10^{18} cm^{-3}$ and substrate layer height of $100 \ nm$. We also show that, this increase in leakage current can also be reduced significantly by having KOZ around MIV, which is dependent on the process.

I. INTRODUCTION

Monolithic three-dimensional integrated circuit (M3D-IC) technology offers a promising solution to meet future computational needs. The need for M3D-IC technology arises since the conventional 2D-IC technology is limited by lithography and power constraints, whereas conventional threedimensional integrated circuit (3D-IC) technology enabled by die stacking is limited by the through-silicon-via (TSV) size [1]–[4]. The substrate layers in M3D-IC technology are realized by sequential integration. These layers are connected by metal inter-layer via (MIV), which are of the same size as logic gates [5]. This reduction in MIV size compared to the TSV has become possible by reduction in via height through sequential integration. However, to ensure the stability of the devices at the bottom layer, the top layers of M3D-IC should be processed below 500° C [6]–[9] which limits the M3D-IC process such as doping concentrations.

MIVs are realized by metal surrounding oxide to provide electrical insulation to the substrate. However, this realization also forms metal-insulator-semiconductor (MIS) structure, and hence MIV can affect the substrate region around it [10], [11]. Therefore, the impact of MIV on the transistors around it should be studied to ensure the reliability of M3D-IC implementations. To the best of authors' knowledge, there are no commercial ICs with the defined M3D-IC process specifically doping concentration of top layers, substrate layer height and MIV thickness. Therefore, the process parameters for the IC design should be considered to understand the MIV impact on the devices around it.

In this work, we systematically studied the impact of MIV on the adjacent devices and the simulation results suggest that the transistor placed near MIV considering the M1 metal pitch as the separation will have up to $68,668 \times$ increase in leakage current specifically when the channel doping is 10^{15} cm⁻³, source/drain doping of 10^{18} cm⁻³ and substrate layer height of 100 nm. This impact can be reduced by increasing the keep-out-zone (KOZ) for MIV and this KOZ is highly dependent on the process parameters of M3D-IC technology. Therefore, process-aware KOZ is required to ensure the reliability of M3D-IC design.

The organization of the rest of the paper is as follows: Section II discusses about the background and previous works on M3D-IC technology and the motivation of this work. Section III demonstrates the impact of MIV on different transistor placement scenarios. Section IV investigates the process parameters influence on the transistor operation when MIV is placed at M1 metal pitch separation to the transistor. Section V discusses the need for process-aware Keep-out-zone (KOZ) for the MIV, and KOZ values for different process parameters are presented. Section VI brings up the future directions for current work. The concluding remarks are given in Section VII.

II. BACKGROUND AND MOTIVATION

In M3D-IC technology, the top-layer devices should be processed sequentially under low-temperatures i.e., less than 500^{0} C to ensure the quality of bottom-layer devices [6]–[9]. With this sequential integration, the substrate layers are thinned down below 100nm thickness using layer transfer process [12]. With thin substrate and thin inter-layer dielectric (ILD), the metal inter-layer via (MIV) that connects devices

at two different layers has the height of 100nm - 500nm. This reduction in height helps us to reduce the MIV thickness significantly thus allowing high MIV density (> $10^8 MIV/cm^2$) [13]. Recent works from CEA-LETI focus on sequential layer integration at lower temperatures and measured the device characteristics on both top and bottom layers with different integration techniques specifically Fully Depleted Silicon On Insulator (FDSOI) transistors [14], [15]. Several works on the M3D integration focuses on the partitioning, placement and routing in Monolithic 3D integration considering different toplayer device technology specifically bulk [16], [17] or FDSOI [15], [18]. Monolithic 3D-FPGA is designed using thin-filmtransistors (TFT) in the lop layer [19]. [20] have used the unique structure of recessed-channel-transistors in top laver to study its performance. Some M3D-IC based open libraries are available currently. [16], [17] use conventional CMOS technology to present 45nm library for M3D integration. [18] have studied the power benefit of M3D-IC using FinFET based 7nm technology node. Although several demonstrations of M3D-IC process are performed, there are no existing commercial industry standards [21].



Fig. 1: 2-Layer M3D Process used in our work

In this work, we focus on the SOI devices on the top layer with thin substrate layer of up to 100 nm thickness as suggested by previous works [12]. One of the major benefit of M3D-IC technology is to allow heterogeneous integration. This M3D-IC process will also consider the substrate biasing at the top-tier and hence tuning the threshold voltage of the transistor for analog and digital applications similar to the conventional MOSFET. The two-layer M3D process assumed in this work is shown in Figure 1. With this consideration, the MIV passes through the substrate and essentially forms a metal-insulator-semiconductor (MIS) structure. Therefore, the impact of MIV on the adjacent devices should be studied since this MIS structure can interact through the substrate region around it. The rest of the paper will systematically study the impact of MIV on the adjacent devices considering the orientation of the channel with respect to the MIV.

III. MIV EFFECT ON TRANSISTOR OPERATION

MIV with substrate around it forms a metal-insulatorsemiconductor (MIS) structure, and essentially works like a MOS capacitor [10], [11]. If there is a p-type substrate region around MIV then it can be inverted (or form an n-type region) when carrying high voltage. This effect of MIV is shown in Figure 2, where the substrate around MIV will become n-type region if a higher voltage is applied to the MIV because of the MIS structure. The extent of this inversion region depends on the voltage of MIV and the M3D-IC process. If there is an n-type transistor placed near MIV, then this effect should be considered since there is a possibility of forming resistive region between source and drain, or source/drain and MIV. Therefore, an n-type transistor placed near MIV can have significant impact on its characteristics.



Fig. 2: MIV interacting with adjacent device

In this section, we study the MIV affect on transistor operation by systematically investigating two scenarios of MIV placement with respect to the transistor and is as follows:

- Vertical placement MIV is placed parallel to the transistor as shown in Figure 3.
- Horizontal placement MIV is placed beside the transistor as shown in Figure 7.

These scenarios are modeled using Sentaurus Technology Computer Aided Design (TCAD) software. We used Boron (B) as p-type substrate material, where carrier behavior is modeled with Shockley-Read-Hall (SRH) recombination model and Fermi-based statistics. The source/drain regions of the transistor is doped with Arsenic (As) (n-type) material using Gaussian profile concentration. The substrate terminal is formed with a highly doped p+ region on the substrate to provide substrate biasing. Although, not shown in the figure, the substrate contact is placed near the transistor.

The process parameters with their nominal values and range considered for this paper is given in Table I. We considered Copper (Cu) as the interconnect metal for MIV, Silicon (Si) the substrate material and Silicon dioxide (SiO₂) as the liner material. t_{miv} is the thickness of MIV, t_{ox} is the thickness of oxide liner to provide insulation from the substrate, H_{sub} is the height of the substrate layer through which the MIV passes through, n_{sub} is the substrate doping concentration, and n_{src} is the source and drain doping concentrations of the transistor. The nominal value of t_{miv} is assumed to be 50 nm as discussed in the previous works [22]. The nominal value of t_{ox} is assumed to be 1 nm considering the scaling between the TSV to MIV as discussed in [23], [24]. The length (l_{src}) and depth (not shown in figure) of the source/drain regions to implement the transistor is assumed to be 32 nm and 7 nm respectively. The width (w) of the transistor is assumed to be 32 nm. The length of the channel is assumed to be 14 nm, and the thickness of gate oxide is assumed to be 1 nm. The thickness and depth of guard ring are assumed to be 7 nm and 10 nm. The MIV pitch is assumed to be 100 nm [25].

We consider two performance metrics of the transistor to study the impact of MIV:

- 1) Maximum drain current $(I_{D,max})$, which is I_D at $V_{GS} = 1 V$ and $V_{DS} = 1 V$.
- 2) Maximum drain leak current $(I_{D,leak})$, which is I_D at $V_{GS} = 0 V$ and $V_{DS} = 1 V$.

We also assume that the voltage on the MIV ($V_{MIV} = 1$) since it inverts the region around MIV (to n-type) due to MIS structure.

In this section, we assume the nominal values for process parameters and the only variable considered is the placement of MIV with respect to transistor.

Parameter	Description	Value	Range
t _{miv} (nm)	MIV thickness	50	$20 \sim 100$
t _{ox} (nm)	Liner thickness	1	$0.25 \sim 2$
H _{sub} (nm)	Substrate height	100	$20 \sim 150$
$n_{sub} \ (cm^{-3})$	Substrate doping	10^{17}	$10^{15} \sim 5 \times 10^{17}$
$n_{src} \ (cm^{-3})$	Source / Drain doping	10^{19}	$10^{18} \sim 10^{21}$

TABLE I: Process parameters with their range

A. Scenario 1 – Vertical placement of MIV

In this scenario, MIV is placed in parallel to the transistor channel as shown in figure 3. In this subsection, we first focus on the effect of MIV on the transistor characteristics, when channel and MIV centers are aligned. Second, we study the impact of the offset distance from transistor channel to the center of MIV (d_{offset}) on the transistor performance. Finally, the transistor performance will be analyzed when the distance between the MIV and the transistor (d_{sep}) is varied.

1) MIV affect on transistor characteristics when channel center and MIV center are aligned: The impact of MIV on the transistor characteristics when $d_{sep} = 50 \ nm$ and $d_{offset} = 0$ is shown in Figure 4. The drain current I_D v.s. gate-source voltage V_{GS} plots for different drain-source voltage V_{DS} along with the ideal case where there is no MIV is shown in Figure 4(a). Similarly, I_D v.s. V_{DS} for different V_{GS} is shown in Figure 4(b). From the figure, we see that the $I_{D,max}$ increases by up to $1.58 \times$ and $I_{D,leak}$ increases by $70 \times$. The increase of $I_{D,leak}$ by $70 \times$ is a major concern since it will affect the power and thermal reliability of the IC.



Fig. 3: MIV placement to transistor channel in vertical placement scenario (model not to scale)



(b) I_D v.s. V_{DS}

Fig. 4: Nominal v.s. MIV effect on transistor characteristics

2) d_{offset} affect on transistor: The $I_{D,max}$ and $I_{D,leak}$ v.s. d_{offset} when $d_{sep} = 50 \ nm$ is shown in Figure 5, where the $I_{D,max}$ at $d_{offset} = 50 \ nm$ increased $1.34 \times$ compared with the $I_{D,max}$ of transistor without MIV. The $I_{D,max}$ is maximum at $d_{offset} = 0 \ nm$ and is increased by $1.58 \times$ compared with transistor without MIV. Similarly $I_{D,leak}$ is maximum when $|d_{offset}|$ is low and is about $70 \times$ compared with the transistor without MIV. This $I_{D,leak}$ is reduced to $6.6 \times$ when $|d_{offset}|$ is high. Therefore, placing MIV such that the transistor channel and MIV centers are not aligned is a good practice for leakage reduction.

3) d_{sep} affect on transistor: The $I_{D,max}$ and $I_{D,leak}$ v.s. d_{sep} at $d_{offset} = 0$ is shown in Figure 6, where the $I_{D,max}$ and $I_{D,leak}$ reduces significantly with increase in d_{sep} . At



Fig. 5: $I_{D,max}$ and $I_{D,leak}$ v.s. d_{offset} for $d_{sep} = 50 \ nm$

 $d_{sep} = 20 \ nm, I_{D,max}$ increased to 2.2× where as $I_{D,leak}$ increased to 225, 400× compared with the transistor characteristics without MIV. Also, please note the log axis for $I_{D,leak}$ in the Figure 6. At higher d_{sep} i.e., at 100 nm, the $I_{D,max}$ increases by $1.08\times$ and $I_{D,leak}$ increases by $1.41\times$ compared with the transistor characteristics without MIV. Therefore, d_{sep} has significant impact on the leakage of the transistor and should be considered as a design consideration for MIV placement to ensure proper M3D-IC realizations. Please note that, d_{sep} is the distance between MIV and the transistor and can be considered as the keep-out-zone for MIV.



Fig. 6: $I_{D,max}$ and $I_{D,leak}$ v.s. d_{sep} for $d_{offset} = 0 nm$

B. Scenario 2 – Horizontal placement of MIV

In this scenario, MIV is placed horizontally or in series with the transistor active region where the centers of transistor channel and MIV are aligned as shown in Figure 7. The transistor is separated from the MIV by d_{sep} distance where two cases are possible depending on the terminals T_1 and T_2 : 1) T_1 – source and T_2 – drain and, 2) T_1 – drain and T_2 – source.

The $I_{D,max}$ and $I_{D,leak}$ v.s. d_{sep} for the two cases i.e., case $1 - T_1$ as source and case $2 - T_1$ as drain is shown in Figure 8. The $I_{D,max}$ and $I_{D,leak}$ decreases with increase in d_{sep} . At $d_{sep} = 20 \ nm$, the $I_{D,max}$ increased by $1.8 \times$ and $1.3 \times$ compared with the transistor without MIV for case 1



Fig. 7: MIV placement to transistor channel in horizontal placement scenario (model not to scale)

and case 2 respectively. $I_{D,leak}$ increased by $6.5 \times$ and $11 \times$ compared with the transistor without MIV at $d_{sep} = 20 \ nm$ for case 1 and case 2 respectively. At higher d_{sep} i.e., at 100 nm, the $I_{D,max}$ increase only by $1.1 \times$ and $1 \times$ for case 1 and case 2 respectively compared with the transistor without MIV. Similarly, $I_{D,leak}$ increase only by $1.1 \times$ and $1.11 \times$ for case 1 and case 2 respectively compared with the transistor without MIV. Similarly, $I_{D,leak}$ increase only by $1.1 \times$ and $1.11 \times$ for case 1 and case 2 respectively compared with the transistor without MIV. Therefore, d_{sep} should be as higher as possible for scenario 2 to ensure $I_{D,leak}$ not to increase significantly. Although not discussed, the offset distance between MIV and transistor channel reduces both $I_{D,max}$ and $I_{D,leak}$ and should be as high as possible.

Observation 1: Vertical placement of MIV shown in Figure 3 has significant affect on transistor characteristics and require more keep-out distance compared with the horizontal placement of MIV shown in Figure 7.

However, eliminating the vertical placement scenario of MIV is not practically possible in order to obtain higher integration density. Therefore, in the rest of the paper, we consider only the vertical placement scenario of MIV and the same conclusions will also be valid for horizontal placement scenario.



Fig. 8: $I_{D,max}$ and $I_{D,leak}$ v.s. d_{sep}

IV. IMPACT OF PROCESS PARAMETERS ON TRANSISTOR CHARACTERISTICS

One important consideration for M3D-IC design is the process parameters since the sequential integration should be achieved at low temperatures specifically below 500°C [8], [9].

Therefore, the impact of MIV on the transistor characteristics by varying process is an essential study to make practical design considerations since there is no defined process for M3D IC technology. In addition, with the rising demand for heterogeneous integration and mixed-signal IC designs, we believe that it is essential to investigate process parameter affect on transistor characteristics in M3D-IC. For clarity purposes, we consider only Scenario 1 i.e., vertical placement of MIV for this study. First, we systematically study the impact of process parameters on the transistor characteristics in the presence of MIV at $d_{sep} = 50 \ nm$ in M3D-IC using control variable method to change one parameter at a time. The nominal values of these parameters are given Table I.

A. MIV thickness (t_{miv})

 $I_{D,max}$ and $I_{D,leak}$ v.s. t_{miv} is shown in Figure 9. The nominal $I_{D,max}$ and $I_{D,leak}$ obtained for the transistor without MIV is 2.79 μA and 3.78 fA respectively. Note that the transistor characteristics without MIV does not change with t_{miv} . From the figure, we can see that the $I_{D,max}$ increases almost linearly from $1.4\times$, when $t_{miv} = 20nm$ to $1.8\times$, when $t_{miv} = 100 \ nm$ compared with nominal $I_{D,max}$. Also, the $I_{D,leak}$ increases from $10\times$, when $t_{miv} = 20 \ nm$ to $805\times$, when $t_{miv} = 100 \ nm$ compared with the nominal $I_{D,leak}$. Therefore, the MIV affect is more prominent on the $I_{D,leak}$, and this effect should be considered while placing MIV near transistors. From previous observations, we know that $I_{D,leak}$ will reduce with d_{sep} , and hence the increase in t_{miv} require more d_{sep} (or KOZ) from the transistor to ensure lower $I_{D,leak}$.



Fig. 9: $I_{D,max}$ and $I_{D,leak}$ v.s. t_{miv}

B. MIV liner thickness (tox)

 $I_{D,max}$ and $I_{D,leak}$ v.s. t_{ox} is shown in Figure 10. The nominal $I_{D,max}$ and $I_{D,leak}$ obtained for the transistor without MIV is 2.79 μA and 3.78 fA respectively. Note that the transistor characteristics without MIV does not change with t_{ox} . From the figure, we can see that the $I_{D,max}$ almost remains constant at around $1.58 \times$ increase compared with nominal $I_{D,max}$. $I_{D,leak}$ decreases with increase in t_{ox} where it is $89 \times$, when $t_{ox} = 0.25$ nm to $58 \times$, when $t_{ox} = 2$ nm compared with the nominal $I_{D,leak}$. Therefore, higher t_{ox} is desired for reducing MIV impact on leakage current.



Fig. 10: $I_{D,max}$ and $I_{D,leak}$ v.s. t_{ox}

C. Height of Substrate (H_{sub})

 $I_{D,max}$ and $I_{D,leak}$ v.s. H_{sub} obtained for transistor with MIV and without MIV is shown in Figure 11. In this case, the transistor characteristics without MIV will also change with H_{sub} and therefore the $I_{D,max}$ and $I_{D,leak}$ of transistor without MIV is also included in Figure 11, where the plots labeled as $I_{D,max}$ and $I_{D,leak}$ correspond to the transistor without MIV case and the plots labeled as $I_{D,max}(MIV)$ and $I_{D,leak}(MIV)$ corresponds to the transistor with MIV case. From the figure, the presence of MIV near the transistor increases both $I_{D,max}$ and $I_{D,leak}$ compared with the transistor without MIV presence. From the figure, we see that $I_{D,max}$ increases by up to $1.7 \times$ in MIV presence at nominal separation compared with the case without MIV. Similarly, $I_{D,leak}$ increases by up to $353\times$. One important thing to consider is that the height of substrate also affects the minimum thickness of MIV due to the change in aspect ratio of MIV and hence we cannot increase the substrate height significantly.



Fig. 11: $I_{D,max}$ and $I_{D,leak}$ v.s. H_{sub}

D. Substrate Doping (n_{sub})

 $I_{D,max}$ and $I_{D,leak}$ v.s. n_{sub} characteristics for transistor with MIV and without MIV is shown in Figure 12. From

the figure, we see that as n_{sub} increases, the I_{leak} decreases for both transistor in presence of MIV and transistor without MIV cases. However, the presence of MIV increases both $I_{D,max}$ and $I_{D,leak}$ of the transistor compared with the transistor without MIV. We also found that $I_{D,max}$ and $I_{D,leak}$ increases by up to $2.25 \times$ and $403,100 \times$ respectively with MIV presence. Also, the nominal n_{src} is 10^{19} cm^{-3} and therefore if the n_{src}/n_{sub} ratio is higher, the leakage will be very high because of higher reverse saturation current at drain and substrate boundary. In addition, we know that the depletion region between the drain and substrate will increase with the decrease of substrate doping n_{sub} [26] and therefore the impact of MIV on $I_{D,leak}$ is higher at the lower n_{sub} .



Fig. 12: $I_{D,max}$ and $I_{D,leak}$ v.s. n_{sub}

E. Active Doping (n_{src})

 $I_{D,max}$ and $I_{D,leak}$ v.s. n_{src} is shown in Figure 13. From the figure, we see that the $I_{D,max}$ increases in the linear scale where as the $I_{D,leak}$ increases exponentially for both transistor with MIV and without MIV cases. As n_{src} increases up to $10^{19} \ cm^{-3}$, presence of MIV resulted in increased leakages ranging from $48 \times$ to $70 \times$. We also observed that the $I_{D,max}$ increases by up to $4.23 \times$ and $I_{D,leak}$ increases by up to $70 \times$ for transistor with MIV presence compared with the transistor without MIV. We also observed that $I_{D,leak}$ increases significantly with the increase of n_{src} and, therefore the n_{src}/n_{sub} ratio should not be very high.

Observation 2: n_{sub} has significant impact on the leakage current of the transistor, when the other process parameters are assumed to be nominal values shown in Table I and MIV is placed at $d_{sep} = 50 \ nm$.

V. KEEP-OUT-ZONE FOR MIV IN M3D-IC PROCESS

In this section, we consider three process parameters, specifically substrate height H_{sub} , substrate doping n_{sub} and source/drain doping n_{src} to study the impact of MIV at the assumed process for realizing the transistor at M3D-IC technology. We assume that n_{src}/n_{sub} to be 100 and 1000 and varied the n_{src} from 10^{18} cm⁻³ to 10^{21} cm⁻³. The substrate height H_{sub} is also varied from 25 nm to 100 nm. For these cases, we assume the thickness of MIV to be 50 nm and the liner thickness to be 1 nm. The impact of MIV placed



Fig. 13: $I_{D,max}$ and $I_{D,leak}$ v.s. n_{src}

at 50 nm away from the transistor of 32 nm width on the transistor characteristics is shown in Table II. From the table, we can see that at higher n_{src} (i.e., last three rows colored in blue), the leakage is not significantly increased with MIV presence compared with the transistor leakage without MIV. At lower n_{sub} , the MIV presence has significant impact on the leakage where the I_{leak} increased more than $100 \times$ compared with the transistor leakage without MIV (i.e., top rows colored in red) and is increased by up to $68, 668 \times$. Therefore, the M1 metal pitch of 100 nm ($d_{sep} = 50$ nm) is not sufficient to ensure the reliability of M3D-IC design. From Table III, we can say that keep-out-zone (KOZ or minimum d_{sep}) between MIV and the transistor is needed to ensure reliability of the M3D-IC realization, and is highly dependent on the n_{sub}, n_{src} and H_{sub} of the transistor.

Note: KOZ is defined as the minimum spacing around MIV where no other active devices should be formed. d_{sep} is the distance between MIV and the transistor placed near by. Therefore, the minimum d_{sep} required and KOZ are same.

Table III shows the KOZ in nm for the different process parameters of the transistors where we assumed that the KOZ increases in steps of 50 nm. The KOZ value is obtained when the I_{leak} of the transistor placed near MIV is less than $10 \times$ compared to the transistor without MIV. From the table, we can see that transistor process-aware KOZ for MIV is essential for proper operation of the M3D-IC design where the KOZ value can range between 50 nm to 500 nm for the assumed variations in the process parameters specifically n_{src} , n_{sub} and H_{sub} . Therefore, at floorplanning and placement stage of M3D-IC designs, we need to consider these KOZ considerations, and is dependent on the nearby transistor specifications. For example, assume a transistor near MIV has the process parameters as $H_{sub} = 100 \ nm, n_{sub} = 10^{17} \ cm^{-3}$ and $n_{src}=10^{19}\ cm^{-3}$ then the KOZ for MIV should be at least 100 nm.

VI. FUTURE DIRECTIONS

In this work, we focused on the thin silicon substrate of 25nm – 100 nm thickness for top-layer in M3D-IC technology. Our future work will also focus on the effect of MIV when multiple transistors are placed around it and the process-aware

	n_{src}	n_{sub}	H_s	ub = 25nm	m $H_{sub} = 50nm$		$H_{sub} = 75nm$		$H_{sub} = 100 nm$	
	(cm^{-3})	(cm^{-3})	I_{max} (μA)	I_{leak} (A)	I_{max} (μA)	I_{leak} (A)	I_{max} (μA)	I_{leak} (A)	I_{max} (μA)	$I_{leak}(A)$
$d_{sep} = 50 nm$	10 ¹⁸	10^{15}	4.60 (×1.30)	$1.65 \times 10^{-07} \ (\times 171)$	4.48 (×1.64)	$2.63 \times 10^{-07} (\times 882)$	4.66 (×2.01)	$3.04 \times 10^{-07} (\times 8090)$	4.55 (×2.53)	$3.50 \times 10^{-07} \ (\times 68668)$
		10^{16}	2.89 (×2.00)	$5.34 \times 10^{-09} \ (\times 1865)$	$1.71 (\times 3.30)$	$1.01\times 10^{-09}~(\times 13906)$	$1.45 (\times 5.90)$	$4.56\times 10^{-10}~(\times 31241)$	1.30 (×6.53)	$3.10 \times 10^{-10} \ (\times 44983)$
	10 ¹⁹	10^{16}	11.89 (×1.29)	$8.93 \times 10^{-08} \ (\times 442)$	9.34 (×1.56)	$1.25 \times 10^{-08} \ (\times 6988)$	8.23 (×1.84)	$5.00 \times 10^{-09} \ (\times 18709)$	7.92 (×1.90)	$2.83 \times 10^{-09} \ (\times 31175)$
		10^{17}	8.57 (×1.33)	$1.78 \times 10^{-10} (\times 244)$	5.37 (×1.56)	$1.33 \times 10^{-12} \ (\times 201)$	4.51 (×1.59)	$4.61\times 10^{-13}~(\times 99)$	4.35 (×1.56)	$2.64 \times 10^{-13} \ (\times 70)$
	10 ²⁰	10^{17}	30.60 (×1.12)	$8.23 \times 10^{-07} (\times 7)$	24.92 (×1.15)	$2.15 \times 10^{-08} \ (\times 26)$	23.51 (×1.16)	$8.51 \times 10^{-09} \ (\times 26)$	23.24 (×1.15)	$3.74 \times 10^{-09} \ (\times 17)$
		10^{18}	17.89 (×1.01)	3.36×10^{-11} (×1.13)	14.92 (×1.00)	$2.63\times 10^{-12}~(\times 1.09)$	14.81 (×1.01)	$2.35\times 10^{-12}~(\times 1.21)$	15.09 (×1.01)	$2.41 \times 10^{-12} (\times 1.07)$
	10^{21}	10^{18}	29.21 (×1.02)	$3.60 \times 10^{-08} \ (\times 1.16)$	24.61 (×1.02)	$2.37 \times 10^{-09}~(\times 1.20)$	24.36 (×1.01)	$2.25 \times 10^{-09} \ (\times 1.10)$	24.93 (×1.01)	$3.60 \times 10^{-09} \ (\times 1.09)$
		10^{19}	4.01 (×1.03)	$3.79 \times 10^{-15} \ (\times 1.16)$	4.01 (×1.02)	$4.45 \times 10^{-15} (\times 1.13)$	3.47 (×1.00)	$3.01 \times 10^{-15} \ (\times 1.03)$	4.32 (×1.00)	$6.39 \times 10^{-15} \ (\times 1.00)$

TABLE II: Maximum drain current $I_{D,max}$ and Leakage current $I_{D,leak}$ for different process parameters of M3D-IC

TABLE III: KOZ or minimum d_{sep} (in nm) for different
process parameters of M3D-IC

n_{src}	n_{sub}	$H_{sub}(nm)$			
(cm^{-3})	(cm^{-3})	25	50	75	100
10 ¹⁸	10^{15}	400	450	500	500
10	10^{16}	200	200	200	200
1019	10^{16}	200	250	200	200
10	10^{17}	100	100	100	100
1020	10^{17}	50	100	100	100
10	10^{18}	50	50	50	50
1021	10 ¹⁸	50	50	50	50
10	10^{19}	50	50	50	50

KOZ of MIV-based design optimization for M3D-IC circuits. However, there are also demonstrations on the FDSOI device with ultra-thin channel in the range of 6nm - 10nm [6], [8], [14], [15], [27], [28]. For this top-layer realization, the backgate bias for top-layer FDSOI devices should be investigated for coupling reduction from the bottom-layer devices and interconnects. Although the MIV does not pass through the substrate for top-layer FDSOI devices, the device will be adjacent to the MIV depending on the MIV minimum distance. The channel with the MIV will also form the MIS structure but with thick oxide defined by the separation between MIV and adjacent device. Therefore, the MIV impact on the device characteristics should also be considered for reliable toplayer devices since MIV can potentially turn on the channel and increase leakage due to the capacitive coupling. Also, FinFET based top-layer devices are also realized in M3D-IC technology [18]. Similar study for the effect of FinFET device characteristics with MIV adjacent to it should also be considered for the reliable M3D-IC implementations.

Capacitive coupling between MIV and the substrate is considered to realize MIV-devices thus reducing the MIV area overhead in [10], [11]. Similar study considering this MIS structure for ultra-thin FDSOI devices can be considered. In addition, the placement and routing considerations of power delivery networks (PDN) and clock distribution networks (CDN) considering MIVs to route between layers should be studied.

VII. CONCLUSIONS

In this work, we have discussed the impact of MIV on the surrounding substrate region and on the transistor placed near MIV. We have performed a systematic study on the effect of MIV on the characteristics of the transistor when an MIV is placed near the transistor at different orientations. We then demonstrated that the process parameters specifically substrate doping and source/drain doping of the transistor have a significant effect on the leakage current of the transistor. Finally, we studied the minimum KOZ requirement for the M3D-IC process where we assumed that the substrate doping, source doping and substrate height as parameters and obtained KOZ for each possible process parameter with the assumed M3D-IC process.

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