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# An Inductively Powered Scalable 32-Channel Wireless Neural Recording System-on-a-Chip for Neuroscience Applications

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There has been considerable effort devoted to developing technology for interfacing with the central nervous system in laboratory animals and humans [1-2]. Even though these efforts have led to marvelous technological advancements in circuits and systems, some of the resulting devices may find little use in their application domain, because the specifics of the targeted applications or the realistic needs of the end users may not be taken into account.

Neural interfacing technology can be applied to two major areas: neurological diseases (clinical) and neurosciences (research). Devices that target the former, i.e. neuroprostheses, need to be chronically implantable, extremely safe, and highly reliable to be used in humans as part of a therapeutic procedure. Size, power consumption, and carrier frequency are highly constrained due to implantation requirements. Cochlear implants and deep-brain stimulators (DBS) are examples of neuroprostheses with undeniable positive outcomes [3]. On the other hand, devices that target neuroscience research do not necessarily need to be implantable. However, they have to compete with sophisticated instruments that are currently in use by the neuroscience community [4]. These devices should at least provide the same quality and quantity of information as their older counterparts, while resolving some of their limitations, such as eliminating hardwires. For instance, a device that utilizes the UWB band (3.1-to-10.6GHz) for wireless communication is not suited for implantation and clinical applications, while data reduction and classification by simple on-chip DSP is not sufficient for most research purposes [5].

We introduced a Wireless Integrated Neural Recording system (WINeR-5) in [6] as a substitute for hardwires in recording setups from freely moving animals in behavioral neuroscience research applications. This removes a source of motion artifacts and bias in the experimental results due to psychological effects of tethering. However, a key limitation of WINeR-5 and many similar wireless systems is the need for the animal subject to carry a payload of batteries. This may not matter when recording from costly primates [7]. However, most labs use small animals such as rats and mice, for which there will be a compromise between the size/weight of the headstage and the uninterrupted duration of experiments. Here we report the first closed-loop inductively powered wireless integrated neural recording system-on-a-chip (WINeR-6) for research applications, which can simultaneously record from 32-channels for an unlimited period of time without losing any piece of information.

Figure 6.4.1 shows the WINeR-6 block diagram and its test setup. Neural signals are amplified and filtered by an array of capacitively coupled fully differential LNAs with adjustable gain (67.8/78dB) and bandwidth (HPF: 0.1Hz-1kHz/LPF: 8kHz) [6]. Our prior

experience with WINeR-5 showed that although each LNA consumes a small current (~25µA), since there are 32 of them, the LNA block quickly becomes the dominant power consumer (42%). This condition is exacerbated with an increased number of channels. To address this issue, we employ a power-scheduling mechanism, depicted in Fig. 6.4.2, that puts most of the LNAs that are not being sampled in sleep mode with a fraction of their active current consumption (0.5µA). We do not completely turn the LNAs off to reduce the transient time,  $t_T$ , for a dormant LNA to reach its active state ahead of each sampling. The number of LNAs that should be activated ahead of sampling, *N*, depends on the overall sampling rate,  $f_S$ , which in turn depends on the desired neural signal bandwidth ( $N > f_S t_T$ ). In WINeR-6, *N* is programmable by bits SR0:2, which change the number of consecutive '1's in a circular shift register (CSR) that activates the LNAs. The last circulating '1' indicates the channel that is ready to be sampled. A key advantage of this mechanism over [5], in which the 1<sup>st</sup> stage is always on, is its robustness against stimulus artifacts. Artifact rejection will be necessary in future revisions of the WINeR system, which will have stimulation capability.

Amplitude-to-time conversion (ATC) is done by comparing the last active LNA output with a precision triangular waveform, whose frequency and  $V_{P-P}$  ( $V_{Low}-V_{High}$ ) can be adjusted by the user to indicate  $f_S$  and input dynamic range, respectively. Four monitoring signals ( $V_{REC}/2$ ,  $V_{SS}$ ,  $V_{BG}$ ,  $V_T$ ) are also sampled along with 32 LNA outputs in each 36-pulse TDM-PWM packet to close the inductive power control loop and monitor the ASIC functionality and temperature. These signals also provide a unique pattern that indicates the beginning of each TDM-PWM packet on the Rx.

The TDM-PWM signal drives the Tx block, which includes a VCO with an off-chip inductor followed by a PA (Fig. 6.4.3). Changes in the loading and reflected RF signal result in undesired VCO frequency shifts in WINeR-5 when the animal is moving in the cage. We resolve this problem by adding the nonlinear class-AB PA, which also helps with implementing wideband OOK (through M6) and Tx output matching with miniature  $50\Omega$  antennas, extending the range. Coarse and fine VCO tunings are done with the choice of off-chip inductor and a 4b on-chip varactor bank (VC0:3), respectively. WINeR-6 is also equipped with an LED driver, which can support an optical or hardwired data link. The wideband custom Rx, shown on the lower right side of Fig. 6.4.1, has been described in [6].

Figure 6.4.4 shows the power-transmission circuit. The primary coil (L1), whose geometry has been optimized for  $f_P$  =13.56MHz [8], is driven by a 1W class-C PA, which is driven by a commercial RFID reader (MLX90121). On the receiver side, we have an off-chip L<sub>2</sub>C<sub>2</sub> tank circuit tuned at  $f_P$ , followed by a full-wave active rectifier and 3V LDO, both of which are integrated on WINeR-6. This rectifier provides a measured power conversion efficiency (PCE) of 80.2% at 13.56MHz utilizing a pair of offset-controlled high-speed comparators that compare  $V_{INI,2}$  and  $V_{REC}$  across P1 and P2 (W/L=2100/0.6), and drive their large gates. Four offset-control bits in each comparator (CTL0:3) adjust the rising and falling times such that the comparator delay is reduced to 0.75ns, and back currents are minimized. Changes in the coil coupling coefficient (k), resulting from animal movements, affect the rectifier output voltage ( $V_{REC}$ ), which is fed back to the Rx as one of the monitoring signals. This

information is then used to control the PA supply voltage through an MSP430, a DAC, and a Darlington pair (Fig. 6.4.4) [9].

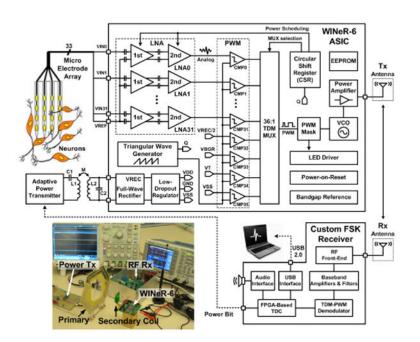
WINeR-6 is fabricated in a 0.5µm 3M2P standard CMOS process and measures  $4.9 \times 3.3$  mm<sup>2</sup> (Fig. 6.4.7). When all channels are active, it consumes 7mW from ±1.5V supplies in the FSK mode. With power scheduling (*N*=12) the power consumption drops to 5.8mW. With Tx and Rx antennas 0.5m apart, and L<sub>1</sub> and L<sub>2</sub> separated by 8cm, the system was bench-top tested using two function generators, whose outputs were divided to generate voltages below 1mV (Fig. 6.4.3 inset). Figure 6.4.5 shows the effect of power scheduling on the recorded waveforms at the LNA and PWM outputs, as well as power distribution among blocks. Figure 6.4.6 summarizes the specifications of the WINeR-6 ASIC and the experimental setup (Fig. 6.4.1 inset).

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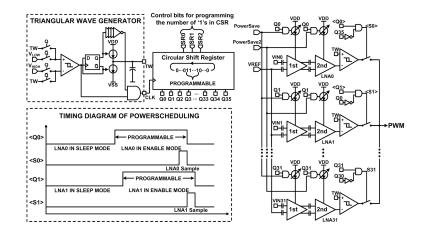
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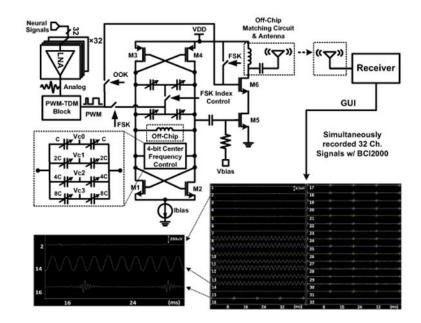


**Figure 6.4.1.** WINeR-6 overall system block diagram. Inset: Measurement setup.



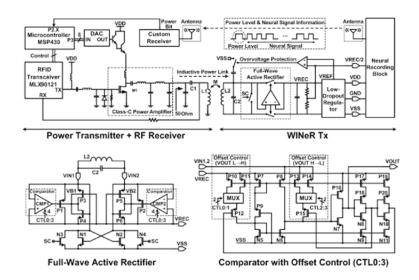
#### Figure 6.4.2.

Power scheduling keeps the majority of LNAs in the sleep mode using a circular shift register. A programmable number of the LNAs, which need to be turned on ahead of sampling, are moved to the active mode at any time.



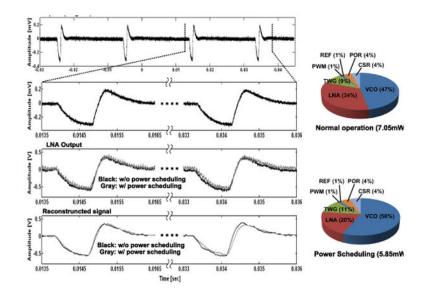
## Figure 6.4.3.

Neural signal-flow diagram, emphasizing the VCO architecture and on-chip class-AB PA, which reduces the effects of loading on the VCO. Inset: Wirelessly recorded 32ch waveforms when the WINeR-6 ASIC is inductively powered.



# Figure 6.4.4.

Inductive power flow diagram, showing the closed-loop power-control mechanism and highefficiency full-wave active rectifier schematic [8].



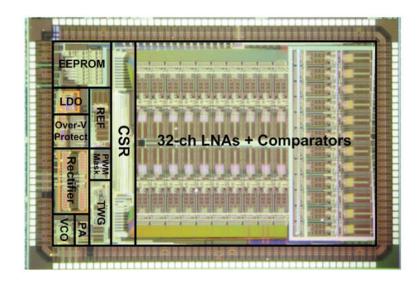
# Figure 6.4.5.

Measured waveforms from top: Original artificial spike waveform, recorded waveforms at the LNA output, sampled and pulse width demodulated waveforms. Power distribution chart among different blocks with and without power scheduling (N = 12).

| Wireless Integrated Neural Recordin                 | g System (WINeR-                 | 6)                   |  |
|---|----------------------------------|----------------------|--|
| Fabrication technology                              | ON Semi 0.5µm 3M2P Std. CMOS     |                      |  |
| Die size (mm <sup>2</sup> )                         | 4.93 × 3.33                      |                      |  |
| Total power consumption (mW)                        | 7.05 (N=32) / 5.85 (N=12)        |                      |  |
| Sampling rate (kSps)                                | 58 ~ 709                         |                      |  |
| Neural Recording                                    | 7                                |                      |  |
| Power source  | Battery                          | Inductive            |  |
| Number of channels                                  | 32 recording + 4 monitoring      |                      |  |
| LNA gain (dB)                                       | 67.8 / 78                        |                      |  |
| LNA CMRR / PSRR (dB)                                | 134 / 62.7                       |                      |  |
| LNA input referred noise (µVms) (0.1Hz ~ 10kHz)     | 4.39                             | 4.97                 |  |
| System input referred noise (µVrms) (0.1Hz ~ 10kHz) | 6.9                              | 9.37                 |  |
| LNA current consumption (µA)                        | 25 (Simulation)                  |                      |  |
| LNA bandwidth                                       | HPF: 0.1-1kHz / LPF: 8kHz        |                      |  |
| RF Telemetry Lin                                    | k                                |                      |  |
| FSK carrier frequency (MHz)                         | 915/845.5 or 915/877             |                      |  |
| VCO center frequency adjustment (MHz)               | 0 ~ 50 (16 steps)                |                      |  |
| VCO and PA current consumption (mA)                 | 1.1                              |                      |  |
| Tx RF output power (dBm)                            | -22                              |                      |  |
| Max. Tx-Rx antenna distance (m)                     | 1.5                              | 0.8                  |  |
| Inductive Powerin                                   | 18                               |                      |  |
| Operating frequency (MHz)                           | 13.56 (ISM band)                 |                      |  |
| Rectifier Vout / Vin(Peak) / Vin(RMS) (V)           | 3.12 / 3.55 / 2.41               |                      |  |
| Rectifier power conversion efficiency (PCE)         | 80.2%                            |                      |  |
| Distance between coils (cm)                         | 12 (Max.) / 8 (Nominal)          |                      |  |
| LDO dropout voltage (mV)                            | 150                              |                      |  |
| LDO current consumption (µA)                        | 24 (Simulation)                  |                      |  |
| Peak to peak ripple on VDD / VSS (mV)               | 80                               |                      |  |
| Tx coil diameter (cm) / Turns / inductance (µH)     | 16.8/2                           | 16.8 / 2 / 0.88 (L1) |  |
| Rx coil diameter (cm) / Turns / inductance (µH)     | 3.0 / 2 / 0.41 (L <sub>2</sub> ) |                      |  |

#### Figure 6.4.6.

Summary of WINeR-6 system and test setup specifications.



**Figure 6.4.7.** WINeR-6 4.9×3.3 mm<sup>2</sup> die micrograph and floor plan.