4.3 A Wideband IM3 Cancellation Technique for CMOS Attenuators

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In the receiver path and in spectrum analyzers, typically gain control blocks are used to limit the incident power to the level that the receiver circuitry can handle without degrading the linearity; in the transmitter path stringent power control is also desirable. Although variable-gain amplifiers (VGAs) traditionally implement the gain-control block, attenuators based on FET transistors show superior performances on linearity, power handling capability and power consumption.

Much effort [1-3] has been devoted to improving the linearity and power-handling capability of attenuators. Adaptive bootstrapped body biasing [1] is used in a cascaded-Π attenuator to suppress the body-related parasitic effects and improve P_{1dB}. A Π attenuator with parallel branches designed for discrete attenuation steps achieving +23dBm IIP3 is shown in [2]. The stacked-FET technique used in [3,4] distributes the signal swing among many FETs in series to reduce the drain-source voltage swing for each FET and hence reduce the IM3 distortion. However, the large transistors required by this technique bring in large parasitic capacitances, which lower the bandwidth and increase the minimum insertion loss at high frequency. Moreover, the capacitive nonlinearities introduced by large parasitic capacitances will limit the highest achievable IIP3. Therefore, this technique is mainly effective in SOI CMOS [3].

This paper proposes a wideband IM3 cancellation technique for bulk CMOS Π attenuators where the IM3 distortion currents of transistors within the attenuator cancel each other. In the Π attenuator in Fig. 4.3.1(upper), the voltage swings across the nonlinear output conductances of transistors M_1, M_2 and M_3 generate IM3 distortion currents $i_D^{M_1}$, $i_D^{M_2}$ and $i_D^{M_3}$ defined from drain to source.

The distortion current of M_1 ($i_D^{M_1}$) is directed towards R_{load}, while the distortion currents of M_2 and M_3 ($i_D^{M_2}$ and $i_D^{M_3}$) are directed out of R_{load}. This suggests that the distortion due to M_1 can cancel the distortion generated by M_2 and M_3. Using the weakly nonlinear distortion analysis approach in [5], for a certain attenuation value $0 \le A \le 1$, the IM3 output voltage is given by

$$v_{out}^{\omega_{IM3}} \propto \frac{3\times {V_{in}}^3}{(1+A)^4 \cdot 16 {R_s}^3} \times \left[\frac{16A^4}{{W_{M_1}}^3} - \frac{(1-A)^4 A^3}{{W_{M_2}}^3} - \frac{(1-A)^4 A}{{W_{M_3}}^3}\right] \quad (1)$$

where W is the transistor width. In deriving (1) the transistor's 3rd-order output conductance nonlinearity is assumed to dominantly contribute to IM3. Eq. (1) suggests that in the Π attenuator, the IM3 current of M_1 at least partially cancels the IM3 current of M_2 and M_3 at the output. When $\frac{16A^3}{{W_{M_1}}^3} = \frac{(1-A)^4 A^2}{{W_{M_2}}^3} + \frac{(1-A)^4}{{W_{M_3}}^3}$ there is full IM3 cancellation within the Π attenuator, which is robust since it only relies on the ratio of transistor widths; then IIP3 is limited by mechanisms such as capacitive nonlinearity.

To verify the concept of (1) we implemented the Π attenuator shown in Fig. 4.3.1(lower) with four parallel branches in a standard 0.16um CMOS process. For this attenuator, each parallel branch is designed for -12dB attenuation (A=0.25) and has different width for M_1 that yields either full or partial IM3 cancellation. For the measurements, we enable M_2 and M_3 while selectively enabling one parallel branch at a time. This mimics a Π attenuator with a selectable W_{M1} for fixed W_{M2} (23um) and W_{M3} (20um). For a two-tone input signal centered at 1GHz with 3.2MHz spacing, the IIP3 is extrapolated from -15dBm to -10dBm.

The measured and simulated IIP3 (using PSP model) as a function of W_{M1} are shown in Fig. 4.3.2, which verifies this IM3 cancellation theory. Note that the calculated optimal W_{M1} is 18um while it is 20um from simulations. For small W_{M1}, M_1 is dominant for the IM3. As W_{M1} increases its distortion decreases and hence IIP3 increases until its maximum at full IM3 cancellation. For even larger W_{M1} the IIP3 is dominated by M_2 and M_3 yielding a saturated sub-optimum value because W_{M2} and W_{M3} are fixed. Figure 4.3.2 also shows the measured IIP3 for four different W_{M1} by sweeping the center frequency from 0.1GHz to 3GHz. The differences between measured and simulated IIP3 are due to limited accuracy of transistor modeling. For the Π attenuator with full IM3 cancellation (W_{M1}=20um), the IIP3 decreases as the f_{rf} increases because the phase difference between the distortion current of M_1 and that of M_2 and M_3 increasingly deviates from 180° due to parasitic capacitances. As a result, the IM3 cancellation degrades as the frequency increases. Since this IM3 cancellation technique involves no extra devices but only properly dimensioning the transistors' W, there is no need to trade large transistors for high linearity as in [3].

A four-branch attenuator system with selectable attenuation (see Fig. 4.3.3) using this IM3 cancellation technique was fabricated in a standard 0.16um CMOS process. Each branch contains one Π attenuator that uses the topology shown in Fig. 4.3.1 (upper) and is designed for one specific attenuation setting (-6dB, -12dB, -18dB and -24dB) and optimized for full IM3 cancellation (transistor W fixed by (1)). A 3-to-8 digital decoder provides the controlling voltage (1.8V for enabling and 0V for disabling). The active area of the attenuator and the decoder is 50x30um^2 and 60x65um^2 respectively. For each of the forenamed attenuation settings, only one branch is enabled. For minimum signal attenuation, the series transistors in all four branches are enabled, and the shunt transistors in all four branches are disabled, yielding an additional -1.8dB attenuation. For isolation and ac-bootstrapping purposes, the gate of transistor M_1 in the Π attenuators is connected to the controlling voltage via a 20kΩ resistor; while the bulk is connected to GND via a 20kΩ resistor. The attenuator (see Fig. 4.3.7) was measured by on-wafer probing. The two-tone spacing is 3.2MHz for all measurements.

Figure 4.3.3 shows the measured and simulated S_{11}/S_{21} (50Ω reference) for all attenuation settings. Due to a mistake in the decoder design, the minimum attenuation setting (-1.8dB) cannot be enabled. For this setting we only show the simulated S_{11}/S_{21}. Due to unaccounted parasitics, the measured S_{21} for f_{rf}>5GHz deviates >1.6dB from simulation. Since the proposed IM3 cancellation does not require large transistors, 5GHz bandwidth is achieved with S_{11}<-14dB and with S_{21} variation <1.6dB. The difference between the measured NF and measured insertion loss ($|S_{21}|$) is within 0.1dB up to 10GHz, which shows that little noise is introduced by the attenuator. Figure 4.3.4 shows the measured HD1 and IM3 output at 1GHz. The compression/expansion P_{1dB} is >10dBm for all attenuation settings. The IIP3 are respectively 31dBm, 33dBm, 38dBm and 36dBm for attenuation settings -6dB, -12dB, -18dB and -24dB. Due to higher-order nonlinearities, the IM3 curves start to show 5th-order behavior for input power levels higher than -8dBm.

Figure 4.3.5 shows the measured IIP3 by sweeping the input frequency f_{rf}, from 0.1GHz to 10GHz. We achieve +30dBm IIP3 for the TV band (DC to 1.2GHz) and +26dBm for DC to 5GHz. At higher f_{rf}, extra phase shifts caused by the parasitic capacitances degrade the IM3 cancellation. The measured IIP3 of ten dies for f_{rf}=1GHz is also shown in Fig. 4.3.5. The IIP3 variation is within 1dB, which shows good robustness of this IM3 cancellation technique.

The benchmarking results in Fig. 4.3.6 shows that the presented attenuator achieves very high linearity for a very low active area in standard bulk CMOS. In conclusion this IM3 cancellation provides a robust IIP3 improvement with minimum active area consumption.

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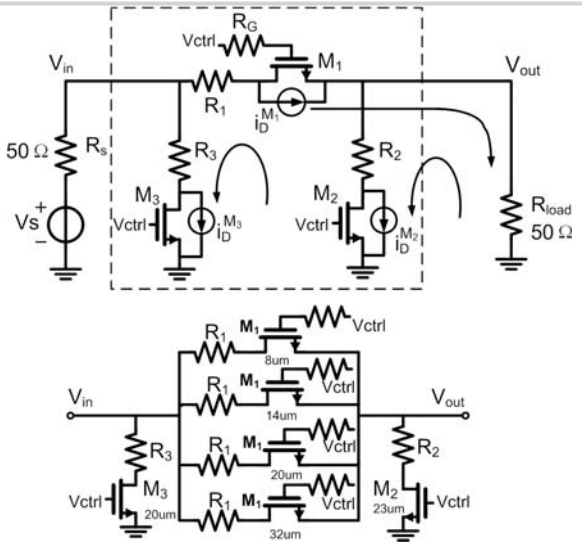

Figure 4.3.1: Concept of the wideband IM3 cancellation for Π attenuator and demonstration circuit for this concept.

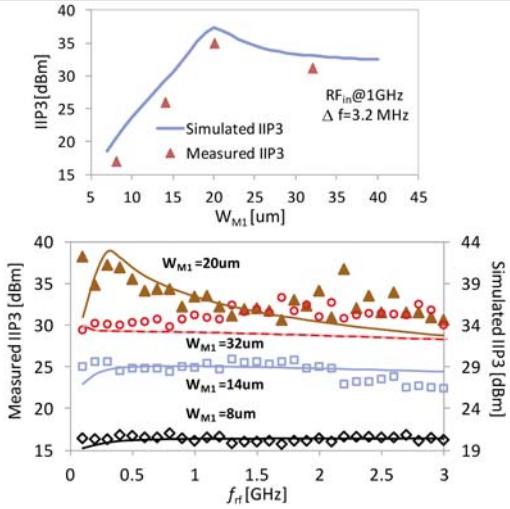

Figure 4.3.2: Measured and simulated IIP3 illustrating the IM3 cancellation technique for the Π attenuator. Symbol for measurement results, line for simulation results.

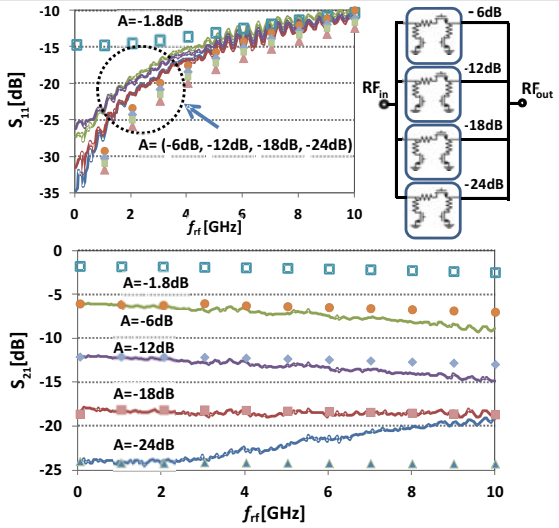

Figure 4.3.3: S_{11}/S_{21} for the four-step attenuator. Line for measurement results, symbol for simulation results.

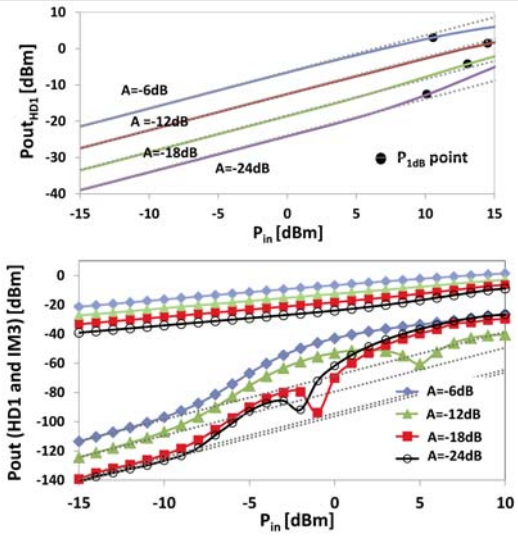

Figure 4.3.4: Measured output HD1 and IM3 vs input power for two-tone input signals centered at 1GHz with 3.2MHz spacing.

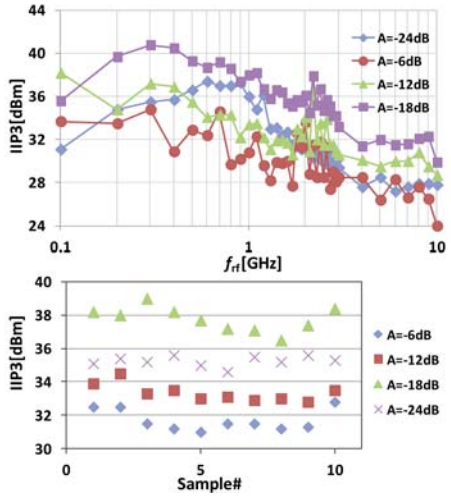

Figure 4.3.5: Measured IIP3 as a function of the two-tone center frequency f_{rf}, with 3.2MHz frequency spacing and measured IIP3 of ten samples for f_{rf}=1GHz.

	Huang [1]	Youssef [2]	Dogan [6]	Granger-Jones[3]	Ku[7]	This work
Technology	0.18um CMOS	65nm CMOS	0.13um CMOS	CMOS SOI	0.18um CMOS	0.16um CMOS
VDD [V]	1.8	1.2	1.2	5	N/A	1.8
Chip area[mm^2]	0.28	0.05	0.7	N/A	0.5	0.0054
Bandwidth[GHz]	0.4-3.7	0.4-0.8	DC-2.5	0.05-4	DC-14	DC-5
IIP3[dBm]	+15	+23	+10	+47	29@10GHz	+30(0.1-1.2GHz) +26(0.1-5GHz)
P1dB[dBm]	+6	N/A	+2.5	30	15@10GHz	+10
Attenuation flatness[dB]	2.6	N/A	2.6	3	0.5	1.6
Max. attenuation[dB]	33	48	42	40	31.5	24
Minium attenuation[dB]	0.96-2.9	N/A	0.9-3.5	2.4-4	3.7-10	1.8-2.4 (sim)
Return loss[dB]	>9	>12	>8.2	>14	>9	>14
Control mode	Linear-in-dB	Discrete step	Linear-in-dB	Linear-in-dB	Discrete step	Discrete step

Figure 4.3.6: Comparison of state-of-the-art attenuators.

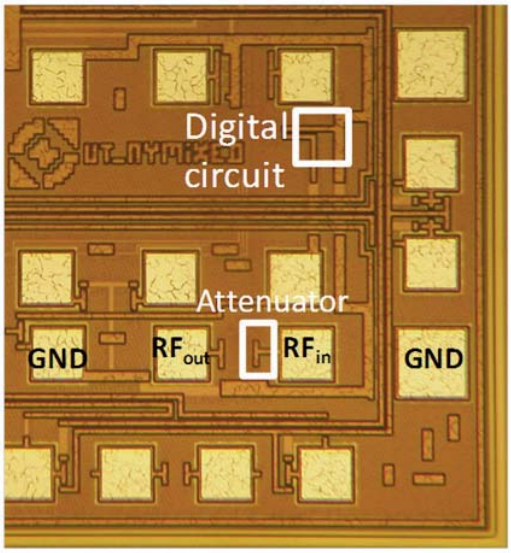

Figure 4.3.7: Micrograph of the chip fabricated in a standard 0.16um bulk CMOS.

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