21.1 A 0.3-to-1.2GHz Tunable 4th-Order Switched g_m-C Bandpass Filter with >55dB Ultimate Rejection and Out-of-Band IIP3 of +29dBm

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The trend towards reconfigurable receivers requires on-chip flexible filters that can replace dedicated, bulky and non-tunable filters (e.g., SAW and BAW [1]). Although BAW filters are compatible with silicon processes, their center frequency is sensitive to thickness variation of the piezoelectric material and the achievable tuneability is limited [1]. Other techniques to make RF on-chip band-pass filters (BPFs) include Q-enhancement, g_m-C and N-path. Q-enhancement approach has several disadvantages such as large area due to inductors which do not obey process scaling, limited tuneability and poor dynamic range [2]. Main drawbacks of g_m-C filters are the tradeoff between power consumption, quality factor, center frequency and dynamic range and the need for tuning circuitry [3]. Recently there has been renewed interest in the translational impedance conversion of N-path filters [4-6]. Due to the "transparency" of the passive mixer, baseband impedance is translated to frequencies around the clock frequency f_{lo} [7]. The interesting features of these filters are their direct tuneability with f_{lo}, higher quality factor compared to on-chip CMOS LC filters [2], high linearity and graceful scaling with process.

However, N-path filters [6] have two main limitations: 1) The switch resistance R_{sw} limits the ultimate rejection to $R_{sw}/(R_{sw}+R_s)$ (typically around 16dB [4]) where R_s is the source impedance; 2) Recent published N-path filters have only 2nd-order filtering, and higher orders have only been achieved by cascading [4], still rendering a "round" band-pass filter shape. This paper proposes a new method to increase the order of the BPF while having a better pass-band shape as compared to [4,6]. It also weakens the effect of the switch resistance on the ultimate rejection to obtain >55dB ultimate rejection in a 65nm CMOS chip.

To achieve a higher-order filter, we propose the use of subtraction. Suppose we have two 2nd-order BPFs with equal bandwidth ($\omega_{0,1}/Q_1 = \omega_{0,2}/Q_2$), but slightly different center frequencies ($\omega_{0,1}$ and $\omega_{0,2}$). If we subtract the output of these two filters, 4th-order filters with good pass-band shape results (see Fig. 21.1.1).

The 4-path implementation of the proposed filter is shown in Fig. 21.1.2. The switches in each path are driven by a non-overlapping 25% duty-cycle LO. The combination of baseband capacitors C_{BB} and switches in each path emulate the RLC tanks of Fig. 21.1.1 with center frequency of f_{lo} [6]. To shift the center frequency of the two filter sections apart, the use of multiple clocks would give a lot of overhead, so we looked for another way to obtain frequency shifting. In [4], the filter center frequency is shifted by means of a 16-phase switched capacitor technique. One drawback of this technique is that it folds blockers located at $f_{lo}+17\times f_{IF}$ or $f_{lo}-15\times f_{IF}$. Instead, here we use poly-phase g_m cells in baseband to shift the baseband admittance from $C_{BB}j\omega$ to $C_{BB}j(\omega \pm \omega_b)$ with $\omega_b=2g_m/C_{BB}$. N-path passive mixers realize transformation from baseband to $\omega_{0,i}= \omega_{lo} \pm \omega_b$, i=1,2 (see lower part of Fig. 21.1.2).

To drive two BPF paths from one source, the input signal needs to be split. Using capacitive splitting via two times C_s as shown in Fig. 21.1.2 offers several advantages: 1) it isolates the two N-path filters from each other if the impedance of C_s is relatively high compared to 50Ω; 2) it increases the quality factor of each BPF and consequently lowers the value of required C_{BB} for a given BPF-Q; 3) It improves the ultimate rejection of each path. Finally, a second set of switches has been added to further improve the ultimate rejection of each BPF path (Fig. 21.1.2).

The filter also features suppression of signals at even harmonics of f_{lo}. This is because at even harmonics of the clock frequency, the differential baseband voltages ($V_{I1,2}$ and $V_{Q1,2}$ in Fig. 21.1.2) are zero. Therefore, there will be no frequency shift of the two BPF sections and the signal is cancelled in the subtraction. There is folding back from $3f_{lo}$, $5f_{lo}$, ... to f_{lo}[6]. To reduce folding back and filtering at odd ($n\neq1$) harmonics of the f_{lo}, a time-invariant wideband and fixed low-pass pre-filter can be used.

For measurement purposes, two buffer stages have been added. The buffer stages and the differential g_m stages of the filter are shown in Fig. 21.1.3. The baseband capacitors C_{BB} are 20pF, made of accumulation-mode n-type MOS capacitors. The on-resistance of the switches is around 10Ω, the series capacitor C_s is 1pF, and the bandwidth of the filter is 21MHz.

The circuit is realized in 65nm CMOS. The simulated rejection characteristics of a differential 4-path filter [6] (R_{sw}=5Ω and C_{BB}=40pF, the same total capacitor) and the proposed filter have been included for comparison with measurement results (upper part of Fig. 21.1.4). Clearly, the shape factor and maximum filter rejection are improved significantly. Moreover, to check the out-of-band filter shape mismatch, 10 samples have been measured (Fig. 21.1.4, lower part). The measurements in Fig. 21.1.5 show a well-defined band-pass shape and tuneability from 300MHz to 1.2GHz, with an equivalent quality factor Q changing from 14 to 57. The filter characteristics are quite insensitive to strong out-of-band blockers as shown in Fig. 21.1.5 for a continuous-wave blocker of +2dBm at Δf=+50MHz from the center frequency. The only visible change in the filter shape is the reduction of rejection at $2f_{lo}$.

The static and dynamic current draw of the filter are 3.2mA from a 2.5V supply and 12.4mA from a 1.2V supply, respectively (at 1GHz). The LO leakage power to the input port is <-60dBm. The maximum absolute value and the maximum variation of the group delay of the filter are 70ns and 30ns, respectively. The inband 1dB compression point of the filter is -4.4dBm, the inband IIP_3 of the filter is +9dBm and the out-of-band IIP_3 is +29dBm. The input-referred rms noise voltage is 2.66nV/√Hz and the noise figure of the filter is 9.5dB (noise of the buffers, estimated from simulation, has been de-embedded from the noise figure). The main contributors to the noise are the 1/f noise of the g_m stages and the loss in the splitting of the input signal with relatively high-impedance capacitors. The filter noise figure is similar to a typical mixer noise figure and hence an LNA will usually be needed in an antenna filter application. Also, this filter might be used as an IF filter for super-heterodyne architecture, where the IF frequency can be adapted to actual interference conditions.

The die micrograph is shown in Fig. 21.1.7 and the active area of the filter is 0.127mm^2. The filter is compared with [1-6] in Fig. 21.1.6. We even added filtering receivers [4,5] in the comparison table. The proposed filter outperforms Q-enhancement [2] and g_m-C [3] filters from a linearity, noise and tuneability points of view. Compared to [5,6], it has a better pass-band shape and much higher rejection at RF frequencies. Moreover, this work has comparable out-of-band rejection and better pass-band shape compared to [4] where most of the filtering is done in IF stages and the RF filtering is limited.

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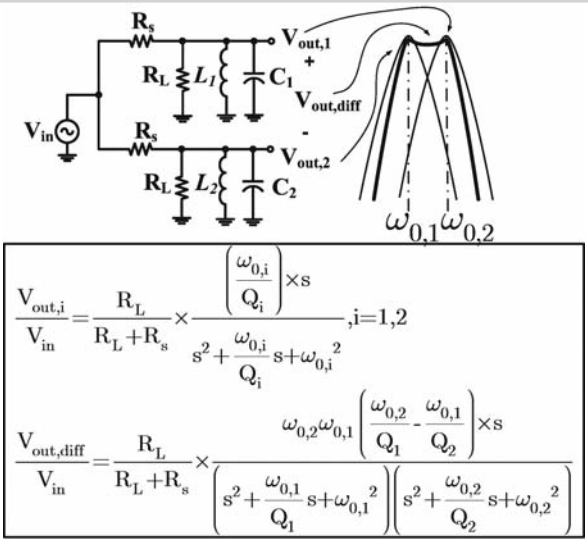

Figure 21.1.1: Subtracting the output voltage of two 2nd-order BPFs with slightly different center frequency to create a 4th-order BPF.

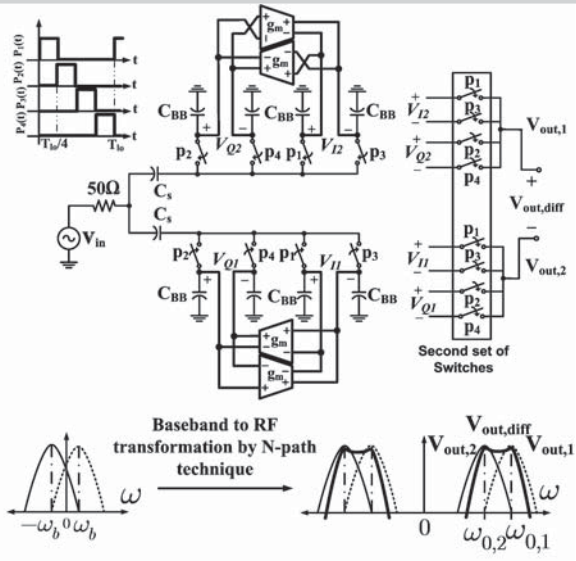

Figure 21.1.2: 4th-order switched g_m-C BPF.

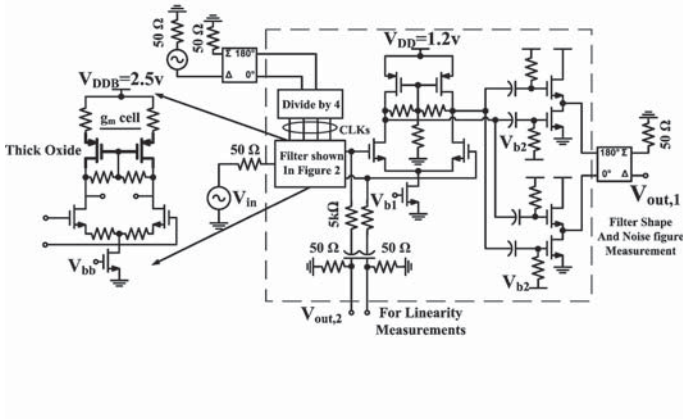

Figure 21.1.3: The complete filter schematic with buffer stages for measurements.

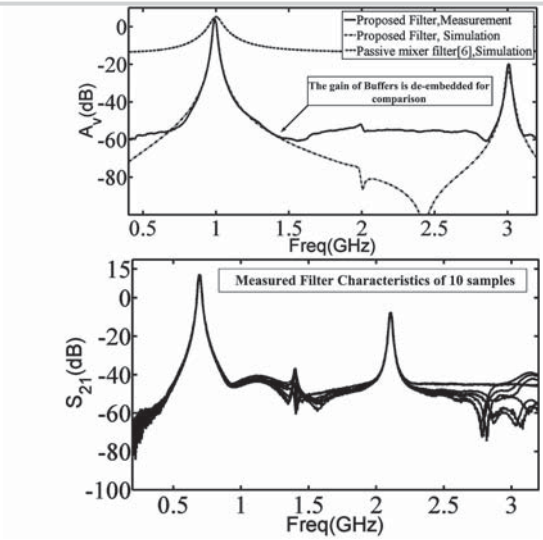

Figure 21.1.4: Comparing measurements with simulation and 4-path filter [6] (top); measured out-of-band filter shape mismatch (bottom).

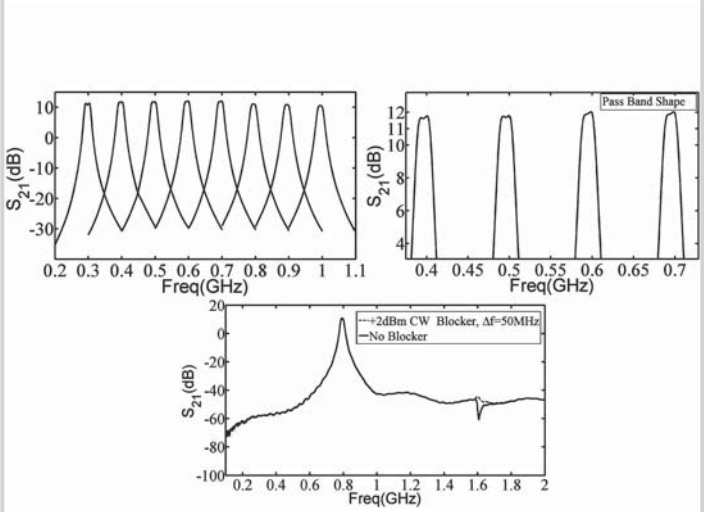

Figure 21.1.5: Measured tuneability of the filter and the filter characteristics w/wo +2dBm CW blocker at Δf=+50MHz from the center frequency.

	[4]	[5]	[6]	[3]	[2]	[1]	[This work]
Type	Receiver	Receiver	Filter	Filter	Filter	Filter	Filter
Technology[g]	65nm	65nm	65nm	65nm	250nm	SiGe BiCMOS250nm BAW piezoelectric	65nm
Center Frequency(GHz)	2.14	0.05-2.4	0.1-1	0.08	2.14	2.14 (±0.15%)	0.3-1.2
Order of filter	6	2	2	4	6	4	4
BW(MHz)	4	20	35	10	60	60	21
Gain (dB)	+55[k]	+70[k]	-1	+2	0	-9	+3.5[b]
Ultimate Rejection (dB)	48[d]	13[i]	16[c]	32	?	28	55
P_{1dB}(in-band)(dBm)	?	?	2	?	-13.4	?	-4.4
IIP_3(in-band)(dBm)	-8.5	-67	+19	-2	-4.9	+35	+9
IIP_3(out-of-band)(dBm)	?	+25	?	?	?	?	+29[L]
NF(dB)	2.8[e]	5.5	5.5	21.5	19	9[f]	9.5[a]
Active Area(mm^2)	0.76	2.5	0.07	0.25	3.51	6.65	0.127
Max. Ripple(dB)	N.A	N.A	N.A	0.1	0.7	1.5	0.5
P_{diss}(mW)	34.2	60	18	13.2	17.5	7	17.6[b]

[a] Buffers noise contribution is de-embedded($V_{in,n,rms}$=2.66nV/√Hz). [e] 10dB on-chip passive gain in Front [i] Calculated from S_{11}
[b] 3.2mA static and 12.4 mA dynamic current consumption @ 1GHz [f] Estimated from the loss of filter [k] Whole receiver gain
[c] R_{on}=5Ω [g] CMOS, unless otherwise stated [L] Δf=50MHz
[d] It is achieved by cascading 3 BPF, of which most filtering is done in IF. [h] De-embedding the buffer's gain.

Figure 21.1.6: Comparison Table.

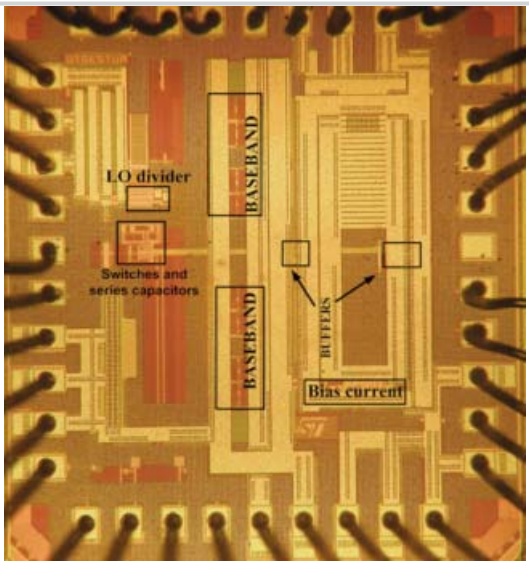

Figure 21.1.7: Chip Micrograph.

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