5.2 Simultaneous Spatial and Frequency-Domain Filtering at the Antenna Inputs Achieving up to +10dBm Out-of-Band/Beam P_{1dB}

Amir Ghaffari, Eric E.A.M. Klumperink, Frank van Vliet, Bram Nauta

University of Twente, Enschede, The Netherlands

Multi-antenna transceivers with beam-forming are recently gaining interest for low GHz frequencies (<6GHz) [1-4]. In the antenna beam, (phase-shifted) signals from multiple antennas add constructively, improving SNR, while out-of-beam signals add destructively (i.e. spatial filtering). Usually the summation point is behind some gain blocks, which then need to be capable of handling strong signals. To improve the input-referred compression point P_{1dB}, a fully passive switched-capacitor approach was presented in [4], providing P_{1dB}=+2dBm, but at a high noise penalty: NF=18dB. Here we propose to sum immediately at the baseband capacitors of passive mixer-first switched-RC downconverters. We show that this can render a direction-dependent RF impedance (spatial filtering) together with RF bandpass frequency filtering at lower noise and higher P_{1dB}.

The proposed architecture is shown in Fig. 5.2.1 for a 4-element phased-array. Four 8-phase passive mixers driven by non-overlapped 1/8 duty-cycle clocks, downconvert the RF signals impinging the 4 antennas on the baseband capacitors. If the RC time constant composed of the real impedance of the antenna and the baseband capacitors is large enough compared to the on-time of the mixer switches, the baseband signals BB_1-BB_8 will be the average of a periodically observed 1/8th fraction of the RF signal. Assuming linearity, superposition holds and signal contributions from the 4 antennas are added. For a particular direction of arrival, these antenna contributions are in phase, so they add up constructively on the capacitors. For other directions, the integration on the capacitors is partly or fully destructive. This can be modeled as a direction-dependent impedance, which due to the transparency of the passive mixers is upconverted to the RF antenna nodes rendering spatial filtering (see Fig. 5.2.2 top). Moreover RC lowpass filtering also occurs on the capacitors, which is also upconverted to the switching frequency and its harmonics rendering high-Q "N-path" frequency domain bandpass filtering [5-7]. In order to rotate the direction of the received beam, a controllable phase shift is required. This is realized in the LO path (see Fig. 5.2.1). An external clock is divided-by-four and by combining different phases, 8 non-overlapped clock phases with a duty cycle of 1/8 are generated. A phase selector with a digital control unit provides 8 freely programmable mixer LO-phases.

Unlike traditional receivers, this one aims at selectivity around the 3rd harmonic of the LO frequency. The baseband voltage signals on the capacitors are converted to current outputs via V-to-I converters. By proper weighting of the G_m blocks the first harmonic is rejected and the third one is received. The procedure of the vector weighting and summation is illustrated in Fig 5.2.2 (note that a delay of 1/8 LO-period renders α at f_{LO}, but 3α at $3f_{LO}$). Third harmonic reception increases the frequency range where power efficiency is larger compared to fundamental reception. Moreover it reduces significantly the on-chip space and real estate for high frequency clock distribution. Although conversion gain is reduced and noise increased, the phased-array principle improves SNR, theoretically up to 6dB for 4 elements. Luckily, for 8-phase mixers the loss is just about 3dB [6]. This happens to be exactly what we need to provide power matching at the mixer input, without special measures as in [4]. The V-to-I converters are realized with self-biased inverters that can tolerate high input swings with a capacitive input impedance. Since the vector summation at the output of the G_m blocks is in the current domain, a Transimpedance Amplifier (TIA) can provide a virtual ground limiting the output voltage swing of the G_m blocks, which improves linearity. For experimental freedom and to be sure we characterize the RF front-end limitations, external TIAs were used.

A prototype was implemented in 65nm CMOS technology (see Fig. 5.2.7). The input clock frequency range is 0.8 to 4.8GHz, which provides 3rd-harmonic reception of 0.6 to 3.6GHz. The constructed beam pattern for broadside reception at 2.4GHz (f_{LO}=800MHz) is shown in Fig. 5.2.3 (equal phase settings). It largely follows the ideal 4-element phased-array (gray line). A blocker at variable incident angle was emulated using 4 RF signal generators with a variable well-controlled phase difference connected to the 4 receivers. The compression point was measured, observing the IF signals. While the measured results show a P_{1dB}=-5.5dBm for zero incident angle, it increases to up to +10dBm at null points, i.e. more than 15dB spatial rejection. The maximum improvement is limited due to the effect of the switch resistance. Note that +10dBm corresponds to $2V_{pp}$ in 50Ω at the input! In Fig. 5.2.3 the constructed beam patterns for 8 uniform electrical phase shifts are presented as polar plots. As expected from phased-array theory, a maximum gain is achieved for the spatial angles 0, ±14.48, ±30, ±48.6 and 90 degrees, corresponding to electrical LO phase shifts of (0, ±45, ±90, ±135, 180 degrees) and antenna physical distance of d=λ/2 where λ is the wavelength of the incident RF signal. The beam patterns are superimposed in a single figure in Fig. 5.2.4 (top-left), showing a maximum gain variation of 0.8dB over different directions. The IF transfer curves for 1 element and 4 elements are shown in Fig. 5.2.4 (top-right). The measured 3dB bandwidth for the single element is 5MHz (10MHz @ RF). In this measurement the external TIAs were replaced by 10Ω differential resistors in order to eliminate TIA bandwidth limitations. When all 4 elements are activated, the effective resistance seen by the capacitors "looking to the antennas" is reduced by a factor of 4 resulting in 4 times larger bandwidth. As shown in Fig. 5.2.4 (top-right) P_{1dB} increases to +11dBm for out-of-band blockers with 4 elements. Measured S_{11} is shown for three switching frequencies in Fig. 5.2.4, consistently giving better than -10dB of S_{11} in the received band. S_{11} is measured with just one element and also 2 elements activation. With 2 elements activated the (common mode) S_{11} shows a broader dip in Fig. 5.2.4, consistent with doubled bandwidth as discussed earlier in this paragraph. This measurement proves that indeed filtering takes place at the antenna inputs. Figure 5.2.5 shows the single element DSB NF of 3 to 6dB. Neglecting the shared noise in the 4 paths generated by G_m blocks, 6dB improvement in SNR is expected. However, noise floor measurements at the output show 4dB instead of 6dB, due to the shared noise of G_m blocks. Simulations show 4.5dB improvement in NF. Analog G_m blocks consume 36mW generating 100mS at I and Q paths. Overall power when 4 elements are activated is 68 to 195mW for the received frequency range of 0.6 to 3.6GHz. The maximum ripple in the gain is 2.5dB and in-beam/band IIP3 varies from +2 to +9dBm (see Fig. 5.2.5). The first harmonic is rejected between 15 and 25dB. The measurement results are compared to three previously reported 4-element phased-array systems. Clearly remarkable P_{1dB} and NF are achieved, and the dynamic range at the antenna inputs is substantially improved compared to previous work.

Acknowledgment:
This research is supported by STW. We thank STMicroelectronics for silicon donation and CMP for their assistance. Also special thanks go to G. Wienk, H. de Vries and M. Soer.

References:
[1] J. Paramesh, et al., "A 1.4V 5GHz Four-Antenna Cartesian-Combining Receiver in 90nm CMOS for Beamforming and Spatial Diversity Applications", *ISSCC Dig. Tech. Papers*, pp. 210-211, Feb. 2005.
[2] R. Tseng, et al., "A Four-Channel Beamforming Down-Converter in 90nm CMOS Utilizing Phase-Oversampling", *IEEE J. Solid State Circuits*, vol. 45, no. 11, pp. 2262 - 2272, Nov. 2010.
[3] M.C.M. Soer, E.A.M. Klumperink, B. Nauta , F.E. van Vliet, "A 1.0-to-4.0GHz 65nm CMOS Four-Element Beamforming Receiver Using a Switched-Capacitor Vector Modulator with Approximate Sine Weighting via Charge Redistribution", *ISSCC Dig. Tech. Papers*, pp. 64-65, Feb. 2011.
[4] M.C.M. Soer, E.A.M. Klumperink, B. Nauta, F.E. van Vliet, "A 1.5-to-5.0GHz Input-Matched +2dBm P_{1dB} All-Passive Switched-Capacitor Beamforming Receiver Front-End in 65nm CMOS", *ISSCC Dig. Tech. Papers*, pp. 174-175, Feb. 2012.
[5] C. Andrews, A.C. Molnar, "A Passive-Mixer-First Receiver with Baseband-Controlled RF Impedance Matching, < 6dB NF, and > 27dBm IIP3", *ISSCC Dig. Tech. Papers,* pp. 46-47, Feb. 2010.
[6] A. Ghaffari, E.A.M. Klumperink, M.C.M. Soer, B. Nauta, "Tunable High-Q N-Path Bandpass Filters: Modeling and Verification", *IEEE J. Solid State Circuits*, vol. 46, no. 5, pp. 998-1010, May 2011.
[7] A. Mirzaei, H. Darabi, D. Murphy, "Architectural Evolution of Integrated M-Phase High-Q Bandpass Filters", *IEEE Trans. Circuits and Systems-I*, vol. 59, no. 1, pp. 52-65, Jan. 2012.

 978-1-4673-4516-3/13/$31.00

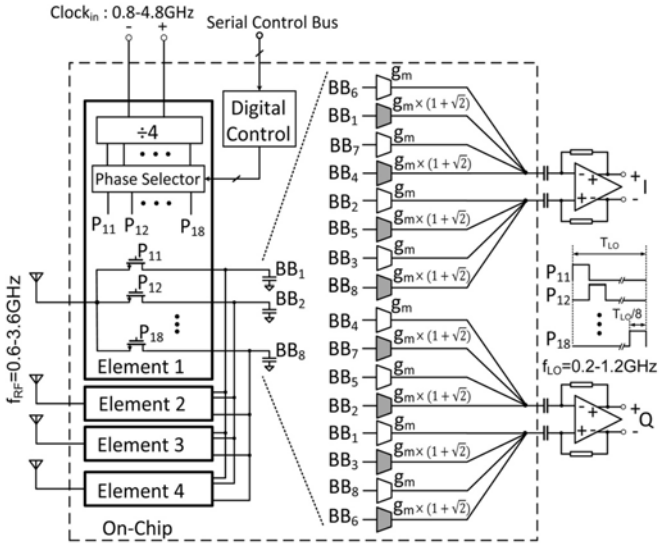

Figure 5.2.1: Block diagram of the 4-element phased-array system.

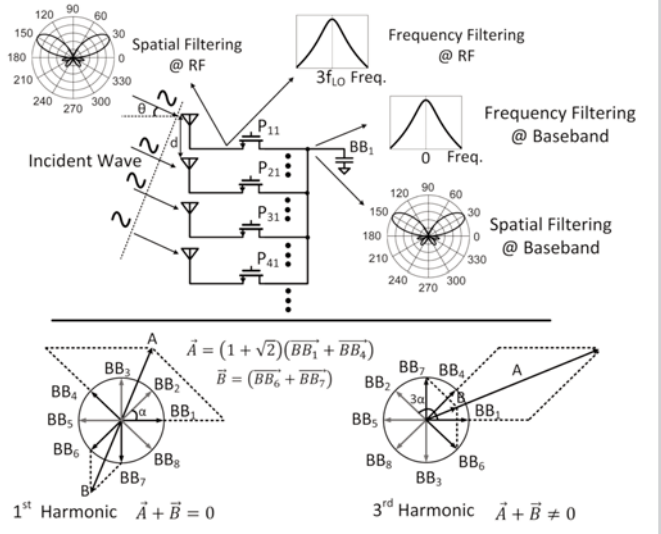

Figure 5.2.2: Spatial and frequency-domain filtering (top) and 3rd-harmonic reception (bottom).

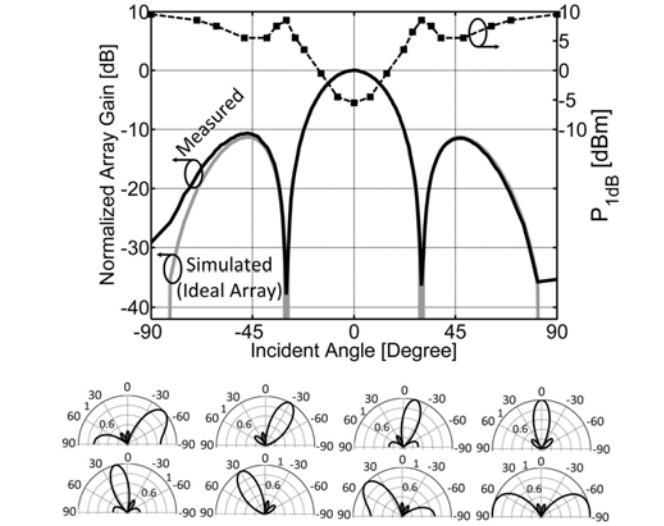

Figure 5.2.3: Beam patterns and P_{1dB} measurement at f=2.4GHz received band (d=λ/2 in Fig. 2.5.2 top).

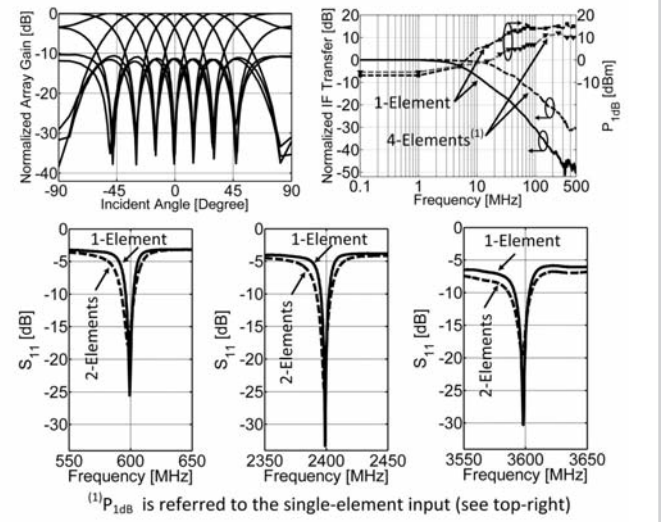

Figure 5.2.4: Beam patterns, IF transfer and P_{1dB} at f=2.4GHz RF frequency, and S_{11}.

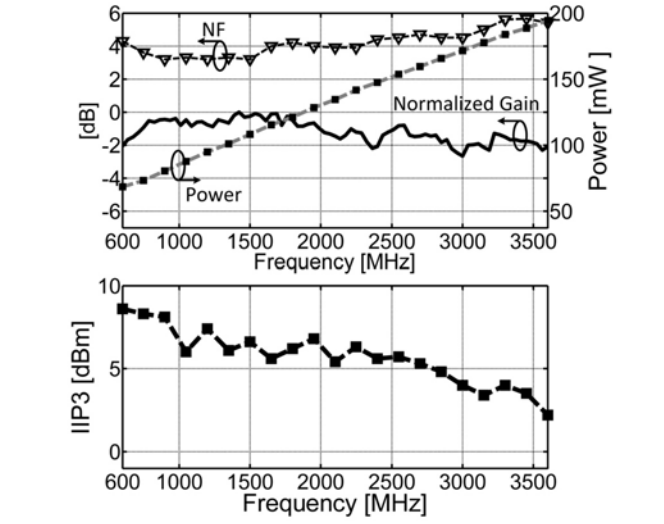

Figure 5.2.5: NF, normalized gain and in-beam/band IIP3 of single-element, and power consumption of 4 elements versus received frequency.

	[2]	[3]	[4]	This Work
Technology	CMOS 90nm	CMOS 65nm	CMOS 65nm	CMOS 65nm
Active Die Area (mm^2)	1.4	0.44	0.18	0.97
RF Frequency (GHz)	4	1-4	1.5-5	0.6-3.6
Phase/Amplitude Resolution (bits)	5 / 3	5 / 3	5 / -	3 / -
4-Elements Power (mW)	166	308	65-168	68-195
1-Element IF Bandwidth (MHz)	NA	65	300	5(1)
1-Element Noise Figure (dB)	13	10	18	3-6
4-Elements SNR Improvement (dB)	6(2)	6(2)	6(2)	4
1-Element Input Referred P$_{1dB}$ (dBm)	NA	-14	2	-5.5 (In-Beam/Band)(3) +10 (Out-of-Beam)(3) +11 (Out-of-Band)(3)
1-Element IIP3 (dBm)	2	-1	13	+2 .. +9 (In-Beam/Band)(3)

(1) IF$_{BW}$=20MHz when 4 elements are activated (see Fig. 5.2.4).

(2) 6dB improvement in SNR is expected but not measured.

(3) Measured with 4-elements, but power is referred to the single-element input.

Figure 5.2.6: Comparison of CMOS 4-element phased-array systems.

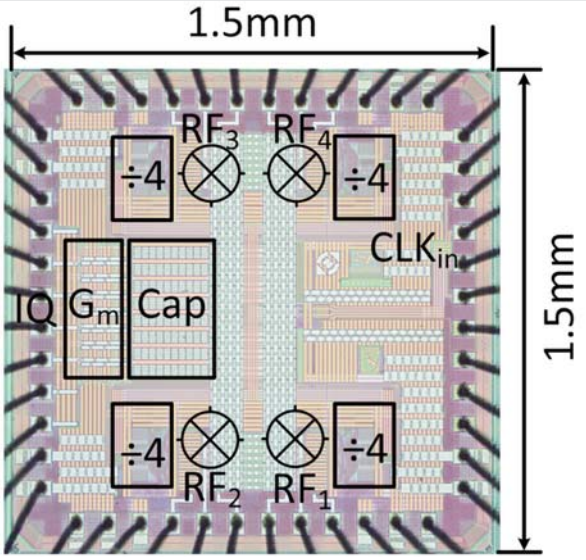

Figure 5.2.7: Die micrograph in 65nm CMOS technology.

 978-1-4673-4516-3/13/$31.00