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8.5 A 93-to-113GHz BiCMOS 9-Element Imaging Array Receiver Utilizing Spatial-Overlapping Pixels with Wideband Phase and Amplitude Control

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Benefiting from aggressive feature size scaling, silicon technologies have recently shown the capability of implementing W-band imaging receivers with an image resolution of 1.5mm and temperature resolutions of less than 0.5K [1-4]. This paper extends the capability of an imaging array receiver by improving image resolution using the novel concept of spatial-overlapping sub-arrays and enhancing image capture time using a phased-array within an imaging array receiver (RX). Specifically, the design and implementation of a BiCMOS 9-element array RX consisting of four 2x2 overlapping sub-arrays is presented. The RF-path-sharing between neighboring sub-arrays leads to a reduction in the chip area by 40% as compared to a conventional imaging array consisting of four 2x2 non-overlapping sub-arrays, while improving the RX's spatial resolution due to the higher sub-array density. Each 2x2 sub-array in this imaging array RX forms a pixel (Fig. 8.5.1).

Figure 8.5.1 shows how a 9-element imaging array can form four sub-arrays, where each 2x2 overlapping sub-array drives a single detector. Each path connecting neighboring antennas and detectors is independently controllable in phase (time delay) and amplitude. The pixel spacing in this architecture is half that of the pixel spacing in non-overlapping 2x2 sub-arrays, resulting in 4x improvement in 2-D image resolution. Moreover, while the proposed architecture has the same pixel spacing as the conventional 9-element imaging array RX where each element forms a pixel, the use of phase/amplitude control (independently) within each element's RF path enables beam-steering, and resolution improvement. This architecture increases directivity for each pixel, thereby improving the RX SNR by as much as 6dB, as shown in Fig. 8.5.2.

A 2x2 sub-array is highlighted and enlarged in Fig. 8.5.1. Each element within a sub-array in this scheme incorporates a bowtie antenna and a wideband LNA. The LNA output of each element is then fed to a 1:4 power splitter comprised of a tree of 1:2 active power splitters. In order to reduce the chip area, the 1:2 active splitters additionally incorporate wideband digitally controllable delay functionality, enabling beam-steering within individual sub-arrays. To provide amplitude control and gain equalization between the different RF paths, the output of each power splitter is fed to a VGA that provides independent gain control for all individual RF paths. Each of the 2x2 sub-array's four VGA RF outputs are combined and fed to a W-band power detector, which is then followed by an integrator.

Each on-chip antenna is designed as a slot bowtie structure with an area of 500x900 μm^2 . On the lowest level metal, a GND shield with narrow slots has been placed below the antenna to decrease leakage into the lossy substrate, thus improving the antenna radiation efficiency. Further improvement of the antenna gain has been obtained by back-grinding the substrate by 50 μm , down to 220 μm . Figure 8.5.2 shows a single antenna's measured normalized radiation pattern in the H-plane with 7 different VGA settings, exhibiting 6dB of amplitude tuning range with 1dB steps. The measured normalized H-plane radiation pattern of a 2x2 sub-array is also shown in Fig. 8.5.2. Beam-steering in the H- and E-planes is made possible by the active power splitter with built-in true-time delay (TTD) functionality. Measured normalized radiation patterns with different pointing angles are shown in Fig. 8.5.2. The TTDs enable the beam pointing angle of each 2x2 sub-array to be varied in the range of ± 18 degrees with 4-degree resolution.

The LNA consists of a four-stage single-ended bandwidth (BW)-enhanced cascode topology (Fig. 8.5.3). Input matching is designed for simultaneous noise and power match, with the first stage current density optimized for minimum NF and the last three stages biased for maximum gain. To reduce the chip area, lumped inductors (rather than T-lines) are used for wideband output as well as inter-stage matching. Wideband matching networks consisting of 4th-order LC high-pass networks were used to increase the overall LNA's BW. BW and gain enhancing T-lines (T_B , T_C and T_E) are used in each stage of the LNA core. The base T-line, T_B , is designed carefully to increase the gain while maintaining

unconditional stability of the LNA (k -factor > 20). The LNA break-out circuit exhibits a measured peak gain of 39dB and a 3dB BW of 20GHz (93 to 113GHz), as shown in Fig. 8.5.3. The LNA draws 19mA from a 1.8V supply, excluding bias.

Figure 8.5.3 shows the topology of the 1:4 power splitter. Each 1:2 power splitter incorporates a broadband delay tuning mechanism, realized by a number of delay cells, each of which is composed of a g_m transistor feeding a complementary transistor pair, distributed along the input and output CPW-based T-lines (Fig. 8.5.3). The delay of each 1:2 splitter is controlled independently by complementary digital signals applied at the inputs (indicated by 1 to 18, and their complements, in Fig. 8.5.3) of the control transistor pairs in each cell [5]. This complementary current steering ensures that the g_m transistor's DC current will remain constant for all delay settings. This guarantees that the parasitic capacitor C_n of the g_m transistor remains constant, thereby maintaining constant impedance of the input/output T-lines for all delay settings. The emitter-degenerating 80 μm T-line resonates out the undesired parasitic capacitance at the collector of the g_m transistor, thereby increasing BW. The circuit layout of this power splitter is designed symmetrically. Therefore, the routing loss from the splitter to combiner is the same for every path. The wideband variable delay of each path is controllable from 0ps to ± 2 ps with 0.45ps steps, corresponding to 0° to $\pm 18^\circ$ for beam-steering with 4° steps (Fig. 8.5.2). Figure 8.5.3 also shows the TTD phase-versus-frequency response for different TTD control settings.

A chip-on-board solution was used to evaluate the system performance. The delay and beam-steering were controlled by the variable TTD blocks. Delay settings are stored in on-chip registers, and controlled off-chip by custom software. Figure 8.5.4 shows the measured responsivity (including on-chip antenna losses) w.r.t. frequency for minimum, nominal, and maximum VGA gain settings. The measured coherent responsivity ranges from 300 to 1100 MV/W, based on the VGA gain setting. Additionally, hot/cold measurements were carried out to experimentally determine the RX performance in a passive setting. The incoherent hot/cold temperature measurements result in an average RX responsivity of 800 MV/W, as shown in Fig. 8.5.4. A noise equivalent temperature difference (NETD) [6] of 0.45K was also measured with the hot/cold test setup. Active images were constructed using a W-Band frequency source. Figure 8.5.5 shows the images from the outputs of the four individual 2x2 sub-arrays, obtained by 4-mm spatial sampling, compared with the image obtained by combining the four overlapping sub-arrays data. It can be visibly seen that the 2-mm over-sampled image results in a sharper image resolution. The complete measured performance of the proposed 9-element array RX consisting of four 2x2 overlapping sub-arrays is summarized in Fig. 8.5.6. The die photo of the proposed fully integrated 9-element array is shown in Fig. 8.5.7.

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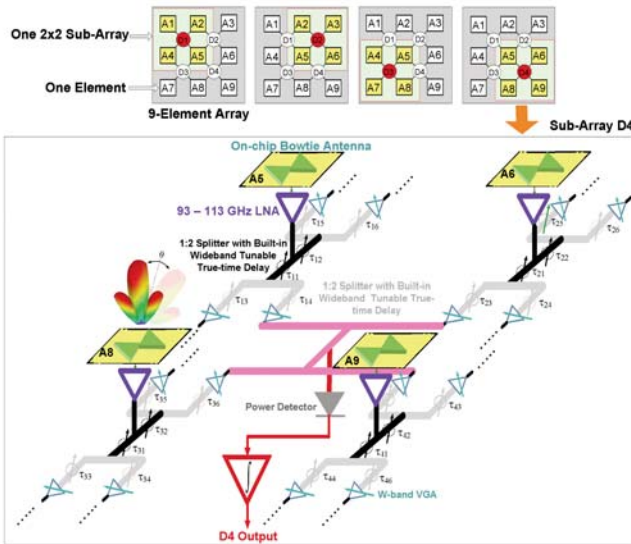


Figure 8.5.1: 9-element imaging array RX diagram; 2x2 sub-array.

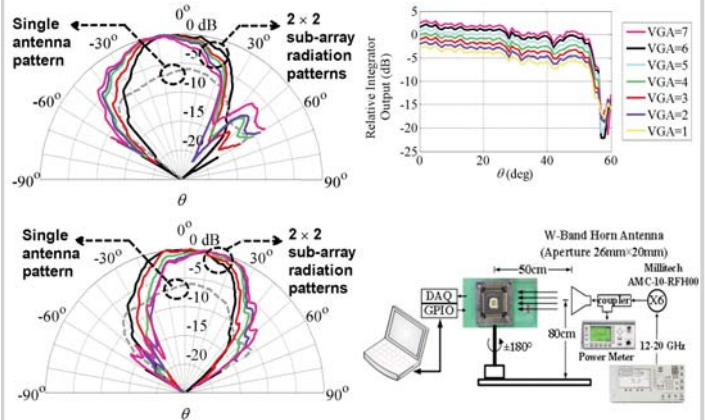


Figure 8.5.2: Measured antenna gain and radiation patterns; test setup.

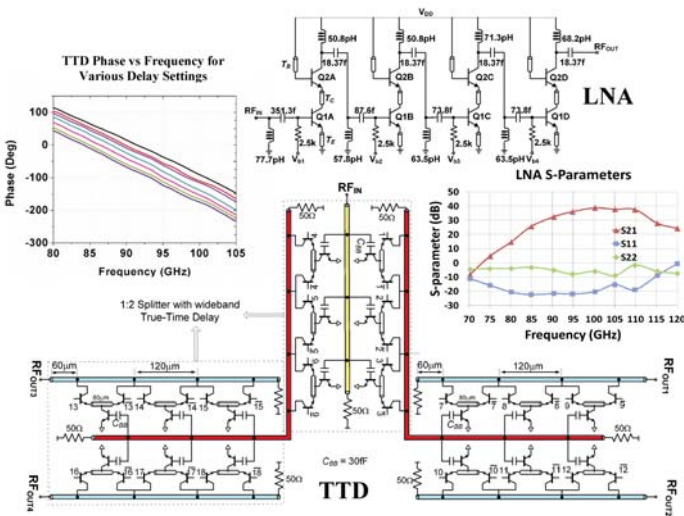


Figure 8.5.3: LNA and TTD schematics and measurement results.

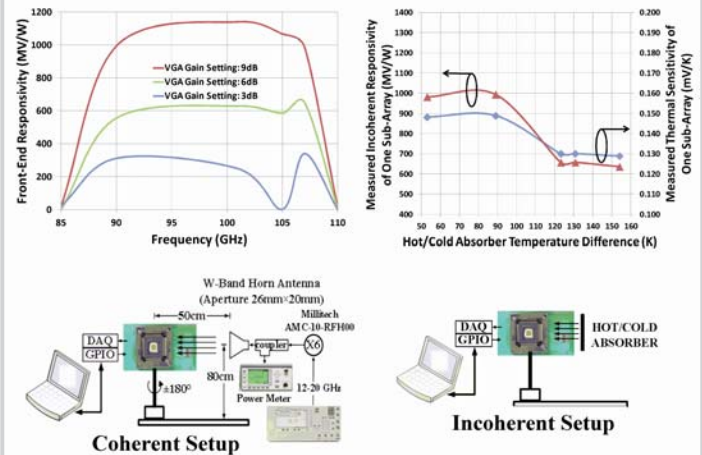


Figure 8.5.4: 2x2 sub-array measurement results; test setups.

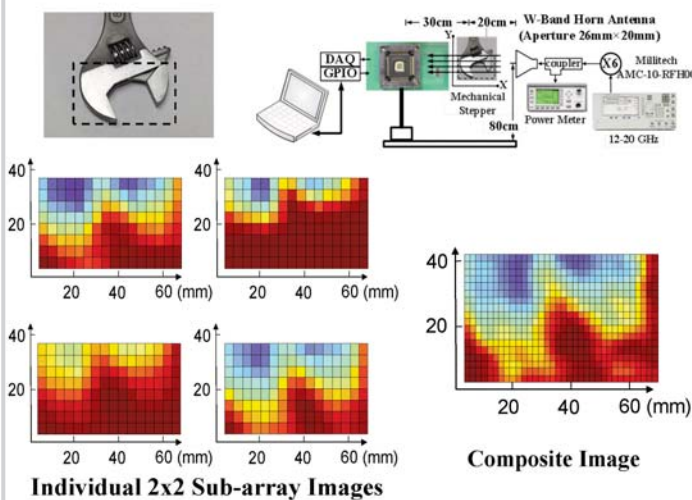


Figure 8.5.5: 2x2 sub-array images; composite image; test setup.

Table I Summary of the Array Performance	
Pre-detection Gain	39 dB
LNA 3-dB Bandwidth	93-113 GHz
Minimum/Maximum Sub-Array Beam-Steering Angle	-18°/+18°
Beam-Steering Resolution	4°
Measured Average Incoherent Responsivity (Passive Hot/Cold Measurement)	800 MV/W
Measured NETD (Averaged Across Multiple Hot/Cold Measurements)	0.45 K
Power Dissipation (W)	2.03 W (225mW for each of the 9 elements)
Process Technology	0.18μm SiGe BiCMOS
Level of Integration	9 On-Chip Antennas forming 4 Overlapping 2x2 Sub-Arrays with Baseband Circuitry
Die Area	6mm×6mm

Table II Performance Comparison of W-Band Imagers					
Reference	Technology	Level of Integration	Integration Time	Responsivity	NETD
[1]	0.13μm SiGe BiCMOS	Dicke Switch + LNA + Detector	30 ms	5 MV/W	0.83 K (Calculated)
[2]	0.18μm SiGe BiCMOS	Dicke Switch + LNA + Detector + Baseband	30 ms	45 MV/W	0.4 K (Calculated)
[3]	65nm CMOS	Dicke Switch + LNA + Detector	30 ms	0.09 MV/W	10 K (Calculated)
[6]	InP HEMT	LNA + Detector Chipset	3.125 ms	0.5 MV/W	0.45 K (Measured)
[4]	0.18μm SiGe BiCMOS	4 Element Focal Plane Array with On-chip Antennas and PLL	30 ms	48 MV/W (283 MV/W not including on-chip antenna loss)	3 K (Calculated)
This work	0.18μm SiGe BiCMOS	9 Element Array with On-chip Antennas and Baseband	20 ms	800 MV/W	0.45 K (Measured)

Figure 8.5.6: Chip performance summary; prior-art comparison.

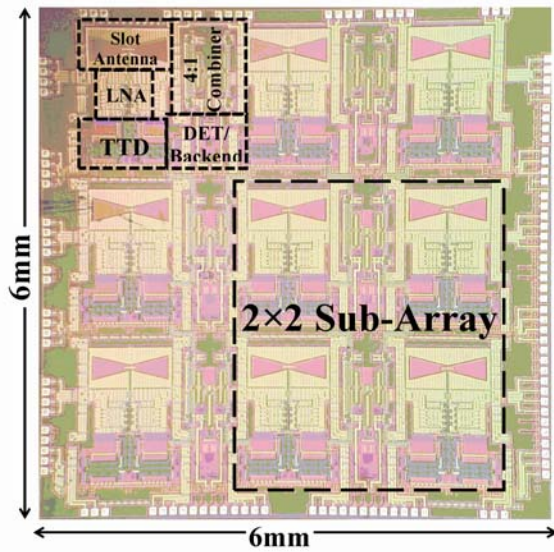


Figure 8.5.7: Die micrograph of 9-element imaging array RX.