Session 5 Overview: *RF Techniques*

RF Subcommittee

Session Chair: *Mike Keaveney*
Analog Devices, Limerick, Ireland

Session Co-Chair: *Joe Golat*
Motorola Solutions, Schaumburg, IL

New circuit architectures continue to evolve to enhance the performance of highly integrated CMOS radios. Cancellation schemes have been implemented to improve immunity to high blocker levels at the receiver front-end. In the transmitter, advancements have been made in efficiency improvement and also in achieving higher output power in deep-submicron CMOS.

1:30 PM

5.1 SAW-Less Analog Front-End Receivers for TDD and FDD

I. Fabiano, University of Pavia, Pavia, Italy

In Paper 5.1, the University of Pavia presents a 0dBm blocker-tolerant SAW-less receiver in 40nm CMOS with +16dBm out-of-band IIP3 and +65dBm IIP2. The receiver also utilizes a current-mode passive mixer with baseband LC series resonance that provides 56/65dB 3rd/5th-order harmonic rejection.

2:00 PM

5.2 Simultaneous Spatial and Frequency-Domain Filtering at the Antenna Inputs Achieving up to +10dBm Out-of-Band/Beam P_{1dB}

A. Ghaffari, University of Twente, Enschede, The Netherlands

In Paper 5.2, the University of Twente demonstrate both spatial and RF filtering techniques to achieve a 4-element phased-array receiver in 65nm CMOS tolerant to +10dBm out-of-band blockers.

2:30 PM

5.3 A Phase-Noise and Spur Filtering Technique Using Reciprocal-Mixing Cancellation

M. Mikhemar, Broadcom, Irvine, CA

In Paper 5.3, Broadcom describes a new architecture capable of minimizing the effects of phase noise and spurs on the receiver NF in the presence of a large blocker. This new topology relaxes the performance requirements of the integrated local oscillator and is implemented in a 40nm CMOS technology.

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3:15 PM

5.4 A 30.3dBm 1.9GHz-Bandwidth 2×4-Array Stacked 5.3GHz CMOS Power Amplifier

M. Fathi, Stanford University, Stanford, CA

In Paper 5.4, Stanford presents a scalable power amplifier array in 65nm CMOS capable of delivering 30.3dBm output power at 5.3GHz with a PAE of 17.8%. The authors utilize both series-parallel transformer combining and transistor stacking to achieve this high level of performance.

3:45 PM

5.5 A 1.8GHz Linear CMOS Power Amplifier with Supply-Path Switching Scheme for WCDMA/LTE Applications

K. Onizuka, Toshiba, Kawasaki, Japan

In Paper 5.5, Toshiba describes a 3.3V linear power amplifier in 65nm CMOS that achieves 27.2dBm output power at 1.8GHz. This PA incorporates a new supply-path switching scheme capable of envelope tracking that improves PAE in the power back-off mode.

4:15 PM

5.6 A New TX Leakage-Suppression Technique for an RFID Receiver Using a Dead-Zone Amplifier

S-S. Lee, KAIST, Daejeon, Korea

In Paper 5.6, KAIST and PHYCHIPS propose a new dead-zone amplifier-based technique for TX leakage suppression into an RFID receiver, at 0.18µm CMOS, improving SNR by up to 15.8dB.

4:45 PM

5.7 A 200mW 100MHz-to-4GHz 11th-Order Complex Analog Memory Polynomial Predistorter for Wireless Infrastructure RF Amplifiers

F. Roger, Scintera, Sunnyvale, CA

In Paper 5.7, Scintera demonstrates an 11th-order analog predistorter with 25dB linearly improvement from 100MHz to 4GHz. This chip consumes less that 200mW from 1.8V and is implemented in 0.18µm CMOS technology.