Session 10 Overview: *Analog Techniques*

Analog Subcommittee

Session Chair: *Jafar Savoj*
Xilinx, San Jose, CA

Session Co-Chair: *Chris Mangelsdorf*
Analog Devices, San Diego, CA

Analog technology continues to defy simple categories. This session illustrates the diversity and vigor of modern analog circuitry. Entries span the range of filters, amplifiers, audio, and oscillators. New frontiers of precision, power, and performance are established.

8:30 AM

10.1 A 0.1-to-1.2GHz Tunable 6th-Order N-Path Channel-Select Filter with 0.6dB Passband Ripple and +7dBm Blocker Tolerance

M. Darvishi, University of Twente, Enschede, The Netherlands

In Paper 10.1, University of Twente presents a 0.1-to-1.2GHz tunable 6th order channel-select filter in 65nm CMOS. It is based on N-path filters coupled with gyrators, achieving a flat pass-band and high out-of-band linearity. It has a NF of 2.8dB, gain of 25dB, and IIP3 of 26dBm. It consumes 11.7mA from a 1.2V supply.

9:00 AM

10.2 A 2mW 800MS/s 7th-Order Discrete-Time IIR Filter with 400kHz-to-30MHz BW and 100dB Stop-Band Rejection in 65nm CMOS

M. Tohidian, Delft University of Technology, Delft, The Netherlands

In Paper 10.2, Delft University of Technology presents a 65nm CMOS 7th-order discrete time IIR filter operating at up to 1GS/s sampling rate. The 3dB bandwidth is tunable between 400kHz to 30MHz and the stop-band rejection is 100dB. The IIP3 is +16dBm and the integrated noise is 12nV/√Hz. The filter consumes 2mW from a 1.2V supply.

9:30 AM

10.3 A Multi-Path Chopper-Stabilized Capacitively Coupled Operational Amplifier with 20V-Input-Common-Mode Range and 3μV Offset

Q. Fan, Delft University of Technology, Delft, The Netherlands

In Paper 10.3, Delft University of Technology presents an outside-the-rail chopper-stabilized opamp. It uses capacitive-coupling to achieve a 20V common-mode range and a multi-path architecture to obtain a smooth transfer function and a step response free of significant chopper-ripple. The opamp achieves 3μV offset, 148dB CMRR and consumes only 8μA from a 5V supply.

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9:45 AM

10.4 A 0.06mm² 14nV/√Hz Chopper Instrumentation Amplifier with Automatic Differential-Pair Matching

I. Akita, Toyohashi University of Technology, Toyohashi, Japan

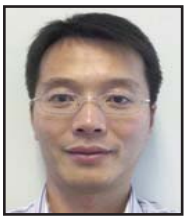
In Paper 10.4, Toyohashi University of Technology and EIIRIS presents a 0.06mm² current-feedback instrumentation amplifier with 32MHz GBW in a standard 0.18μm CMOS. The amplifier uses the chopper-stabilized technique and a novel digital calibration for ripple suppression. The fabricated chip achieves less than 3.5μV offset voltage, 13.5nV/√Hz input-referred noise and 194μA current consumption.

10:15 AM

10.5 A 4Ω 2.3W Class-D Audio Amplifier with Embedded DC-DC Boost Converter, Current-Sensing ADC and DSP for Adaptive Speaker Protection

M. Berkhout, NXP Semiconductors, Nijmegen, The Netherlands

In Paper 10.5, NXP Semiconductors presents a class-D audio amplifier with speaker protection in 0.14μm CMOS. A DC-DC booster provides 2.3W of output power to a 4Ω load. A protection algorithm running on an embedded DSP estimates membrane excursion and voice coil temperature using a speaker model that tracks the speaker impedance.



10:45 AM

10.6 A 62mW Stereo Class-G Headphone Driver with 108dB Dynamic Range and 600μA/Channel Quiescent Current

J. Chen, Broadcom, Irvine, CA

In Paper 10.6, Broadcom and Oregon State University presents a stereo class-G headphone driver for battery-operated mobile devices. The circuit employs a hybrid output stage with an adaptive class-B control scheme to facilitate low quiescent current and low THD. The class-G headphone driver consumes 600μA/channel of quiescent current and achieves 108dB dynamic range, 62mW output power and 50μV pop-and-click noise.

11:00 AM

10.7 A 120nW 18.5kHz RC Oscillator with Comparator Offset Cancellation for ±0.25% Temperature Stability

A. Paidimarri, Massachusetts Institute of Technology, Cambridge, MA

In Paper 10.7, Massachusetts Institute of Technology, Texas Instruments, and MediaTek presents a fully-integrated 18.5kHz RC time-constant-based oscillator in 65nm CMOS for sleep-mode timers in wireless sensors. A comparator offset cancellation scheme achieves 7x temperature stability improvement, leading to an accuracy of ±0.25% over −40 to 90°C and ±0.1% over 0 to 90°C. The oscillator has a long-term Allan stability of 20ppm or better for measurement intervals over 0.5s and consumes only 120nW.

11:15 AM

10.8 A 63,000 Q-Factor Relaxation Oscillator with Switched-Capacitor Integrated Error Feedback

Y. Cao, KU Leuven, Heverlee, Belgium and SCK-CEN, Mol, Belgium

In Paper 10.8, KU Leuven and SCK-CEN presents a relaxation oscillator with the best reported effective Q-factor of 63,000 in 65nm CMOS. It employs a SC integrated error feedback to reduce the close-in phase noise and achieves a FOM of 154dB at 1kHz offset and consumes 82μA from a 1.2V supply. The frequency varies by only ±0.07% over a supply range of 1.1 to 1.5V. From 0 to 80°C, the total frequency variation is within ±0.82%.

11:45 AM

10.9 A 0.45V 423nW 3.2MHz Multiplying DLL with Leakage-Based Oscillator for Ultra-Low-Power Sensor Platforms

D-W. Jee, Pohang University of Science and Technology, Pohang, Korea

In Paper 10.9, Pohang University of Science and Technology and University of Michigan presents an all-digital MDLL for ultra-low-power sensor platforms with a leakage-based oscillator and a fast frequency acquisition scheme for intermittent operation of sensor node platforms. The MDLL is implemented in 65nm CMOS and consumes 423nW at 3.2MHz.