Session 12 Overview: *Non-Volatile Memory Solutions*

Memory Subcommittee

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While the scaling of conventional nonvolatile memories is slowing, emerging memory technologies are starting to show significant technological progress. At the same time, new circuit techniques for existing nonvolatile memories are being introduced to improve reliability and system performance. The papers in this session highlight various technologies from devices to systems, each paper providing potential solutions to its unique challenges.

1:30 PM

12.1 A 130.7mm² 2-Layer 32Gb ReRAM Memory Device in 24nm Technology
T-Y. Liu, Sandisk, Milpitas, CA

In Paper 12.1, Sandisk and Toshiba presents a 32Gb ReRAM test chip developed in 24nm process, with a diode as the selection device. Die efficiency is maximized by utilizing area under the array for supporting circuitry and by sharing wordlines and bitlines between adjacent blocks.

2:00 PM

12.2 40nm Embedded SG-MONOS Flash Macros for Automotive with 160MHz Random Access for Code and Endurance Over 10M Cycles for Data
T. Ito, Renesas Electronics, Itami, Japan

In Paper 12.2, Renesas Electronics presents the first-ever 40nm embedded SG-MONOS Flash macros for automotive applications. A SG-MONOS cell, a split-gate memory cell with charge-trapping storage, and three circuit techniques realize random-read access to the code macros at 5.1GB/s. The memory is reliable even at a junction temperature of 170°C.

2:30 PM

12.3 A 6nW Inductive-Coupling Wake-Up Transceiver for Reducing Standby Power of Non-Contact Memory Card by 500×
N. Miura, Keio University, Yokohama, Japan

In Paper 12.3, Keio University presents an inductive-coupling wake-up transceiver able to reduce by 500× the standby power consumption of non-contact memory cards. The transceiver consumes 6nW standby power with 50×50μm² of silicon area in 0.18μm CMOS technology.

 978-1-4673-4516-3/13/$31.00

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12.4 Time-Differential Sense Amplifier for Sub-80mV Bitline Voltage Embedded STT-MRAM in 40nm CMOS

M. Jefremow, Infineon Technologies, Neubiberg, Germany and Technical University Munich, Munich, Germany

In Paper 12.4, Infineon presents a time-differential-sensing scheme for spin-torque-transfer (STT) MRAM that significantly reduces mismatch effects. This allows the bitline voltage to be reduced to 80mV, increasing the read window with only 23ns read time and 1.1V supply voltage.

3:15 PM

12.5 A 128Gb 3b/cell NAND Flash Design Using 20nm Planar-Cell Technology

G. Naso, Micron, Avezzano, Italy

In Paper 12.5, Micron presents the first ever 128Gb 3b/cell NAND Flash design using 20nm planar cell technology. The planar cell allows the memory cell to be scaled in both the wordline and bitline directions, resulting in the smallest 3b/cell memory device to date. The sensing scheme is able to detect hard and soft states, based on a novel ramping technique.

3:45 PM

12.6 Filament Scaling Forming Technique and Level-Verify-Write Scheme with Endurance Over 10^7 Cycles in ReRAM

A. Kawahara, Panasonic, Kyoto, Japan

In Paper 12.6, Panasonic presents an ReRAM filament-scaling forming technique and level-verify-write scheme with endurance over 10^7 cycles for a 16nm cell. It is realized within a 1T1R ReRAM array. A 2-step forming circuit with self-consistent and current-limiting schemes in 0.11µm technology and 256Kb array is presented.

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12.7 A 45nm 6b/cell Charge-Trapping Flash Memory Using LDPC-Based ECC and Drift-Immune Soft-Sensing Engine

K-C. Ho, Macronix, Hsinchu, Taiwan and National Chiao Tung University, Hsinchu, Taiwan

In Paper 12.7, Macronix presents a 45nm 6b/cell charge-trapping Flash memory using LDPC-based ECC and drift-immune soft-sensing engine. Using multiple techniques the cell is boosted up to 6b/cell and no error remains after LDPC decode over a 10-year lifetime.

4:30 PM

12.8 Cycling Endurance Optimization Scheme for 1Mb STT-MRAM in 40nm Technology

H-C. Yu, TSMC, Hsinchu, Taiwan

In Paper 12.8, TSMC presents a cycling-endurance optimization scheme for 1Mb STT-MRAM in 40nm technology with a dynamic load balance circuit. It improves endurance by maintaining uniform voltage and current across the MTJ and proves a 100K cycling without yield loss.

4:45 PM

12.9 Unified Solid-State-Storage Architecture with NAND Flash Memory and ReRAM that Tolerates 32× Higher BER for Big-Data Applications

S. Tanakamaru, Chuo University, Tokyo, Japan and University of Tokyo, Tokyo, Japan

In Paper 12.9, Chuo University, Japan, presents a solid-state storage architecture that merges NAND Flash memory and ReRAM targeted at big-data applications. The system tolerates a 32× higher BER from the NAND cells by using techniques of reverse-mirroring, error-reduction synthesis, page-RAID, and error-masking.