Session 15 Overview: *Data Converter Techniques*

Data Converter Subcommittee

Session Chair: *Michael Perrott*
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Data converters are critical building blocks for a wide variety of applications. The papers in this session demonstrate improved resolution and power efficiency for data converters in technology spanning from 0.6µm BiCMOS to 28nm CMOS. Wideband continuous-time ΔΣ data converters are brought to new levels of energy efficiency in scaled technology. SAR converters, known for their extreme energy efficiency, are now able to achieve the high resolution claimed by pipeline ADCs. Incremental ADCs achieve high resolution and low power consumption. A static output DAC achieves low noise and sub-ppm INL. These improvements impact a wide range of applications, including next-generation wireless transceivers, ultra-low-power sensors, and advanced medical-imaging systems.

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15.1 A 28fJ/conv-step CT ΔΣ Modulator with 78dB DR and 18MHz BW in 28nm CMOS Using a Highly Digital Multibit Quantizer
Y-S. Shu, MediaTek, Hsinchu, Taiwan

In Paper 15.1, MediaTek presents a continuous-time ΔΣ ADC in 28nm CMOS that achieves a peak SNDR of 73.6dB within an 18MHz bandwidth. 27.7fJ/conv-step energy efficiency is obtained using a highly digital multibit, input-tracking quantizer with embedded feedback to compensate for finite opamp bandwidth and excess loop delay.

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15.2 A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with Data-Driven Noise Reduction
P. Harpe, Eindhoven University of Technology, Eindhoven, The Netherlands

In Paper 15.2, Eindhoven University of Technology demonstrates <3fJ/conv-step power efficiency with a SAR design operating at 0.6V in 65nm CMOS. The converter can be configured for 10b or 12b operation at 40kS/s. A data-driven technique utilizes multiple comparator operations to reduce the impact of comparator noise.

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15.3 A 71dB-SNDR 50MS/s 4.2mW CMOS SAR ADC by SNR Enhancement Techniques Utilizing Noise
T. Morie, Panasonic, Moriguchi, Japan

In Paper 15.3, Panasonic utilizes enhancement techniques such as dithering and adaptive averaging to achieve 71dB SNDR (at low input frequencies) with a 50MS/s SAR structure. Implemented in 90nm CMOS, this converter consumes only 4.2mW.

 978-1-4673-4516-3/13/$31.00

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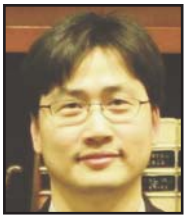
15.4 A 1V 14b Self-Timed Zero-Crossing-Based Incremental ΔΣ ADC

C. Chen, Delft University of Technology, Delft, The Netherlands

In Paper 15.4, Delft University of Technology introduces an asynchronous incremental ADC in 0.16µm CMOS featuring switched-capacitor zero-crossing-based integrators. 14b resolution is achieved in a conversion time of less than 1ms, drawing only 20µA from a 1V supply.



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15.5 A 6.3µW 20b Incremental Zoom-ADC with 6ppm INL and 1µV Offset

Y. Chae, Yonsei University, Seoul, Korea

In Paper 15.5, Delft University of Technology (with presenter now with Yonsei University) presents an incremental ADC in 0.16µm CMOS that utilizes a second-order discrete-time ΔΣ loop to digitize the residue of a 6b SAR quantizer. 21b resolution is achieved with 1µV offset at a power consumption of 6.3µW.

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15.6 A 20b Clockless DAC with Sub-ppm-Linearity 7.5nV/√Hz-Noise and 0.05ppm/°C-Stability

R. C. McLachlan, Analog Devices, Edinburgh, United Kingdom

In Paper 15.6, Analog Devices demonstrates a DAC for low frequency signals at 20b resolution with a noise performance of 7.5nV/√Hz above 10Hz and a stability of 0.05ppm/°C. Code-dependent calibration enables sub-ppm INL, and the structure provides a ±10V output range in 0.6µm BiCMOS with a settling time of 1µs.

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15.7 A 2.4-to-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with Charge-Average Switching DAC in 90nm CMOS

C-Y. Liou, National Tsing Hua University, Hsinchu, Taiwan

In Paper 15.7, National Tsing Hua University utilizes a SAR architecture in 90nm CMOS to achieve scalable operation from 0.5 to 4MS/s from a supply voltage of 0.4 to 0.7 V while maintaining an SNDR greater than 54dB. A charge-average switching DAC enables an energy efficiency between 2.4 and 5.2fJ/conversion-step across these operating conditions.

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15.8 Adaptive Cancellation of Gain and Nonlinearity Errors in Pipelined ADCs

Y. Miyahara, Asahi Kasei Microdevices, Atsugi, Japan

In Paper 15.8, Asahi Kasei Microdevices (with UCSD) leverage an auxiliary amplifier stage to provide nonlinear correction and noise cancellation to achieve 73.3dB SNDR in a 14b pipelined ADC running at 60MS/s. The chip is implemented in 0.18µm CMOS and consumes 68mW from a 1.6V supply.