Session 18 Overview: *Advanced Embedded SRAM*

Memory Subcommittee

Session Chair: *Michael Clinton*
Texas Instruments, Dallas, TX

Session Co-Chair: *Atsushi Kawasumi*
Toshiba, Kawasaki, Japan

SRAM scaling continues with the introduction of a 20nm SRAM using the smallest bit cell reported to date. In addition to scaling, power dissipation continues to be a challenge for SRAM designers. Three of the other papers in this session describe different approaches that significantly reduce active and static power. One design exploits an application-specific solution, the second simultaneously reduces active and static power, and the third uses a fine-granularity-power-gating scheme. While scaling and power reduction are important, one of the most significant aspects of SRAM is performance. The final paper reports on the fastest L1 cache performance ever achieved.

 978-1-4673-4516-3/13/$31.00

10:15 AM

18.1 A 20nm 112Mb SRAM in High-κ Metal-Gate with Assist Circuitry for Low-Leakage and Low-V_{MIN} Applications

J. Chang, TSMC, Hsinchu, Taiwan

In Paper 18.1, TSMC describes the first 20nm SRAM with the smallest bit cell of 0.081μm² demonstrated to date and achieves 200mV lower V_{MIN} by utilizing innovative read and write assist techniques.

10:45 AM

18.2 An SRAM Using Output Prediction to Reduce BL-Switching Activity and Statistically-Gated SA for up to 1.9× Reduction in Energy/Access

M. E. Sinangil, Nvidia, Bedford, MA

In Paper 18.2, researchers from Nvidia and MIT describe an SRAM operating at 0.6V that further reduces energy/access by 1.9× by exploiting application-specific techniques to reduce bitline switching activity. They also employ statistically-gated sense amplifiers.

11:15 AM

18.3 A 27% Active and 85% Standby Power Reduction in Dual-Power-Supply SRAM Using BL Power Calculator and Digitally Controllable Retention Circuit

F. Tachibana, Toshiba, Kawasaki, Japan

In Paper 18.3, Toshiba describes a 28nm SRAM with a 0.12μm² bit cell that utilizes a BL power calculator to reduce active power by 27% and a digitally controllable scheme to control the cell retention voltage resulting in 85% lower standby power consumption.

11:45 AM

18.4 A 64Mb SRAM in 22nm SOI Technology Featuring Fine-Granularity Power Gating and Low-Energy Power-Supply Partition Techniques for 37% Leakage Reduction

H. Pilo, IBM, Essex Junction, VT

In Paper 18.4, IBM describes a 22nm SOI SRAM operating over a wide voltage range of 0.7 to 1.1V and employs a fine granularity power gating feature which reduces bit cell leakage by 37% and also reduces peripheral circuit leakage by 40%.

12:00 PM

18.5 7GHz L1 Cache SRAMs for the 32nm zEnterprise™ EC12 Processor

J. D. Davis, IBM, Poughkeepsie, NY

In Paper 18.5, IBM describes a 32nm L1 Cache SRAM that achieves 7GHz operation by using a 3-level bitline hierarchy and makes extensive use of dynamic circuit design techniques.