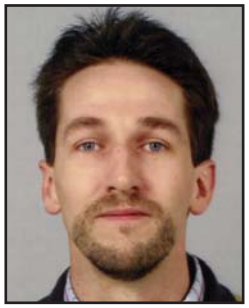
Session 23 Overview: *Short-Reach Links, XCVR Techniques, & PLLs*

Wireline Subcommittee



Session Chair: *Gerrit W. den Besten*
NXP Semiconductors,
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Renesas Electronics,
Kawasaki, Japan

Advances in high-speed short-reach interfaces are essential for on-chip, chip-to-chip, and board-to-board links, in order to satisfy demands for continuously increasing data transfer capacity. Different I/O techniques are required for different applications, but common critical factors are low power consumption and small area. This session includes several papers focused on short-reach link innovations, new approaches to realizing key link components, and additionally two papers describing new PLL techniques.

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23.1 A 0.1pJ/b 5-to-10Gb/s Charge-Recycling Stacked Low-Power I/O for On-Chip Signaling in 45nm CMOS SOI
Y. Liu, IBM T. J. Watson, Yorktown Heights, NY

In Paper 23.1, IBM describes a charge-recycling stacked I/O for on-chip interconnects in 45-nm CMOS SOI, providing power efficiencies of 0.08-to-0.13pJ/b for on-chip interconnects between 1-to-6.5mm and data rates from 5-to-10Gb/s.

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23.2 A Scalable 0.128-to-1Tb/s 0.8-to-2.6pJ/b 64-Lane Parallel I/O in 32nm CMOS
M. Mansuri, Intel, Hillsboro, OR

In Paper 23.2, Intel shows a scalable 64-lane chip-to-chip I/O with 1Tb/s aggregate bandwidth. Per-lane data rates of 2-16 Gb/s and power efficiencies of 0.8-to-2.6pJ/bit are demonstrated in 32nm CMOS, with a total demonstrated bus-level power consumption of 2.6W.

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23.3 A 0.54pJ/b 20Gb/s Ground-Referenced Single-Ended Short-Haul Serial Link in 28nm CMOS for Advanced Packaging Applications
J. W. Poulton, Nvidia, Durham, NC

In Paper 23.3, NVidia describes a new ground-referenced single-ended 20Gb/s serial link for short-haul die-to-die communications over high density interconnect on a laminated package. This link is fabricated in 28nm CMOS, operates from a 0.9V supply and has a power efficiency of 0.54pJ/b.

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23.4 A 5.5Gb/s 5mm Contactless Interface Containing a 50Mb/s Bidirectional Sub-Channel Employing Common-Mode OOK Signaling

K. Hijioka, Renesas Electronics, Kawasaki, Japan

In Paper 23.4, Renesas presents a contactless interface between modules using a coupler-in-package, achieving a BER $<10^{-12}$ over a 5mm distance. Implemented in 0.18μm CMOS, the differential 5.5Gb/s TX+RX consume 104 and 94 mW and the common-mode 50Mb/s TX+RX consume 9 and 5.4 mW.

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23.5 An 8Gb/s 1.5mW/Gb/s 8-Tap 6b NRZ/PAM-4 Tomlinson-Harashima Precoding Transmitter for Future Memory-Link Applications in 22nm CMOS

M. A. Kossel, IBM, Rüschlikon, Switzerland

In Paper 23.5, IBM presents a pipelined half-rate 8-tap NRZ/PAM-4 Tomlinson-Harashima precoder with 6b resolution in 22nm SOI CMOS. Using this design, 8Gb/s PAM-4 data is transmitted over a 34cm PCB channel at a power efficiency of 1.5pJ/bit and 5× ISI-reduction is achieved for 4.0Gb/s NRZ signaling.

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23.6 An 8Gb/s 0.65mW/Gb/s Forwarded-Clock Receiver Using an ILO with Dual Feedback Loop and Quadrature Injection Scheme

J-H. Seol, KAIST, Daejeon, Korea

In Paper 23.6, KAIST describes a low-power receiver using an ILO with dual feedback loop and quadrature injection scheme, which reduces jitter-transfer bandwidth by 4× and phase error from 18° to 3°. Fabricated in 0.13μm CMOS, it achieves an 8Gb/s data rate at a power efficiency of 0.65pJ/bit.

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23.7 A 3.1mW Phase-Tunable Quadrature-Generation Method for CEI 28G Short-Reach CDR in 28nm CMOS

K. Bhardwaj, Stanford University, Stanford, CA

In Paper 23.7, Stanford presents a quadrature clock generation and phase interpolation technique using parametric capacitance modulation. Applied in a dual-loop 28Gb/s CDR in 28nm CMOS, the block achieves 1.5° phase resolution, consumes 3.1mW at 13.5GHz, and exhibits a BER $<10^{-12}$ from 23.2 to 27Gb/s.

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23.8 A Divider-Less Sub-Harmonically Injection-Locked PLL with Self-Adjusted Injection Timing

I-T. Lee, National Taiwan University, Taipei, Taiwan

In Paper 23.8, National Taiwan University shows a divider-less sub-harmonically injection-locked 2.4GHz phase-locked loop in a 65nm CMOS process. The phase noise is -126 dBc/Hz at a 1MHz offset, while the integrated jitter is 188fsrms. It consumes 5.2 mW from a 1.2V supply, and has a FOM of -247 dB.

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23.9 A Wideband Fractional-N Ring PLL with Fractional-Spur Suppression Using Spectrally Shaped Segmentation

T-K. Kao, MediaTek, Hsinchu, Taiwan

In Paper 23.9, MediaTek describes a 1.9GHz fractional-N PLL employing a noise shaping segmentation technique which suppresses fractional spurs by 26dB within the 2MHz PLL bandwidth. Die area of the 40nm CMOS implementation is $0.055mm^2$.