Session 26 Overview: *High-Speed Data Converters*

Data Converters Subcommittee

Session Chair: *Boris Murmann*
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Technology scaling and advances in design are enabling complex systems that thrive on high-performance data converters. Such systems cover applications including Gigabit Ethernet, radar, wireless transceivers, high-speed instrumentation, set-top boxes, and more. Related to the demands of these applications, this session will highlight the latest achievements at sampling rates up to 10.3GS/s and 6-to-14 bits of resolution. The collection of data converters selected for this session exhibit unprecedented combinations of speed, resolution and power efficiency.

1:30 PM

26.1 A 10.3GS/s 6b Flash ADC for 10G Ethernet Applications
S. Verma, Broadcom, Santa Clara, CA

In Paper 26.1, Broadcom presents a 10.3GS/s, 6b flash ADC in 40nm CMOS, with an FoM of 0.7pJ/conv-step. Four-way interleaving, along with dynamic reconfiguration of the comparator order, enables a DSP-based receiver for 10G Ethernet standards.

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26.2 An 11b 3.6GS/s Time-Interleaved SAR ADC in 65nm CMOS
E. Janssen, NXP Semiconductors, Eindhoven, The Netherlands

In Paper 26.2, NXP introduces a 3.6GS/s 11b 4×16 time-interleaved SAR ADC implemented in 65nm CMOS. An on-chip calibration of gain and offset enables the digitization of 2.5GHz inputs with a THD better than –55dB.

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26.3 A 14b 2.5GS/s 8-Way-Interleaved Pipelined ADC with Background Calibration and Digital Dynamic Linearity Correction
B. Setterberg, Agilent Technologies, Santa Clara, CA

In Paper 26.3, Agilent presents an 8× time-interleaved 14b pipelined ADC running at 2.5GS/s for highly reliable measurement equipment applications. The chip exhibits 78dB SFDR over a 1GHz bandwidth and is demonstrated in a 0.13μm SiGe BiCMOS technology with better than 10^{-17} metastability rate.

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26.4 A 3.1mW 8b 1.2GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 32nm Digital SOI CMOS

L. Kull, IBM Research, Rüschlikon, Switzerland and EPFL, Lausanne, Switzerland

In Paper 26.4, IBM (with EPFL) describes a single-channel 8b, 1.2GS/s asynchronous SAR ADC for high-speed data link applications in 32nm SOI technology. Using two alternating comparators with a redundant capacitive DAC, the design consumes only 3.1mW from a 1V supply, yielding an energy efficiency of 34fJ/conv-step.

3:45 PM

26.5 An 8.6 ENOB 900MS/s Time-Interleaved 2b/cycle SAR ADC with a 1b/cycle Reconfiguration for Resolution Enhancement

H-K. Hong, KAIST, Daejeon, Korea

In Paper 26.5, KAIST (with Samsung) introduces a 9b 900MS/s 2-channel time-interleaved SAR ADC. This design utilizes both 2b and 1b/cycle conversions and achieves 8.6 ENOB in 45nm CMOS with an energy efficiency of 40fJ/conv-step.

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26.6 A 14b 80MS/s SAR ADC with 73.6dB SNDR in 65nm CMOS

R. Kapusta, Analog Devices, Wilmington, MA

In Paper 26.6, Analog Devices demonstrates a 14b 80MS/s asynchronous SAR ADC in 65nm CMOS. The circuit features a 2-channel time-interleaved architecture with random shuffling among 3 DACs to relax residual mismatches, thereby yielding 73.6dB SNDR.

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26.7 A 12b 1.6GS/s 40mW DAC in 40nm CMOS with >70dB SFDR over Entire Nyquist Bandwidth

W-T. Lin, National Cheng Kung University, Tainan, Taiwan

In Paper 26.7, National Cheng-Kung University presents a 12b 1.6GS/s current-steering DAC in 40nm CMOS. By combining dynamic element-matching and return-to-zero signaling, this DAC demonstrates >70dB SFDR over the entire Nyquist zone with 40mW power dissipation.