Session 27 Overview: *Image Sensors*

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

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Image sensors continue to evolve and are used in an ever-wider variety of applications. This session highlights sensors that are intended to be used in distributed wireless network nodes, medical imaging, and 3D imaging suitable for both machine vision and the consumer market. Recent advancements in mass production of 3D stacked image sensors are also presented.

1:30 PM

27.1 A 3.4μW CMOS Image Sensor with Embedded Feature-Extraction Algorithm for Motion-Triggered Object-of-Interest Imaging

J. Choi, University of Michigan, Ann Arbor, MI

In Paper 27.1, the University of Michigan reports a 256×256 CMOS imager with integrated feature-extraction capability, to identify objects of interest. The on-chip feature extraction reduces the amount of data that has to be transferred by 96.5%. The chip operates at 0.22μW/frame in motion-sensing mode and at 3.4μW/frame for feature extraction.

2:00 PM

27.2 A 467nW CMOS Visual Motion Sensor with Temporal Averaging and Pixel Aggregation

G. Kim, University of Michigan, Ann Arbor, MI

In Paper 27.2, the University of Michigan proposes a 128×128 CMOS imager with in-pixel motion detection. Spatial aggregation of pixels and temporal averaging are implemented to minimize blindspots and increase sensitivity to slow motion. The 130nm test chip consumes 467nW while performing motion detection. Full-frame images with 38.5dB dynamic range are captured at 6.4fps while consuming 16μW.

2:30 PM

27.3 A Rolling-Shutter Distortion-Free 3D Stacked Image Sensor with -160dB Parasitic Light Sensitivity In-Pixel Storage Node

J. Aoki, Olympus, Hachioji, Japan

In Paper 27.3, Olympus presents a 704×512 rolling-shutter, distortion-free, 3D stacked image sensor with in-pixel storage nodes. The two semiconductor substrates, one with a backside-illuminated photodiode array and one with a storage-node array, are connected with interconnects spaced 8μm apart. The interconnection yield is over 99.9%. A parasitic light sensitivity of -160dB is achieved.

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27.4 A 1/4-inch 8Mpixel Back-Illuminated Stacked CMOS Image Sensor

S. Sukegawa, Sony, Atsugi, Japan

In Paper 27.4, Sony presents an 8Mpixel back-illuminated 3D stacked image sensor. The top substrate consists of an image sensor, implemented using a 90nm CIS process, and the bottom substrate of a logic chip implemented using a 65nm logic process. The substrate interconnect is made with TSVs at the edges of the substrates. The logic chip comprises of an equivalent of 2400k gates. The imager also supports interlaced HDR and RGBW color filter pattern. The HDR mode extends the dynamic range by 24dB.

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27.5 An 8×16-pixel 92kSPAD Time-Resolved Sensor with On-Pixel 64ps 12b TDC and 100MS/s Real-Time Energy Histogramming in 0.13µm CIS Technology for PET/MRI Applications

L. H. C. Braga, Fondazione Bruno Kessler, Trento, Italy

In Paper 27.5, Fondazione Bruno Kessler (with STMicroelectronics and the University of Edinburgh) reports an 8×16 pixel array based on CMOS miniature silicon photomultiplier (MiniSiPM) detectors for PET/MRI applications. The pixel size is 610×570µm^2 and contains 4 digital MiniSiPMs, with a total of 720 SPADs. Energy and time are handled in-pixel by two 7b counters, two 12b 64ps TDCs, accumulator, and FIFOs. The fill factor is 42.9%. An overall system timing resolution of 263ps FWHM is achieved.

3:45 PM

27.6 A 0.18µm CMOS SoC for a 100m-Range 10fps 200×96-Pixel Time-of-Flight Depth Sensor

C. Niclass, Toyota Central R&D Labs, Nagakute, Japan

In Paper 27.6, Toyota Central R&D Labs introduces a CMOS SoC that performs time-correlated single-photon counting and complete DSP for a 100m-range time-of-flight sensor. A relative precision of 0.3% and 0.13% at 10fps and 5fps, respectively, are achieved over the full range and an ambient light level of 70klux.

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27.7 3D Camera Based on Linear-Mode Gain-Modulated Avalanche Photodiodes

O. Shcherbakova, University of Trento, Trento, Italy and Fondazione Bruno Kessler, Trento, Italy

In Paper 27.7, University of Trento (with Fondazione Bruno Kessler) reports a range image sensor based on gain-modulated avalanche photodiodes operated in the linear region. The pixel has a 30×x30µm^2 size with a fill-factor of 25.7% and a demodulation contrast exceeding 80% at 200MHz modulation frequency. A 3D camera using an LED illumination unit modulated at 25MHz is demonstrated, showing a best precision of 1.9cm and a frame rate up to 200fps.

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27.8 A 3D Vision 2.1Mpixel Image Sensor for Single-Lens Camera Systems

S. Koyama, Panasonic, Nagaokakyo, Japan

In Paper 27.8, Panasonic reports a 2.1Mpixel stereo 3D CMOS image sensor with on-chip lenticular lenses and buried sub-wavelength optics. The pixel pitch is 2.75µm, and a crosstalk of 6.3% is achieved.

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27.9 A 187.5µV$_{rms}$-Read-Noise 51mW 1.4Mpixel CMOS Image Sensor with PMOSCAP Column CDS and 10b Self-Differential Offset-Cancelled Pipeline SAR-ADC

J. Deguchi, Toshiba, Kawasaki, Japan

In Paper 27.9, Toshiba presents a 1.4Mpixel CMOS image sensor in a 0.13µm 2P4M CMOS technology. The CDS circuitry uses 1.5V PMOSCAPS with body terminal control to reduce area and power consumption. Furthermore, a 10b pipeline SAR-ADC with an implementation scheme resulting in an 80% reduction of switching power, and 50% reduction of the CDAC area. The read noise and power consumption are 187.5µV$_{rms}$ and 51mW, respectively, at 17fps.