17.1 An Integrated 80V 45W Class-D Power Amplifier with Optimal-Efficiency-Tracking Switching Frequency Regulation

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Piezoelectric actuators are widely used in smart materials for vibration and noise control, precision actuators, etc. [1]. These actuators are largely capacitive and the reactive power applied on them can go to several tens of Watts. High-voltage, high-power class-D amplifiers [2]-[5] are ideal drivers for such loads, because of their high power efficiency. Preferably, efficiency should be high both at maximum power and at average output power. Obtaining high power efficiency over the full output power range of a class-D amplifier is the main focus of this work.

Figure 17.1.1 shows a typical high-voltage class-D power stage, where two identical n-type DMOS FETs are used as both high-side (HS) and low-side (LS) power switches with their gate-driver supply voltage V_{DD} being much lower than V_{DDP} [2]-[5]. The three main dissipation sources in the power stage are then: 1) Conduction loss P_{con} caused by the output current I_{out} due to r_{on} switch resistance; 2) Ripple loss P_{Irip} caused by the inductor ripple current I_{rip} due to r_{on} and magnetic core loss of L_{out}; 3) Switching loss P_{sw} at the V_{pwm} node caused by M_{HS}/M_{LS} having to charge/discharge C_p in Fig. 17.1.1. This can be significant for high V_{DDP}, since the energy stored in C_p is proportional to V_{DDP}^2.

There are two scenarios for P_{sw}, depending on I_{rip} and I_{out}. In the first case, for low I_{out}, the inductor ripple current I_{rip} is large enough for the total inductor current $I_L=I_{rip}+I_{out}$ to be bidirectional. Then, when $I_{rip}>|I_{out}|+C_pV_{DDP}/t_d$, I_L can fully charge and discharge C_p during the dead time t_d without resorting to M_{HS}/M_{LS}. This is the soft switching case where P_{sw} is eliminated. P_{Irip} is now the main dissipation source, and the switching frequency, f_{sw}, should be high to reduce I_{rip} and thus P_{Irip}. In the second case, when $|I_{out}|>I_{rip}$, I_L is unidirectional and one of the V_{pwm} switching transitions has to be finished by M_{HS}/M_{LS}. This is the hard switching case where P_{con} and P_{sw} are dominant. In this case, the power MOSFET sizing for balanced P_{con} and P_{sw} plays a role, which benefits from choosing a low f_{sw} to reduce P_{sw}. The two cases above have contradicting demands on f_{sw}. Common practice is to set f_{sw} in between as a compromise [3], but this is not optimal.

Varying f_{sw} can achieve higher efficiency over a larger output power range as in [6] and [7], but both techniques choose f_{sw} based on output current only. This is suboptimal since the dissipation is highly dependent on both I_{rip} and I_{out}, and there are numerous factors causing I_{rip} variation, apart from external factors like V_{DDP} and L_{out} values. This is especially the case for class-D designs where I_{rip} changes by a factor >5 in the 0.05-0.95 duty cycle (D) range.

We propose to regulate the I_{rip} amplitude such that both P_{sw} and P_{Irip} are minimized by changing f_{sw} based on the V_{pwm} level at the turn-on transition of the power switches. This information is directly related to the dissipation sources and can be used to obtain the optimal f_{sw}, independent of circuit operating conditions affecting I_{rip}. The result is a class-D amplifier with its f_{sw} adapted to achieve minimal dissipation from idle to maximum output power.

Figure 17.1.2 shows the working principle. On the left are the soft switching waveforms, with I_{rip} larger than necessary for eliminating P_{sw}. Both V_{pwm} transitions finish within the dead time t_d and are already at the other supply rail when M_{HS}/M_{LS} turns on. This means I_{rip} (and consequently P_{Irip}) could be smaller by increasing f_{sw}. In the right part of Fig. 17.1.2, I_L is too small to charge C_P during t_d, and the remaining V_{pwm} rising transition is provided by M_{HS}. V_{pwm} is not yet at V_{DDP} when M_{HS} turns on, indicating the existence of P_{sw} and that therefore f_{sw} should decrease. By adapting f_{sw} such that either one of the V_{pwm} switching transitions is at the boundary of being lossless while the other is fully lossless, minimization of both P_{sw} and P_{Irip} is achieved. By setting an f_{sw} lower limit, the system naturally shifts to hard switching at high output power, with minimized P_{sw}.

The implementation of the amplifier is shown in Fig. 17.1.3. In this realization, the amplifier is based on a 1st-order hysteretic self-oscillating loop. Alternative implementations can also use carrier-based topologies [2] by changing f_{sw} of the triangle carrier, either continuously or through a frequency plan to control the spectral content. An f_{sw} regulation loop is added to the basic amplifier structure by tuning the hysteretic window voltage V_{tune}, which is generated by a charge pump/loop filter (CP/LF) that receives UP/DN 1-shots depending on the timing between the V_{pwm} level and the V_{HS}/V_{LS} rising edges.

The output stage works with a V_{DDP} of 80V, an on-chip regulated 3.3V driver supply and has a 2-step level shifter that can handle supply bounce higher than the internal supply [8]. Figure 17.1.4 (upper part) shows the V_{pwm} level detection circuit. At the beginning of a transition, when V_{pwm} is far (up to 80V) from the supply rail, M_{LSC}/M_{HSC} shield the clamps M_{LSD}/M_{HSD} from V_{pwm}. When V_{pwm} is close to the supply rail, M_{LSC}/M_{HSC} are in the linear region, such that M_1/M_4 can detect if V_{pwm} is less than a V_{TH} from the supply rail, which is close enough not to cause significant P_{sw}. Control signals $V_{LS\_detect}/V_{HS\_detect}$ are generated in the output stage with a time shift compared to V_{LS}/V_{HS} such that they only activate M_{LSC}/M_{HSC} for half the switching cycle to prevent cross current flow from the supply. M_4 level shifts to logic levels referred to V_{SSD}. M_1-M_3 level shift in 2 steps to deal with the large (>3.3V) on-chip PGND bounce. The lower part of Fig. 17.1.4 shows the UP/DN decision logic. The V_{pwm} status is sampled at the rising edge of V_{HS}/V_{LS}. The 1-shot for an f_{sw} increase is activated if both V_{pwm} transitions are finished in time while the 1-shot for an f_{sw} decrease is activated if either transition is not. Since V_{tune} is at 2× the signal frequency f_{sig} (when I_{out} increases in either direction), V_{tune} generation is fully differential for minimal 2nd-order distortion.

The amplifier is implemented in a 0.14μm SOI BCD process. For power efficiency measurements, a series-connected 23μF + 1.6Ω is used to model the piezo-actuator [1]. Because this load is mostly capacitive at f_{sig}, efficiency is defined here as $P_{out}/(P_{out}+P_d)$, where P_{out} is the apparent output power $V_{out,rms}$*$I_{out,rms}$ (VA) processed by the amplifier and P_d is the total amplifier dissipation. Figure 17.1.5 shows the measured efficiency of the amplifier for a 500Hz sine wave for three fixed V_{tune} settings and one with f_{sw}-regulation enabled. Figure 17.1.5 clearly shows that the amplifier can adjust its f_{sw} for best efficiency across the whole output power range. Idle power consumption is 360mW while for the two lower f_{sw} cases it is 440mW and 690mW, achieving a reduction of 18% and 48%. The peak efficiency of the amplifier is 93% while for the two higher f_{sw} cases it is 91% and 89%, achieving a power loss reduction of 19% and 31%. In idle, the adaptive f_{sw} is 500kHz while for 45VA output power, the adaptive f_{sw} is from 200kHz at D=0.5 to 100kHz at D=0.05 or 0.95.

A comparison with other high-voltage, high-power class-D designs is shown in Fig. 17.1.6. For better comparison, efficiency with a non-capacitive load (12Ω resistor) is also measured. The V_{pwm}-level-based f_{sw}-regulation technique enables this design to achieve peak efficiency better than those reported in Fig. 17.1.6, while significantly outperforming the other amplifiers at lower output powers. THD+N is 0.015% @ 100Hz, 9VA and 0.94% @ 500Hz, 45VA. For applications that require lower distortion, a higher-order feedback loop can be used. The chip photograph is shown in Fig. 17.1.7, with the die measuring 3.4×2.5mm². To conclude, this amplifier offers the high peak efficiency of existing class-D designs, keeping heat sinks small, while offering significant energy savings at lower, much more prevalent, output powers.

Acknowledgements:
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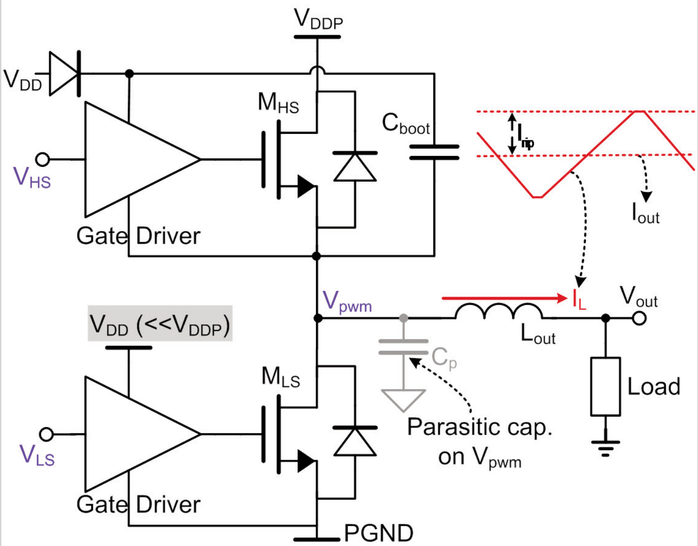

Figure 17.1.1: Basic class-D power output stage topology.

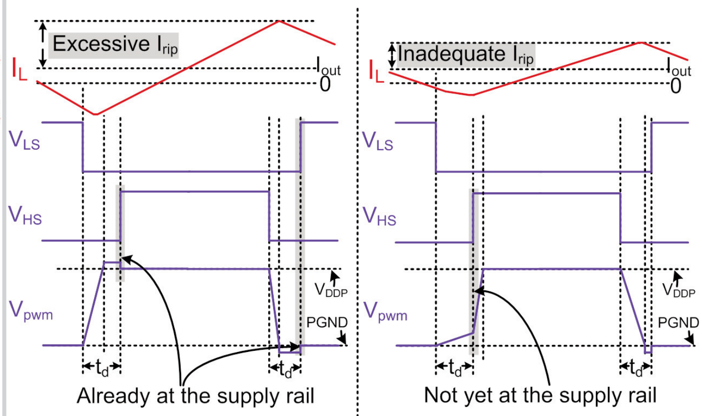

Figure 17.1.2: V_{pwm} level for excessive I_{rip} (left) and inadequate I_{rip} (right). V_{pwm} and t_d are not to scale.

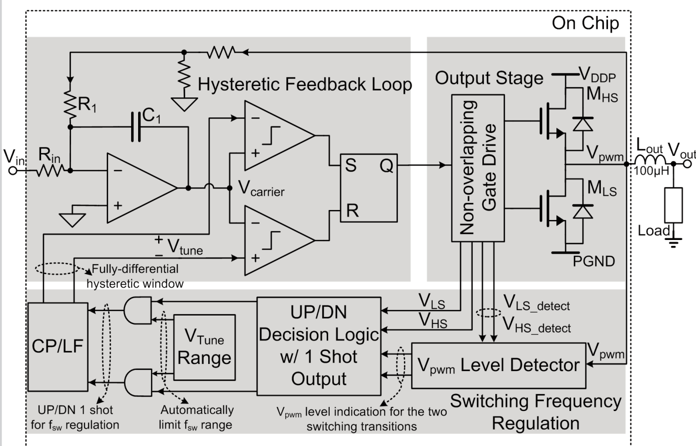

Figure 17.1.3: Implementation of the class-D power amplifier with f_{sw} regulation.

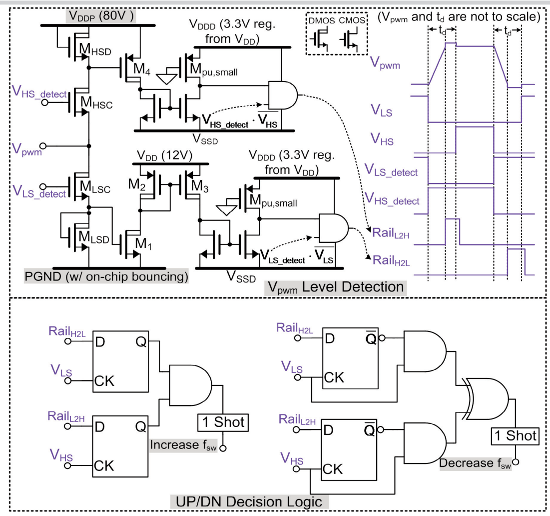

Figure 17.1.4: Schematic of the V_{pwm} level detector, control signal V_{HS_detect} is referred to V_{pwm} with level shifting (Upper); schematic of the UP/DN decision logic with 1-shot output (Lower).

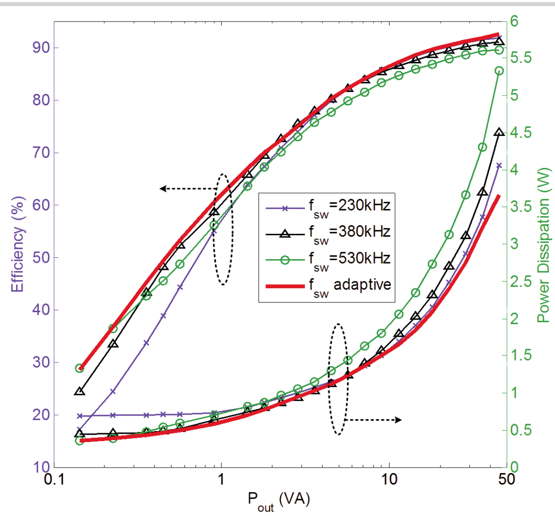

Figure 17.1.5: Efficiency and dissipation measurements for f_{sw} regulation enabled and for fixed V_{tune} settings. For the fixed V_{tune} cases, f_{sw} is measured in idle.

Parameters	This work		[2]	[3]	[4]	[5]
Type	Piezo Driver		Audio Amp.	Audio Amp.	Audio Amp.	Audio Amp.
V_{DDP}	80V		60V	20V	50V	18V
$P_{out,max}$/Channel	45VA(1)	45W(2)	100W	20W	240W	13W
Efficiency @ $P_{out,max}$	93%	91%	>90%	89%	N/A	88%
Efficiency @ 0.1* $P_{out,max}$	80%	84%	N/A	<75%	N/A	<70%
Efficiency @ 0.01* $P_{out,max}$	49%	51%	N/A	<30%	N/A	<30%
Idle Loss/Channel (w. output filter)	0.36W		1.6W	0.5W	2.1W	N/A
THD+N	0.015% (@9VA, f_{sig}=100Hz) 0.94% (@45VA, f_{sig}=500Hz)		0.017% (@1W, f_{sig}=1kHz)	0.01% (@10W, f_{sig}=1kHz)	<0.1%	0.7% (@13W, f_{sig}=1kHz)

(1) Load = 23μF+1.6Ω in series
(2) Load = 12Ω

Figure 17.1.6: Comparison with other high-voltage, high-power class-D power amplifiers.

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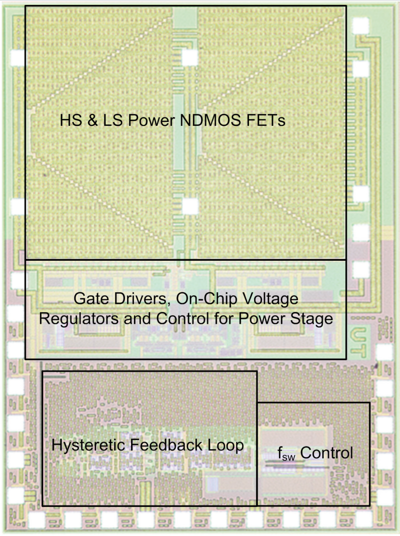

Figure 17.1.7: Chip photograph of the class-D amplifier, the die measures 3.4mm×2.5mm.

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