# 15.3 A 115dB-DR Audio DAC with –61dBFS Out-of-Band Noise

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Out-of-band noise (OBN) is troublesome in analog circuits that process the output of a noise-shaping audio DAC. It causes slewing in amplifiers and aliasing in sampling circuits like ADCs and class-D amplifiers. Nonlinearity in these circuits also causes cross-modulation of the OBN into the audio band. These mechanisms lead to a higher noise level and more distortion in the audio band. OBN also leads to interference in the LF and MF band, compromising e.g. AM radio reception. To avoid these problems, it is desired to reduce OBN power to below -60dBFS. An active low-pass filter after the DAC output can reduce the OBN power to acceptable levels, but this solution is expensive in terms of power consumption and chip area. A FIR-DAC [1] approach implements a 1b PWM modulator, followed by a semi-digital low-pass FIR reconstruction filter. It achieves high-end audio performance with sufficiently low OBN, but the FIR structure costs area, adds latency, and (like an analog low-pass filter) inherently limits the maximum output signal frequency. Multi-bit noise shapers employ smaller quantization steps and therefore output lower OBN. A cascaded-modulator architecture [2,3] can directly be followed by an on-chip amplifier without low-pass filtering. However, with only 330 quantization levels, it still cannot achieve the desired -60dBFS OBN without additional filtering. Moreover, this approach requires complex dynamic-element matching (DEM) and inter-symbol interference (ISI) shaping mechanisms.

We present an approach that reduces OBN to below -60dBFS with minimal increase in power and area consumption. It consists of two paths (Fig. 15.3.1). The main path is based on [4], containing a 128× oversampled 5b 3rd-order noise shaper, thermometer decoder and real-time DEM algorithm followed by a current DAC. Since the digital noise shaper generates negligible in-band noise products, the error signal of the noise shaper is practically equal to the OBN. This error signal is integrated (as part of the loop filter), quantized and fed to a correction path with a differentiating DAC (DIFF-DAC). This DAC inverts the integration action, obtaining unity signal transfer. The output currents of both paths are subtracted, reducing OBN significantly. Quantization noise of the correction path is shaped because the error signal is differentiated after quantization. Depending on the shape of the noise transfer function of the main DAC, the DIFF-DAC needs an over-range in order to accommodate the increased signal swing caused by the integration action. Still, area and power cost is minimal because the range of the DIFF-DAC is still only a fraction of the main DAC range.

The DIFF-DAC is a semi-digital FIR-DAC with a $1\text{-}z^{-1}$ transfer function (Fig. 15.3.2). A major issue with differentiating DACs is that the mismatch between the two DAC elements limits the low-frequency attenuation, which causes severe in-band quantization noise from the correction path quantizer if left unattended. We solve this problem with a simple binary dynamic-element-matching algorithm, where a data-swapper sends even samples to one DAC element and uneven samples to the other. Each DAC element therefore sequentially processes complementary pairs of samples, shaping the mismatch-induced noise with a differentiating transfer function [5].

A chip was designed and manufactured in a 0.18µm CMOS process. The interpolation filters and the noise shaper are implemented in an FPGA for flexibility. The digital part of the chip contains the 5b thermometer decoder, the Real-Time DEM algorithm and the logic circuitry for the DIFF-DAC. To obtain lower than -60dBFS OBN and accommodate some headroom for non-idealities, 2048 quantization levels (11b) are implemented in total. With a 5b main DAC and a factor 2 over-range, the DIFF-DAC needs 7b. An off-chip TIA provides a virtual ground at half the supply voltage.

Figure 15.3.3 illustrates the DAC elements, which consist of degenerated complementary current sources for low 1/f noise. The currents are switched to the differential output nodes by four minimum-sized NMOS transistors. Each set of switches is controlled by a local retiming latch. The switch driver employs a relatively wide PMOS and narrow NMOS to obtain a high crossing point for the switch signals. The main DAC contains 32 unit elements, which are designed for a $3\sigma$ inter-element mismatch of 1%. 64 unit transistors are placed in parallel to enable proper scaling of the two binary-weighted DIFF-DAC elements. The MSB of the DIFF-DAC is equally sized to the unit elements, providing the factor 2 over-range. The smaller bits are scaled by halving the transistor multipliers. Binary up-scaling the degeneration resistors of the LSB sources would dramatically increase chip area, so instead the 6 LSBs share one degeneration resistor. This increases 1/f noise by only a small amount, because 1/f noise is dominated by the unit sources. A dummy source with the weight of one LSB is added to get the same amount of nominal current in all degeneration resistors. Since the LSB current sources are 64 times smaller than the MSB sources, the $3\sigma$ mismatch between two LSBs is expected to be $\sqrt{64} * 1\% = 8\%$. Mismatch in the binary weights of the DIFF-DAC does not lead to distortion because the correlation between the audio signal and the error signal is very low due to the 3rd-order multi-bit noise shaping. It does cause a slightly raised quantization noise floor, but this noise is shaped and is accounted for in the design.

OBN was measured using an active differential probe and a spectrum analyzer. The total OBN power was found by integrating from 20kHz to 3.125MHz (half the sampling frequency). The 1kHz input signal is at -60dBFS to prevent overloading of the active probe. Figure 15.3.4 gives the OBN spectrum of the main DAC, and of the combined output with and without data swapping. The DIFF-DAC significantly reduces the OBN power by 29dB to -61dBFS. The data swapper removes mismatch-induced noise from the low-frequency end of the spectrum.

The in-band output spectrum is given in Fig. 15.3.5, for -6dBFS and -60dBFS signals at 1kHz. Dynamic Range and THD+N are measured at 115dB (A-Wtd) and -103dB, respectively. Figure 15.3.6 summarizes the performance and compares with other current-output audio DACs with low OBN and ≥100dB THD+N. The chip consumes 0.39mA from the 1.8V analog power supply, including the reference current for the bias circuit. The analog chip area is $0.08\text{mm}^2$, of which only 12% is occupied by the DIFF-DAC. The differentiating and data-swapping action of the DIFF-DAC effectively shapes the quantization noise of the correction path and the mismatch-induced noise. This allowed for a very area- and power efficient implementation. OBN is more than 10dB lower than [2], while the trade-off between area, power and noise remains unaffected. Therefore subsequent analog circuits can be driven directly without the power and area penalties of analog filtering.

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*References:*
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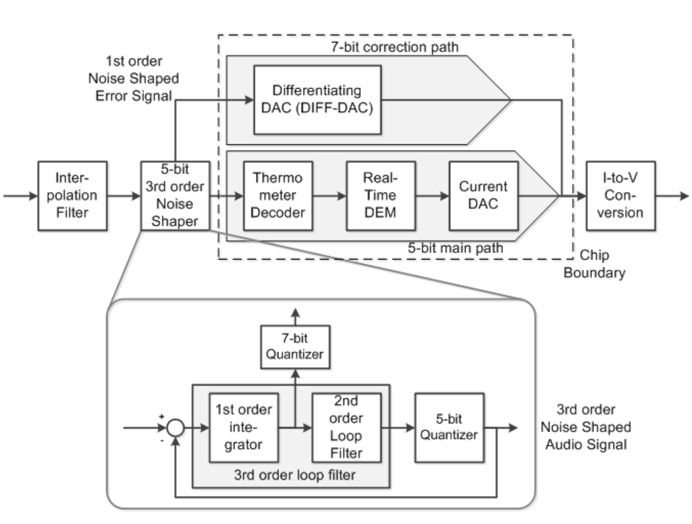


Figure 15.3.1: Audio DAC with main path and correction path for OBN reduction.

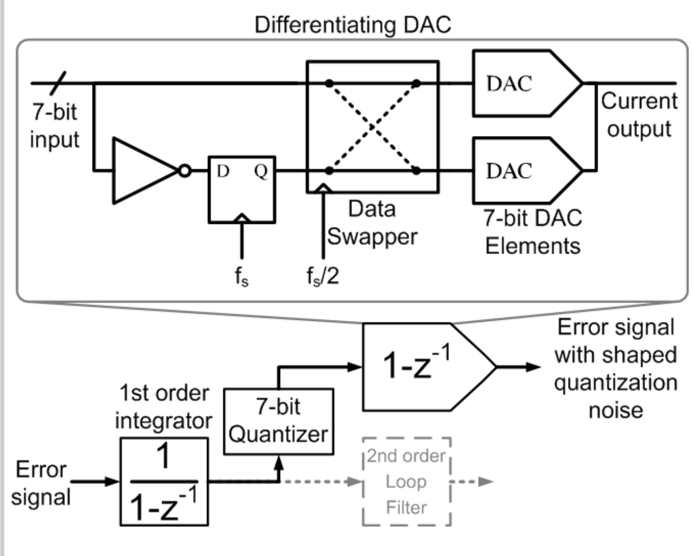


Figure 15.3.2: Correction path with DIFF-DAC.

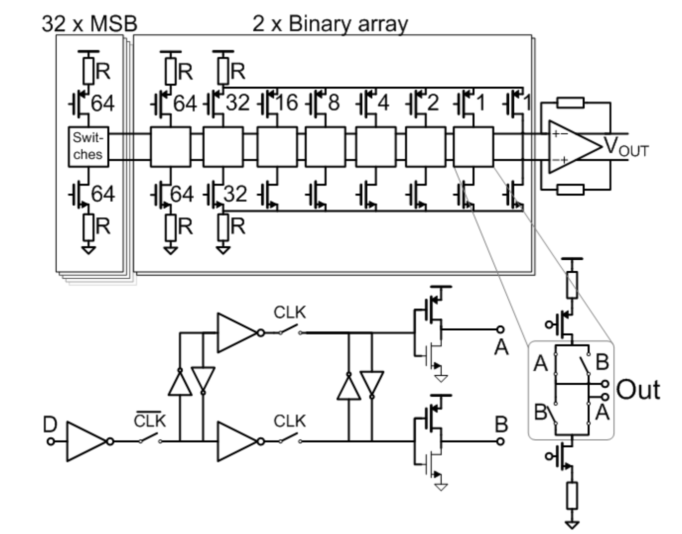


Figure 15.3.3: Implementation of the latches, switch drivers and switched current sources.

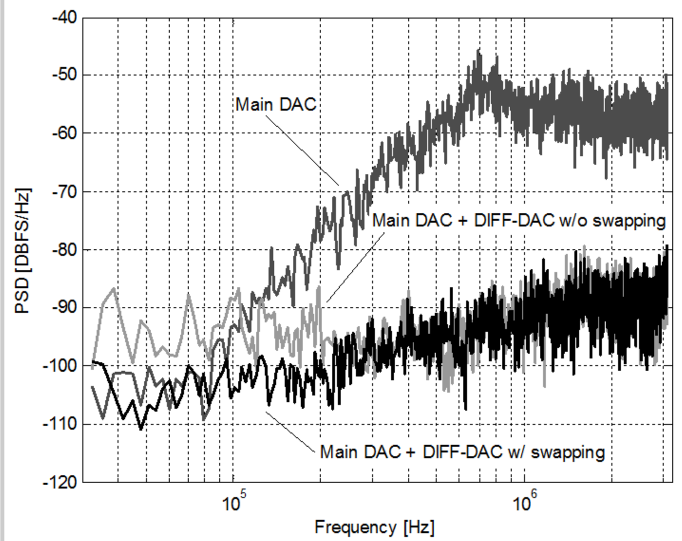


Figure 15.3.4: Measured Out-of-Band Noise PSD from 20kHz to 3.125MHz.

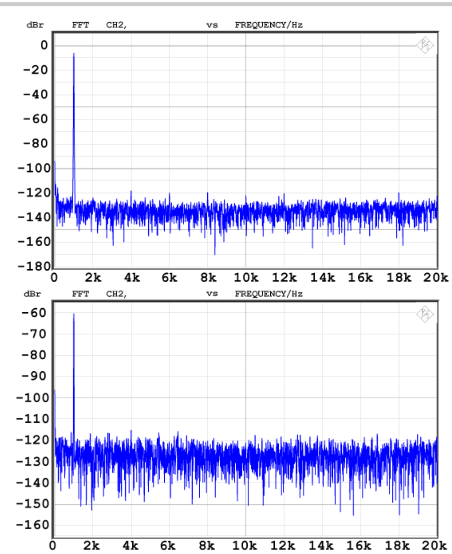


Figure 15.3.5: In-band spectrum with -6dBFS and -60dBFS input signals.

| Single Channel Performance | [1] | [2] | This work |
|---|---|---|---|
| Process | BCD | 45nm CMOS | 180nm CMOS |
| Analog supply (V) | 7 | 1.1 | 1.8 |
| Full-scale output ($mA_{pp}$) | 0.5 | 0.176 | 0.54 |
| Analog power consumption(mW) | 5 | 0.4 | 0.7 |
| Analog area ($mm^2$) | > 0.36 | < 0.04 | 0.08 |
| Dynamic Range (dB A-wtd) | 111 | 110 | 115 |
| THD+N (dB) | -103 | -100 | -103 |
| OBN (dBFS) | -66 | ~ -50(1) | -61 |
| Output resolution (levels) | - | 330 | 2048 |

1: estimated

Figure 15.3.6: Comparison table.

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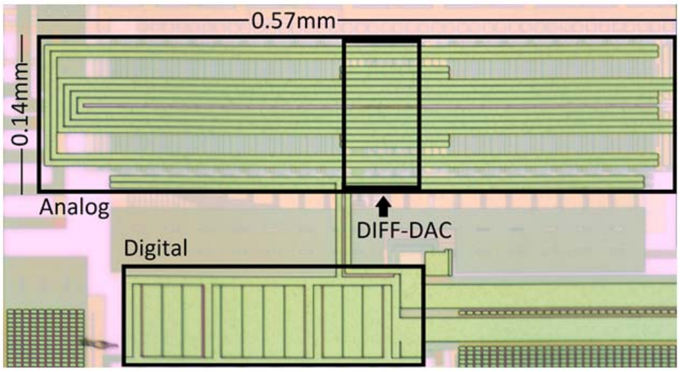


Figure 15.3.7: Die micrograph.