Session 3 Overview: *Ultra-High-Speed Wireline Transceivers and Energy-Efficient Links*

WIRELINE SUBCOMMITTEE

Session Chair: *Hyeon-Min Bae, KAIST, Daejeon, Korea*

Session Co-Chair: *Ajith Amerasekera, Texas Instruments, Dallas, TX*

Smart phones and their social apps are key drivers for the growth of the internet and, more generally, of big data infrastructure. The ever-increasing demands placed on this infrastructure, in turn, spurs the insatiable need for data communication bandwidth between chips. In this context, wireline transceivers that push the limits imposed by process technology – in terms of data rate, energy efficiency, and area – are extremely critical. This session introduces 2 ADC-based receivers operating at or beyond 25Gb/s for multi-standard support. It continues with a presentation of a 25Gb/s equalizer for cable-dominated channels with up to 50dB of half-baud loss. Two papers addressing different approaches for high-data-rate, short-reach communication are presented next, including an NRZ/PAM-4 Ethernet ADC-based transceiver and a 56Gb/s per lane NRZ transceiver. Finally, the session concludes with two papers describing critical components for I/O solutions at per-lane rates at or beyond 45Gb/s, including a power-efficient 45Gb/s PAM-4 transmitter and a 64Gb/s NRZ transmitter for CDE-56-VSR/MR applications, the latter implemented in 16nm finFET.

1:30 PM

3.1 A 25Gb/s ADC-Based Serial Line Receiver in 32nm CMOS SOI

S. Rylov, IBM T. J. Watson Reseach Center, Yorktown Heights, NY

In Paper 3.1, IBM presents a 25Gb/s ADC-based serial line receiver in 32nm CMOS SOI. The receiver uses a ¼ rate 5b flash ADC with on-chip calibration followed by an interleaved 8-tap FFE and 8-tap DFE backend and digital CDR. The transceiver occupies 0.39mm^2 and compensates a reflective 40dB loss channel while consuming 453mW.

2:00 PM

3.2 A 320mW 32Gb/s 8b ADC-Based PAM-4 Analog Front-End with Programmable Gain Control and Analog Peaking in 28nm CMOS

D. Cui, Broadcom, Irvine, CA

In Paper 3.2, Broadcom presents a 32Gb/s 8b ADC-based PAM-4 receiver in 28nm CMOS. The ADC achieves an ENOB of 6.4 and 5.85 at DC and Nyquist, respectively. The entire receiver, occupying 0.89mm^2, features a continuous-time linear equalizer with a 7dB peaking gain, and compensates for channel loss of more than 50dB at 16GHz while consuming 320mW.

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2:30 PM

3.3 A 25Gb/s Multistandard Serial Link Transceiver for 50dB-Loss Copper Cable in 28nm CMOS

T. Norimatsu, Hitachi, Tokyo, Japan

In Paper 3.3, Hitachi presents a 25Gb/s multi-standard serial link transceiver in 28nm CMOS. The receiver, using a 20dB CTLE and a 14-tap DFE, achieves 3mV input sensitivity by using sub-mV dynamic DC-offset cancellation and DFE tap-bias control schemes. The transceiver, occupying 5.5x4.6mm^2, achieves BER < 10^{-12} over a 51dB-loss 5m AWG channel at 25Gb/s and consumes 403mW from 0.9 and 1.5V power supplies.

3:15 PM

3.4 A 40/50/100Gb/s PAM-4 Ethernet Transceiver in 28nm CMOS

K. Gopalakrishnan, Inphi, Santa Clara, CA

In Paper 3.4, Inphi describes a 40/50/100Gb/s NRZ/PAM-4 Ethernet transceiver in 28nm CMOS. The receiver integrates two SAR ADCs with ENOB of 4.8, a DSP for calibration, and an FEC encoder. The transmitter includes a FEC decoder and supports both NRZ and PAM-4 signaling with a maximum swing of 1.4Vpp. The transceiver, which includes an internal supply voltage regulator, occupies 6.3x4.9mm^2 and achieves less than 200fs output jitter while consuming 2.4W from 0.9V and 1.2V power supplies.

3:45 PM

3.5 A 56Gb/s NRZ Electrical 247mW/lane Serial Link Transceiver in 28nm CMOS

T. Shibasaki, Fujitsu Laboratories, Kawasaki, Japan

In Paper 3.5, Fujitsu presents a 56Gb/s/lane electrical NRZ transceiver in 28nm CMOS for high-data-rate applications, using baud-rate sampling to minimize the power consumption. The design features a 2-tap feed-forward equalizer and a continuous-time linear equalizer, followed by a 1-tap speculative decision-feedback equalizer. The receiver compensates for 18.4dB half-baud loss. The transceiver occupies 1.4mm^2 per two lanes and consumes 247mW/lane from a 0.96V supply.

4:15 PM

3.6 A 45Gb/s PAM-4 Transmitter Delivering 1.3V_{ppd} Output Swing with 1V Supply in 28nm CMOS FDSOI

M. Bassi, University of Pavia, Pavia, Italy

In Paper 3.6, researchers from the University of Pavia present a 45Gb/s PAM-4 transmitter able to deliver 1.3Vppd output swing; the design is implemented in 28nm fully-depleted SOI CMOS and is intended to address next generation CEI-56G standards for high speed links. The design occupies an area of 0.28mm^2 and consumes 120mA from a 1V supply.

4:45 PM

3.7 A 40-to-64Gb/s NRZ Transmitter with Supply-Regulated Front-End in 16nm FinFET

Y. Frans, Xilinx, San Jose, CA

In Paper 3.7, Xilinx presents a 3-tap 64Gb/s NRZ transmitter using a quad-rate architecture for short reach electrical links implemented in a 16nm FinFET technology. The design, which is applicable to next generation standards such as CEI-56-VSR/MR, uses power efficient techniques that take into consideration the 16nm FinFET device properties. The transmitter achieves 800mVppd output swing with 150fs random jitter while consuming 225mW at 64Gb/s and occupying an area of 0.32mm^2.