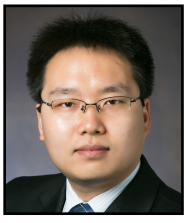
Session 23 Overview:
Electrical and Optical Link Innovations
WIRELINE SUBCOMMITTEE

Session Chair: *Frank O'Mahony, Intel, Hillsboro, OR*

Session Co-Chair: *Simone Erba, STMicroelectronics, Pavia, Italy*

Continued data bandwidth scaling is essential in all segments of electronics, from low-power mobile to high-speed data centers. Each of these segments is faced with different constraints to bandwidth scaling, including power, process technology, and form factor. This session highlights how design and technology are keeping pace with bandwidth demands with innovations in both electrical and optical data links. It starts with a transceiver that combines an integrated regulator and rapid wake-up to scale data rate by 500× while keeping energy-per-bit within a factor of 2×. The next paper describes a proximity communication link with 32Gb/s total bandwidth over four parallel capacitively coupled channels across a 1mm air gap. This is followed by a paper that implements a 5-tap DFE in a 4 x 6Gb/s display interface while overcoming the f_t limits of 0.18µm CMOS. Two papers then introduce a 56Gb/s MZM-based TX and 2x64Gb/s optical TIA, respectively, demonstrating the next-generation path for optical bandwidth scaling. The session concludes with two high-speed wireline receivers that demonstrate <1pJ/bit energy efficiency at 30-40Gb/s and one that demonstrates fast DFE-IIR equalization adaptation.



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23.1 A 16Mb/s-to-8Gb/s 14.1-to-5.9pJ/b Source Synchronous Transceiver Using DVFS and Rapid On/Off in 65nm CMOS

G. Shu, University of Illinois, Urbana-Champaign, IL

In Paper 23.1, the University of Illinois at Urbana-Champaign presents a source-synchronous transceiver that combines dynamic voltage and frequency scaling with rapid on-off techniques to maintain energy efficiency of 5.9-14.1pJ/b across a 500× effective data-rate range. A DC-to-DC converter with 94% efficiency supports fast changes in voltage and load current. Link wake-up time is only 14ns; the design includes a wide-range MDLL that settles in only two reference clock cycles.

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23.2 A 32Gb/s Bidirectional 4-Channel 4pJ/b Capacitively Coupled Link in 14nm CMOS for Proximity Communication

C. Thakkar, Intel, Hillsboro, OR

In Paper 23.2, Intel describes a 4-channel bi-directional proximity interface with 32Gb/s total bandwidth that consumes 4pJ/b in 14nm CMOS. The capacitive couplers use an alternating, rectangular pattern to suppress crosstalk without keep-out areas between channels. Transmitter slew-rate control, an integrating receiver and a 1-tap DFE equalize the resonant channel with low power overhead.

2:30 PM

23.3 A 6Gb/s 3-Tap FFE Transmitter and 5-Tap DFE Receiver in 65nm/0.18µm CMOS for Next-Generation 8K Displays

M. Hekmat, Samsung Semiconductor, San Jose, CA

In Paper 23.3, Samsung Semiconductor presents a 4x6Gb/s display interface for next-generation 8K TVs. The receiver implements a 5-tap partial-response DFE in 0.18µm CMOS. To overcome the f_t limits of this process, it uses body bias to set the weight of the loop-unrolled tap and reduces the number of sequential logic elements in the feedback path.

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23.4 A 56Gb/s 300mW Silicon-Photonics Transmitter in 3D-Integrated PIC25G and 55nm BiCMOS Technologies

G. Minoia, STMicroelectronics, Pavia, Italy

In Paper 23.4, STMicroelectronics and the University of Pavia describe a complete 56Gb/s electro-optical transmitter, operating at a 1310nm wavelength, dissipating 300mW and achieving a >2.5dB extinction ratio. The combination of a traveling-wave Mach-Zender Modulator in a silicon photonic technology and an electronic driver in 55nm BiCMOS realizes the proposed transmitter. Integrated transmission line bandwidth limitations are compensated by applying passive boost, shunt peaking in the pre-driver stage, and passive peaking in the load.

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23.5 A Dual 64Gbaud 10kΩ 5% THD Linear Differential Transimpedance Amplifier with Automatic Gain Control in 0.13µm BiCMOS Technology for Optical Fiber Coherent Receivers

A. Awny, IHP, Frankfurt(Oder), Germany

In Paper 23.5, IHP describes a 64Gbaud linear transimpedance amplifier for long-haul coherent receivers. Implemented in 130nm BiCMOS, it achieves a 3dB bandwidth of 53GHz while consuming 277mW. The dual TIA chip provides an aggregate data rate of 128Gb/s using QPSK modulation.

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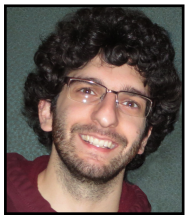
23.6 A 30Gb/s 0.8pJ/b 14nm FinFET Receiver Data-Path

P. A. Francese, IBM Zurich Research Laboratory, Rüshlikon, Switzerland

In Paper 23.6, IBM Zurich Research Laboratory presents a 14nm SOI CMOS 30Gb/s receiver data path. It achieves 0.8pJ/b energy-efficiency at maximum data rate. The CTLE exhibits 9.5dB gain boost tunable at Nyquist frequency without passive inductors. In the 1-tap DFE a single regenerative stage per slice discriminates after selection of analog speculated paths.



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23.7 A 16Gb/s 1 IIR + 1 DT DFE Compensating 28dB Loss with Edge-Based Adaptation Converging in 5µs

S. Shahramian, University of Toronto, Toronto, Canada

In Paper 23.7, University of Toronto presents a 16Gb/s 28nm FD-SOI CMOS receiver. Based on 1 IIR + 1 discrete DFE tap and including integrated clock recovery and adaptation, it equalizes a 28dB-loss channel. An edge-based algorithm adapts both IIR and DT equalizer coefficients using the same high-speed circuitry required for clock recovery.

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23.8 A 40Gb/s 14mW CMOS Wireline Receiver

A. Manian, University of California, Los Angeles, CA

In Paper 23.8, the University of California, Los Angeles, presents a 40Gb/s NRZ receiver in 45nm CMOS. It consists of a one-stage CTLE, a half-rate CDR circuit, a half-rate/quarter-rate DFE, a discrete-time linear equalizer, and a deserializer. The receiver, which dissipates only 14mW, achieves a BER < 10^-12 with a recovered clock jitter of 1.3ps-rms and a jitter tolerance of 0.45UI at 5MHz when operating over a channel with loss of 18.6dB at Nyquist.