# SINGLE-CHIP REDUCED-WIRE ACTIVE CATHETER SYSTEM WITH PROGRAMMABLE TRANSMIT BEAMFORMING AND RECEIVE TIME-DIVISION MULTIPLEXING FOR INTRACARDIAC ECHOCARDIOGRAPHY

A Dissertation
Presented to
The Academic Faculty

by

Gwangrok Jung

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2019

# SINGLE-CHIP REDUCED-WIRE ACTIVE CATHETER SYSTEM WITH PROGRAMMABLE TRANSMIT BEAMFORMING AND RECEIVE TIME-DIVISION MULTIPLEXING FOR INTRACARDIAC ECHOCARDIOGRAPHY

Approved by:


Dr. F. Levent Degertekin
School of Electrical and Computer Engineering
*Georgia Institute of Technology*

Dr. Farrokh Ayazi
School of Electrical and Computer Engineering
*Georgia Institute of Technology*

Dr. Stanislav Emelianov
School of Electrical and Computer Engineering
*Georgia Institute of Technology*

Dr. Coskun Tekes
Department of Computer Engineering
*Kennesaw State University*

Dr. Omer Inan
School of Electrical and Computer Engineering
*Georgia Institute of Technology*



Date Approved: August, 15, 2019

# ACKNOWLEDGEMENTS

I would like to express my gratitude to my advisor, Dr. F. Levent Degertekin for sincere support of scholastic guidance. During 5 years of PhD research, I was able to seek for creative and logical solutions since his door opened always and he was willing to discuss. It is pleasant and precious memory.

I would like thank Dr. Coskun Tekes for his invaluable time and help. He was always with me during acoustic measurements, supporting and teaching me with deep knowledge. I am grateful to Dr. Stanislav Emelianov, Dr. Farrokh Ayazi, and Dr. Omer Inan for their time and advice in reviewing my PhD dissertation and serving as committee members.

My research work is a system level combination of multiple projects, requiring various background and knowledge. I am thankful to Dr. Maysam Ghovanloo for his guidance and support, and previous GT-bionics members. I would like to acknowledge the support during my PhD from Muhammad, Thomas, Ahmad, Evren, Amir, Sush, and Yusuf.

I am grateful to my family, my mother, father and Gwangha. I could not finish my PhD without their help. They support me every time even they are not with me.

Last, but the most important, I would like to express my sincere gratitude to my dear wife Unji. She sacrifices and supports me with her love. I feel myself lucky for having her in my life. This work would not be finished without her support.

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# SUMMARY

The main objective of proposed thesis research is to develop a single chip reduced-wire active catheter system, which adopts programmable transmit beamforming and receive time-division multiplexing (TDM). The proposed front-end application-specific integrated circuit (ASIC) is designed for driving a 64-channel 1-D piezo-transducer array or capacitive micromachined ultrasound transducer (CMUT) array in intracardiac echocardiography (ICE) catheters.

ICE has become more important clinical modality in interventional ultrasound imaging. It requires a minimal invasive procedure during which a small catheter is placed into a femoral vein to image the heart anatomy from inside. It provides real-time ultrasound imaging, guiding interventions like valve repair, placement of stents, closure of atrial septal defects (ASD) and catheter-based ablation to treat atrial fibrillation. ICE needs local anesthesia and the sedation and it is becoming the preferred imaging tool with better image quality over transesophageal echography (TEE) which requires general anesthesia delivered by an anesthesiologist.

Current ICE catheters offer a limited 2-D or 3-D field of view in spite of large number electrical interconnections to the main imaging system, which are mainly determined by the number of array elements and ground connections. Each element in the ICE array is connected to corresponding analog-front-end (AFE) system with a separate long wire, which is a significant limitation for improving image quality and increasing the number of elements. Also, in order to use ICE catheters under MRI instead of the ionizing X-ray radiation-based angiography, the number of interconnect wires in the catheter should

be minimized to reduce RF-induced heating from metal connection. Furthermore, reducing the number of wires would improve the flexibility, reach, and even lower the cost of the single-use ICE catheters. Therefore, an interconnection reduction method which integrates electronics in the catheter tip would have a significant impact in the catheter-based ultrasound imaging applications.

# CHAPTER 1. INTRODUCTION

## 1.1 Medical Ultrasound Imaging for ICE

Medical ultrasound imaging has had a significant impact on clinical practice by providing real time images of different organs with high spatiotemporal resolution non-invasively at low cost [1]. The discovery of piezoelectric effect by Pierre and Jacques Curie in 1880 [2], which enabled generation and perceiving of acoustic waves, was a critical moment in developing ultrasound technology. Furthermore, invention of the submarine detection by Paul Langevin during World War I ignited research on ultrasonics [3], [4]. In 1918, Langevin filed a patent [5] which led to the discovery of SONAR (Sound Navigation and Ranging) system to detect submarines. In 1940s, Neurologist Karl Dussik published theoretical analysis of how ultrasound can be used to image the human body [6]. He was the first to use ultrasound to diagnose a brain tumor. The first real time ultrasound B-scanner, named Vidoson, was developed by Siemens Medical Systems of Germany in 1965. In the last sixty years, medical ultrasound continued to grow and mature becoming one of the popular medical imaging modalities.

In a typical ultrasound imaging system, a one-dimensional (1-D) piezoelectric array probe is used. Piezoelectric materials are simply diced and bonded to a backing layer in the transducer probe. The system further consists of an interface, display, back-end and beamformer unit. Operator can provide instructions to the machine using the user interface. All the receiver electronics, including low noise amplifier (LNA), time gain compensation (TGC) circuits, analog to digital converters (ADCs), receiver beamformer, high voltage

transmitter and transmit beamformers are placed in the beamformer unit. Electrical connection to the array is provided through long cables from the beamformer unit. Data from the scanner unit is processed by the back-end unit for display. Different ultrasound transducer probes are required to diagnose dedicated applications such as ob/gyn, abdomen, and cardiac.

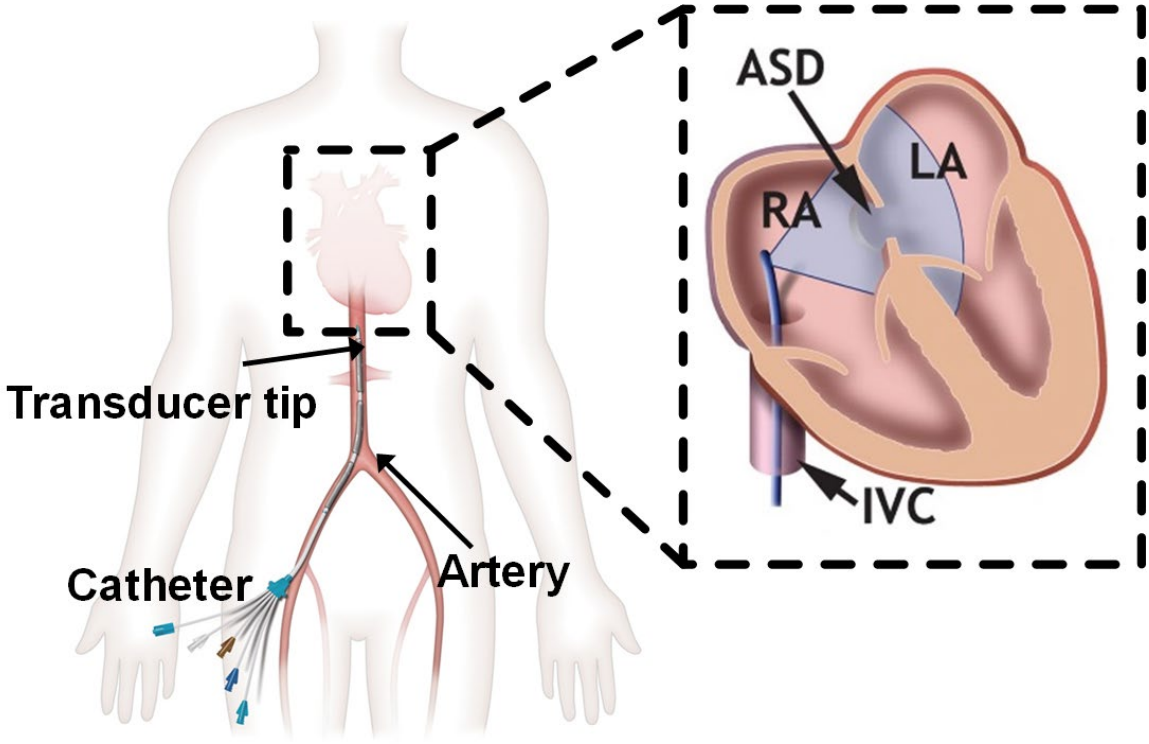



**Figure 1.** ICE probe insertion diagram

Heart disease is the leading cause of death in the World. About 610,000 people die of heart disease in the United States every year [7]. In addition to that, more than five million Americans are diagnosed with heart disease each year. Heart valve disease can occur in any single valve or a combination of the four valves, but diseases of the aortic and mitral valves are the most common. While up to 1.5 million people in the United States

suffer from aortic stenosis, approximately 500,000 within this group of patients suffer from severe aortic stenosis. An estimated 250,000 patients with severe aortic stenosis are symptomatic [8]. So any advances in diagnosis and treatment for heart disease would have an impact. Two leading ultrasound techniques used in interventional cardiac imaging are Intracardiac echocardiography (ICE) [9], [10] and transesophageal echocardiography (TEE) [11]-[14]. These two modalities guide electrophysiology (EP) to treat arrhythmias and for structural heart procedures to treat defects in heart valves, closure of atrial septal defects (ASD) which the Centers for Disease Control and Prevention (CDC) estimated that 13 of every 10,000 babies born had an ASD [15], and catheter-based ablation which single-procedure success rates for curing atrial fibrillation with radio frequency catheter ablation are as high as 80 % for atrial fibrillation [16]. The ICE catheter has a small ultrasound imaging probe at the tip [17]-[19]. To place the ICE catheter inside the human heart, physicians make a small incision near the upper part of the leg to insert the probe inside the femoral vein as shown in Figure 1. The catheter tip is then navigated through the femoral artery to the Inferior Vena Cava (IVC) and positioned into the right atrium of the heart. With its better image quality and ease of use, ICE is becoming the preferred imaging modality over TEE for structural heart interventions. The main advantages of ICE over TEE are it can be performed without the need of general anesthesia and procedure time can be shorter. ICE uses 8 F to 10 F (~ 3mm) catheters, the ultrasound transmitting frequency of the ICE is 5 MHz to 8 MHz, and has a penetration depth of 15 cm with lateral resolution of 1 to 2 mm, axial resolution of ~150 μm. The existing commercial ICE catheters, however, offer a limited 2- D or 3-D field of view despite utilizing large number of wires.

In these catheters, each element in the ICE array is connected to the backend data acquisition channel with a separate wire, which is a critical barrier for improving image quality and widening the field of view. In order to use ICE catheters under MRI instead of the ionizing X-ray radiation-based angiography, the number of interconnect wires in the catheter should be minimized to reduce RF-induced heating. Furthermore, reducing the number of wires improves the flexibility and lowers the cost of the single-use ICE catheters. This is the main motivation of this PhD thesis.

## 1.2 Basic Principles of Ultrasound Imaging

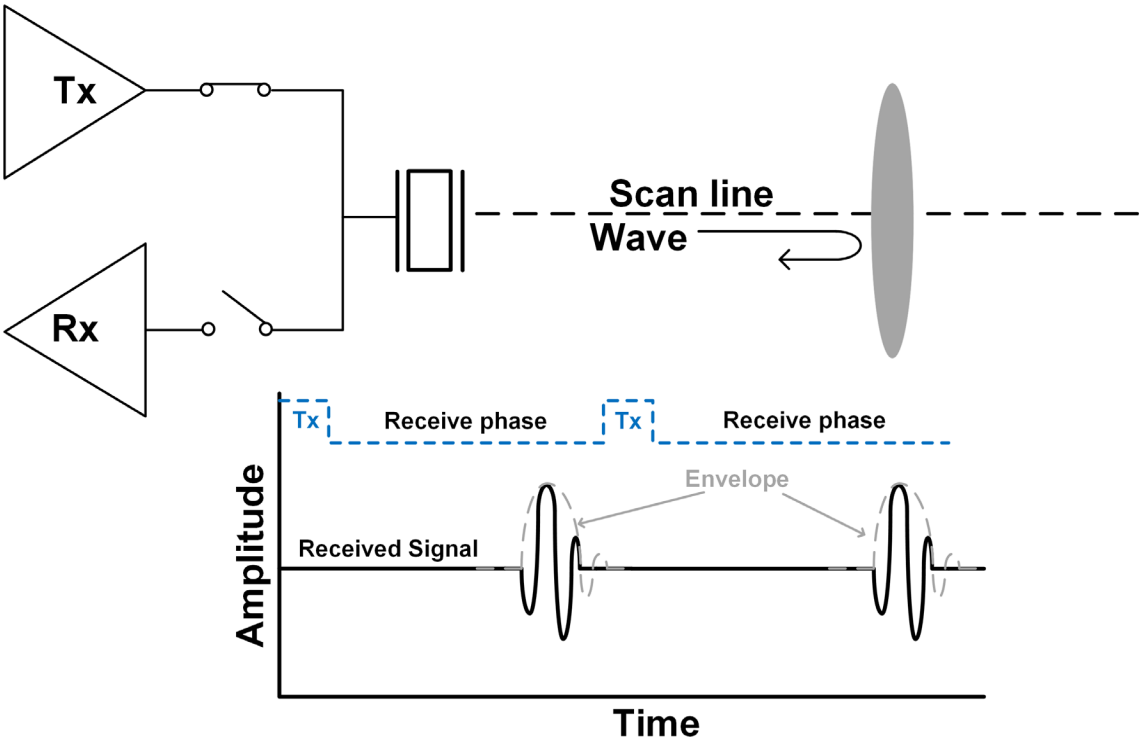



**Figure 2.** Illustration of pulse-echo operation for A-scan.

A typical ultrasound imaging system performs transmit and receive cycles for each of a single transducer element [20]. This combination of transmitting and receiving is referred as a pulse-echo operation. During the transmit mode, the transmitter circuitry excites the transducer with a high-amplitude and short-duration electrical pulse. The transducer converts the electrical pulses into acoustic pressure and generates ultrasound waves propagating at the speed of sound in the medium. After this transmit operation, the transducer element is switched to a receive mode and the receive cycle begins. The receive cycle shows the A (Amplitude)-scans generated by the transducer in response to the received echoes. The transmit/receive cycle is repeated until all the image lines are obtained to create the cross-sectional image as shown in Figure 2.

The medium consists of layers of materials with different acoustic impedances. The acoustic wave gets partially reflected back when it meets these layers with different acoustic impedances along the propagation path in the medium. The amount of the reflected acoustic wave is proportional to the difference of the acoustic impedances. In other words, if the difference in the acoustic impedances is large, most of the incident ultrasound wave gets reflected. Similarly, if the difference of the acoustic impedances is small, which typically is the case at boundaries of soft tissues, a small percentage of the acoustic wave gets reflected, and most of the acoustic power continues propagating in the medium. The reflected wave, which is referred as an echo, travels back towards the face of the transducer. When the echoes reach and hit to the transducer element, the transducer converts the received acoustic pressure into electrical signals. The distance of the reflector from the transducer can be found using the time difference between the initial transmitted

pulse and the received echo. Assuming a constant speed for the acoustic wave propagation in the medium, the distance from the transducer to the reflector is calculated by

$$\boldsymbol{D} = \frac{\boldsymbol{c} \times \boldsymbol{t}}{\mathbf{2}} \quad (1)$$

Where D is the distance, t is the time of arrival, and c is the speed of sound in the particular medium (~1540 m/s for soft tissue [20]).

The process to create images from the received pulse-echo responses is as follows. First, envelope (amplitude) detection is done on the received echo signals. Each transmit pulse and its echoes form an amplitude mode (A-mode) scan line in the particular direction. After each transmit/receive cycle, the scan line is rotated either mechanically or electrically and the transmit/receive cycle is repeated to acquire a new image line. This process is repeated until the complete scan of the two-dimensional cross-sectional image area is completed one scan line at a time. Thus, each cross-sectional image may contain information of hundreds of separate A-scans. To generate the greyscale cross-sectional ICE images from the acquired A-scans, the amplitudes of the received signals in each scan line are mapped to a brightness level where higher amplitude echoes are mapped as brighter in the image. Hence, these generated images are called brightness-mode (B-mode) images.

The duration of each transmit/receive cycle depends on the desired imaging depth because the system needs to wait until the echoes from the deepest tissue come back. For instance, to construct an image with a depth of 15 cm, each receive period must be at least 200 $\mu$s. The pulse-repetition frequency along with the total number of the required scan lines determines the image frame rate. This indicates a trade-off between the image frame

rate and the imaging depth. A volumetric imaging is another ultrasonic imaging mode. In 3D imaging, the received A-scans are rendered and presented on a volumetric image. Usually the same transducer is used both as a transmitter and a receiver. However, it is also possible to use separate transducers dedicated for receiving and transmitting operations. This enables independent optimization of the transducers for their respective operation mode and it also removes the need of switching circuitry between transmit and receive modes. On the other hand, the trade-off is that this also requires two transducers for each pulse-echo operation which requires more area.

The spatial resolution of an ultrasound system refers to the minimum separation between structures within the image that the ultrasound beam can distinguish. Spatial resolution is commonly categorized into axial resolution and lateral resolution. Axial resolution is the resolution in the direction along the axis parallel to the acoustic wave propagation, which is following

$$R_{AX} = \frac{N \times \lambda}{2} \tag{2}$$

where N is the number of cycles in the pulse and λ is the wavelength of the ultrasound signal corresponding to the frequency of the transmitted signal. Note that the transducer impulse response looks like a bandpass filter with a center frequency and a bandwidth. A higher bandwidth improves the axial resolution as it reduces the duration (N) of the transmitted ultrasound pulse and a higher bandwidth reduces the wavelength which also improves the axial resolution. It should be noted that the axial resolution does not depend

on the distance from the transducer (unlike the lateral resolution) and is the same at any point in the scan line.

The lateral resolution is the resolution in a plane perpendicular to the direction of the ultrasound beam. The lateral resolution varies with the width (diameter) of the beam, and hence depends on the distance from the transducer. Along the beam axis there is an optimum point that is referred as the focal zone where the ultrasound beam has the smallest beam diameter providing the best lateral resolution. Away from the focal point (in the far field), ultrasound beams typically diverge which decrease the lateral resolution. Similarly, at locations very close to the array, the beam is not focused which also results in a decreased lateral resolution. The axial length over which the beam remains relatively focused is referred as the depth of field. A typical measure of the depth of field is the distance over which the lateral resolution stays within the 3 dB of the resolution at the focal point. The lateral resolution at the focal point is given with the below expression

$$R_{LA} = \frac{\lambda \times F}{D} \tag{3}$$

where F is the distance of the focal point from the transducer and D is the transducer diameter (aperture size). The ratio of the focal distance to the spatial dimension of the transducer is referred as the f-number. From (3), it becomes apparent that the lateral resolution at the focal point is directly proportional to the f-number and the wavelength. It should also be noted that the lateral resolution is generally few times poorer than the axial resolution.

## 1.3 Receiver Array Cable Reduction Technique

### *1.3.1 μ-Beamformer*

To reduce the number of wires in ultrasound systems, recent research shows several approaches in receiver (Rx) side. Sub-array beamforming (μ-beamforming) with analog delay chains which adopts a switched-capacitor-based delay has been demonstrated [21]-[29]. This technique is performed by delaying the signals relative to each other in such a way that waves from a certain focal point, arrive simultaneously and can be coherently summed in a sub-array block. This approach requires a large number of capacitors and switches for each channel for achieving enough delays, induces mismatch between channels, and could not satisfy back-end system which make use of the advanced imaging technique requiring the raw echo data from all channels. The digital subarray beamforming with ΔΣ modulator has shown compact integration [30]. However, this system requires high frequency operation (960 MHz), which is difficult to feed into long interconnection in catheter-based application, limiting the integration of high voltage (HV) transmit circuits with thick oxide gate on a single chip.

### *1.3.2 Integrated ADCs*

One of the popular techniques which is adopted in 2-D array type systems is on-chip integrated ADC. The integration of ADCs will allow digital signal processing for reducing the number of interconnects between the transducer array and the signal processing unit. This technique is usually used in combination with μ-beamforming [23],

however, in a size and power constrained system, such as an ICE catheter, this would be simply be not feasible or very challenging to implement [31].

### *1.3.3 PWM and FDM*

To reduce the cable count for ultrasound catheter probes, pulse width modulation (PWM) technique was reported in [32]. PWM employs a train of pulses where the signal is sampled and each sample value is encoded in the width of a pulse. Once converted to duty cycle, the information becomes more immune to channel noise and attenuation. Furthermore, PWM requires less area and power than ADCs [33]. One major disadvantage of PWM technique is that it requires very high channel bandwidth to transfer data from PWM source to signal processor. Frequency division multiplexing (FDM) has been shown to be feasible for ICE application [34]. However, this approach requires multiple number of analog filters and mixers that are vulnerable to process variations, which will increase the mismatch and the complexity of the system.

### *1.3.4 TDM*

Time-division multiplexing (TDM) has been used in communications systems to reduce the number of channels. This method allows multiple channels to share the same wire by assigning each channel in a proper time slot while sampling at the receiver with the same channel number of ADCs as shown in Figure 3(a) [35], [36]. One of the advantages of Analog TDM is that it needs relatively small amount of circuitry and lower power consumption, since it requires multiplexer and digital counting logic to sample the data. This compact structure makes it suitable for catheter-based applications. Another

approach shows to reduce the number of ADC that de-multiplexer samples with high clock frequency which is at least the number of channel times of the Nyquist rate as shown in Figure 3 [37].

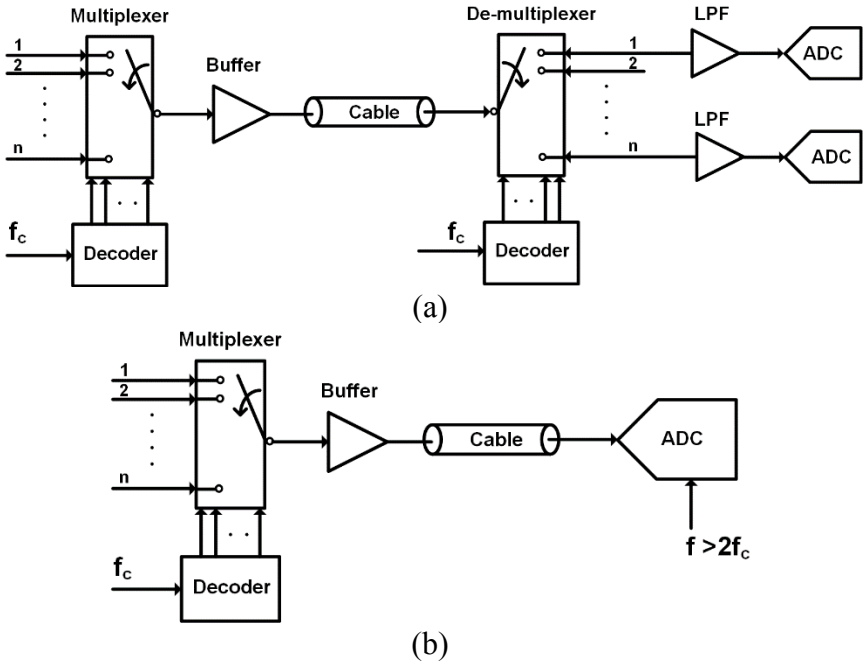



**Figure 3.** (a) Block diagram of standard Time-division multiplexing scheme and (b) reduced number of ADC scheme.

## 1.4 Transmitter Array Cable Reduction

Recent research shows that the transmit beamformer can be integrated in the application-specific integrated circuit (ASIC) to reduce the cable in transmitter (Tx) side. A column-row-parallel on-chip transmit beamformer was reported, however, it requires the number of cables proportional to the number of elements [38]. Another approach uses an external counter and the beamformer has limited operation ability which can only fire one pulse for each channel [39], [40]. On-chip beamformer with integrated counter was

presented in [41], however, it still requires multiple number of control signals to generate pulse for each channel.

## 1.5 Transmitter Technique for Increasing the Acoustic Pressure

In recent years, the capacitive micromachined ultrasound transducers (CMUT) have shown several advantages over the conventional bulk piezoelectric transducers, due to smaller size, wider bandwidth, and ease of integration with interfacing circuitry [42]. Compared to piezo-electric transducers, CMUTs typically have larger electrical impedances for the same transducer area. Although integration with reduced parasitics lead to low noise CMUT receivers [43], larger voltages are required to generate the required pressure output by CMUT transmitters as compared to piezoelectric transducers. Therefore, CMUT based ultrasound systems would benefit from high voltage (HV) ultrasound pulse generators that utilize the maximum available voltage level given the integrated circuit process constraints.

HV digital pulsers are commonly used in current commercial systems for their simplicity [44], while recent publications shows that linear amplifiers are also becoming attractive in driving piezoelectric transducers, capable of generating low harmonic content signals by adopting apodization profiles [45]. For a CMUT load, however, nonlinear distortion of the transducer can refute good linearity performance of the linear amplifier's output signal. Moreover, amplifiers have higher power consumption and considerable power loss when charging and discharging the CMUT parasitic capacitance, which reduce the pulser power efficiency [46]. A three-level pulser with pulse shaping and charge

recycling capabilities has been reported in [47], saving power in the pulser at the cost of requiring multiple supply voltages, which need HV DC-DC converters and extra capacitors, increasing overall system complexity and power consumption. Furthermore, there is demand for pulsers capable of generating versatile HV output waveforms efficiently within a compact chip area especially for applications such as intracardiac echocardiography (ICE) and intravascular ultrasound (IVUS) imaging, which are implemented on catheters that are only 1 mm to 3.3 mm in diameter (3–10 F) [48]-[55].

The main challenges in designing interface electronics in catheter based applications are limited space, temperature rise, supply voltage drop across long interconnects, and number of control lines in the catheter. These applications clearly benefit from interface electronics integration, such as CMUT-on-CMOS or flip-chip bonding [56], [57]. To further reduce the catheter electrical interconnect complexity, the ultrasonic transmitter (US-Tx) beam-forming, driver electronics and HV pulser can be integrated directly under the CMUT array. In addition, the CMUT fabrication processes allow for fabricating HV capacitors within its MEMS structure, which can be used in the pulser bootstrap circuit to further reduce the size and voltage drop across the long catheter wires by using a lower external supply voltage [58].

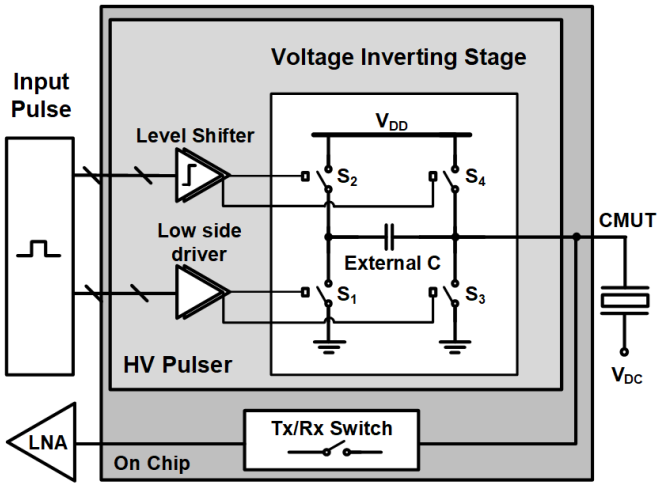
This thesis describes development and implementation of several integrated electronic techniques for high performance ICE catheters with cable reduction. In Chapter 2, high voltage pulser designs are introduced that are suitable for use with CMUTs and provide voltage levels exceeding the CMOS process limits by adopting dedicated protection technique. Chapter 3 focuses on design and verification of ASIC for 64 channel

single-chip reduced wire catheter system. Chapter 4 demonstrates the single-chip CMUT-on-CMOS system, showing compact and feasible package solution for ICE application. Chapter 5 describes the hybrid cable reduction system, which combines TDM system with sub-array beamformer ($\mu$-beamformer). The proposed system shows massive cable reduction in Rx circuitry, paving the way to design reduced wire 2D array system. Finally, Chapter 6 concludes the thesis and describe future works.

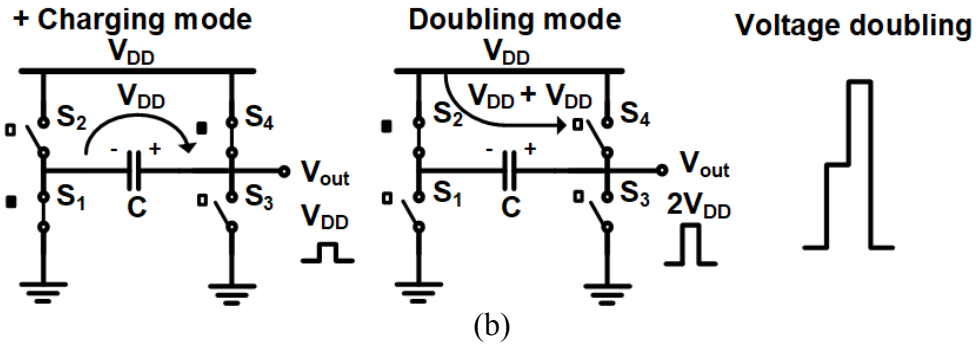
# CHAPTER 2. SUPPLY- DOUBLED PULSER DESIGN FOR CMUTS

## 2.1 Three Level Supply-Doubled Pulser

Capacitive micromachined ultrasound transducers (CMUT) have been shown to have many advantages for medical ultrasound imaging systems, such as compact size, integration with analog front-end circuits, and wide bandwidth. However, CMUTs are prone to having low transmit sensitivity, and one way to overcome this limitation is using higher pulse voltages. Moreover, advanced 3-D ultrasound applications, such as Intracardiac echocardiography (ICE) and intravascular ultrasound (IVUS) imaging, require integration of the interface electronics with the CMUT arrays in a very limited space, in which low supply voltages are preferred for safety reasons.




(a)




(b)

**Figure 4.** (a) A simplified schematic diagram of the supply-doubled (inverted) high voltage pulser, and (b) the operation of voltage doubling stage.

Capacitive micromachined ultrasound transducer (CMUT) has shown many advantages in ultrasound medical imaging, such as compact size, integration with analog front-end circuits, and wide bandwidth. However, CMUTs are prone to having low transmit sensitivity, and one way to overcome this limitation is using higher pulse voltages. Moreover, advanced 3-D ultrasound applications, such as Intracardiac echocardiography (ICE) and intravascular ultrasound (IVUS) imaging, require integration of the interface electronics with the 2-D CMUT arrays in a very limited space, in which low supply voltages are preferred for safety reasons.

The primary objective of voltage-doubling circuit is to generate sharp pulses with amplitudes close to twice the supply voltage without violating safe operating range of its circuit elements [58]. A simplified schematic diagram of the proposed pulser is depicted in Figure 4(a).

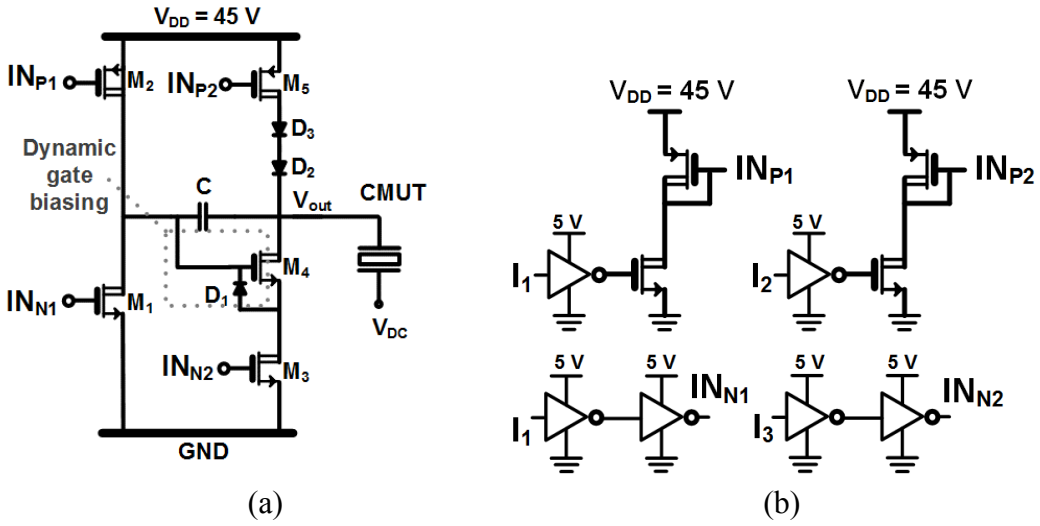



**Figure 5.** (a) Schematic of the proposed voltage doubled pulser. (b) Schematic of the input driving buffers and level shifters for high voltage PMOS input signals.

The external control logic generates low voltage control signals and level shifters convert the dc voltage levels to drive double-diffused metal oxide semi-conductor (DMOS) transistors of the pulser. Figure 4(b) shows operation of the voltage doubling stage. A capacitor, C, which can be on-chip or integrated with the CMUT array, is charged to $V_{DD}$ during charging mode through $S_1$ and $S_4$. Then, a HV switch, $S_2$, drives the negative terminal of C to $V_{DD}$ during doubling mode, while all other switches are open for $V_{out}$ to reach $2V_{DD}$. $S_3$ is used to discharge C by connecting it to ground. The CMUT can be modeled mainly as a capacitive load, resulting in a capacitive voltage divider between C and CMUT, which indicates the actual output pulse voltage. The voltage doubling stage requires careful design because it goes beyond the process operating voltage. To ensure safe operation, we employed dynamically gate-biased transistor stack and Schottky diodes to protect all the transistors from out of range operating conditions.

Figure 5 shows detailed schematic of the proposed pulser, which is driven by three input control signals ($I_1$, $I_2$, and $I_3$). Two N-type DMOS transistors, $M_1$ and $M_3$, are driven by 0 - 5 V control signals. Two P-type DMOS transistors, $M_2$ and $M_5$, are driven by 40 - 45 V level-shifted control signals. Note that in this case, $V_{DD}$ = 45 V. To achieve a compact design, simple level shifters are used in Figure 5(b), while ensuring that $IN_{P1}$ and $IN_{P2}$ generate 40 – 45 V sharp pulses with low current consumption, compared to the CMUT driving stage [59].

The circuit operation is similar to the bootstrapping circuits in [60]-[64]. During charging mode, the external capacitor, C, is charged up to $V_{DD}$ - ($V_{D2}$ + $V_{D3}$) by turning on $M_1$ and $M_5$ transistors, where ($V_{D2}$ + $V_{D3}$) is the forward voltage drop across $D_2$ and $D_3$. When C is charged, we turn on $M_2$ and turn off all the other transistors so that $V_{out}$ is bootstrapped to $2V_{DD}$ - ($V_{D2}$ + $V_{D3}$). During this doubling mode, it is crucial to ensure that all devices in the circuit are operated in their safe operating conditions, considering the fact that in this process, the drain-source junction breakdown and gate-oxide breakdown voltages are 60 V and 5 V, respectively. To prevent excessive $V_{DS}$ on $M_5$ and its parasitic N-well substrate diodes from turning on, two HV Schottky diodes are added in series with $M_5$. Each diode has a maximum reverse voltage of 36 V, and when the output is doubled, the two diodes should handle 45 V of total reverse voltage between them, resulting in each diode having reverse voltage well below its limit. Between $V_{out}$ terminal and GND, stacked N-type DMOS transistors, $M_3$ and $M_4$, are used to ensure safe operation when $V_{out}$ is doubled. The gate of $M_4$ is dynamically biased to $V_{DD}$ during doubling mode, while $M_3$ is

turned off. The Zener diode, $D_1$, keeps $V_{GS}$ of $M_4$ below 5 V, so that $M_3$ and $M_4$ can divide the doubled output voltage across their designated drain-source voltage limit.

The value of external capacitor, C, is key to determine the pulser Vout and slew rate according to,

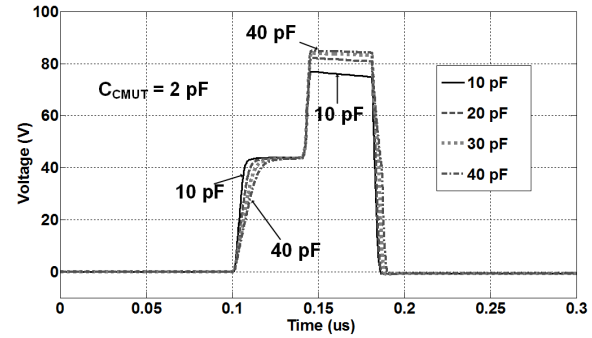
$$V_{out1} = V_{DD} - (V_{D2} + V_{D3}) \tag{4}$$

$$V_{out} = V_{DD} + V_{out1} \times \frac{C}{C + C_{CMUT}} \tag{5}$$

where $C_{CMUT}$ is the equivalent capacitance of the CMUT. Therefore, C should be large to obtain higher $V_{out}$. However, larger C would increase the output RC time constant, limiting the operating frequency range and slew rate of output pulses,

$$SR = \max(\frac{dV}{dt}) = \frac{I_{\max}}{C + C_{CMUT}} \tag{6}$$

where $I_{max}$ is the maximum current sourced to capacitance. By decreasing slew rate, Vout will suffer from slow charging problem. Moreover, if C is integrated in the CMUT, its value may be limited by the size of the CMUT. Thus deciding the optimal value of C is critical in the pulser design. In this study, we consider a particular application of 2-D CMUT array for intracardiac echography (ICE), where the center frequency is about 8.3 MHz and CMUT array element size is limited to approximately 100 × 100 $\mu m^2$, resulting in $C_{CMUT}$ = 2 pF. We also investigated the case for an 8 pF device capacitance, the capacitance of the CMUT when probed by an oscilloscope probe (P6139A, Tektronix) for electrical characterization.

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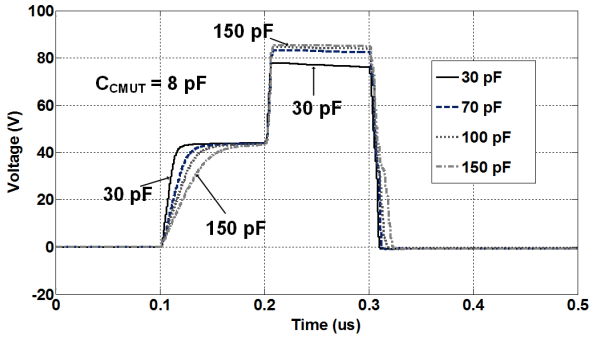



(b)

**Figure 6.** Simulation of the output pulse with different *C* values, (a) when CMUT loading is considered 2 pF, (b) $C_{CMUT}$ = 8 pF.

A realistic design target for the pulser would be to achieve peak HV level of at least 1.8 × VDD while having a rise time less than a quarter period of the CMUT center frequency, i.e. 30 ns for the 8.3 MHz CMUT. (1) and (2) suggest that the minimum required C would be > 4 × $C_{CMUT}$. Considering the forward voltage drop across the diodes and parasitic capacitances of the large DMOS transistors, we chose C = 30 pF for 2 pF of CCMUT. Also to obtain SR > 3 V/ns during the charging mode, we designed $M_5$ to have $I_{max}$ > 100 mA, based on (3). Since the size of large DMOS transistors mainly define the layout size, we chose Imax for driving a 2 pF CMUT load at 8.3 MHz center operating frequency. Figure 7 shows the comparison between simulation and measurement results with three control signals, $I_1$, $I_2$, and $I_3$.

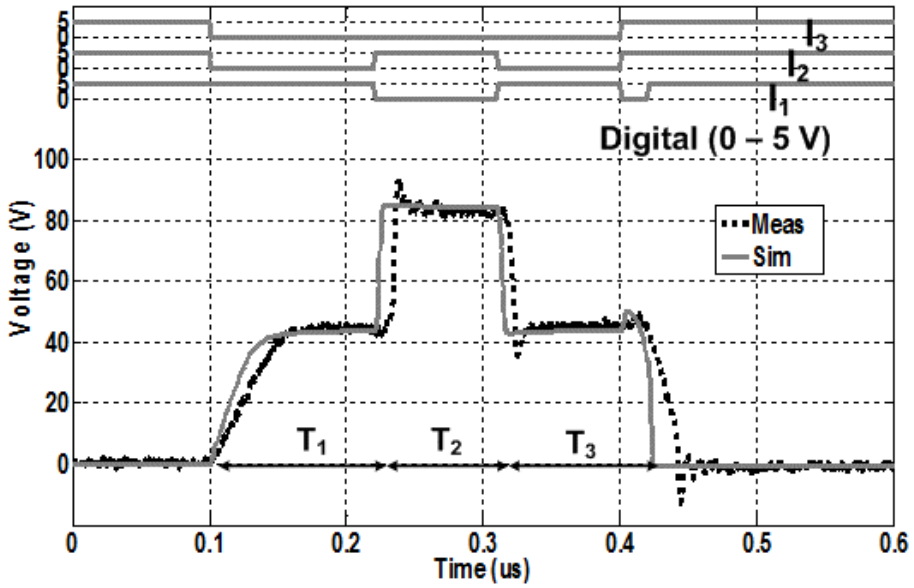



**Figure 7.** Simulated and measured three-level output pulse along with three input control signals. $C$ = 100 pF, $C_{CMUT}$ = 8 pF.

To verify the pulser design and compare with measurements we simulated the voltage-doubled output pulse for 2 pF of CMUT load and 8 pF of passive probe loading, for which C was changed within 10 - 40 pF and 30 - 150 pF, respectively. For ensuring the initial condition of Vout = 0 V, a 100 kΩ resistor was added in parallel with C, which adds a slight slope on doubled output pulse with minimal effect on output voltage division. With 2 pF load, C = 30 pF shows 85 Vpp of output pulse, rise time of 11.5 ns, and SR = 3.2 V/ns in the charging mode, which is suitable for driving a CMUT array with 8.3 MHz center frequency. With 8 pF load, C = 100 pF shows 85 Vpp of output pulse, rise time of 34.8 ns, and SR = 1.0 V/ns during charging mode. The slew rate of the doubling stage does not depend on the value of C, as evident in Figure 6, because the charged C is simply connected in series with $V_{DD}$.

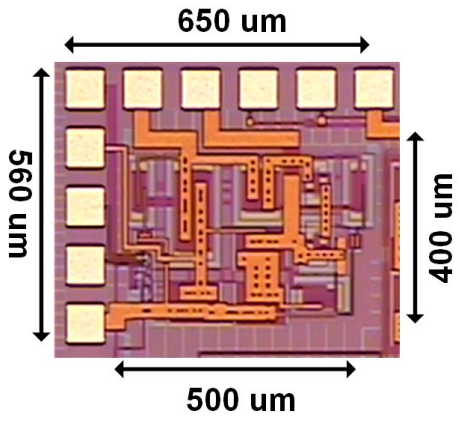



**Figure 8.** Microphotograph of the proposed pulser chip.

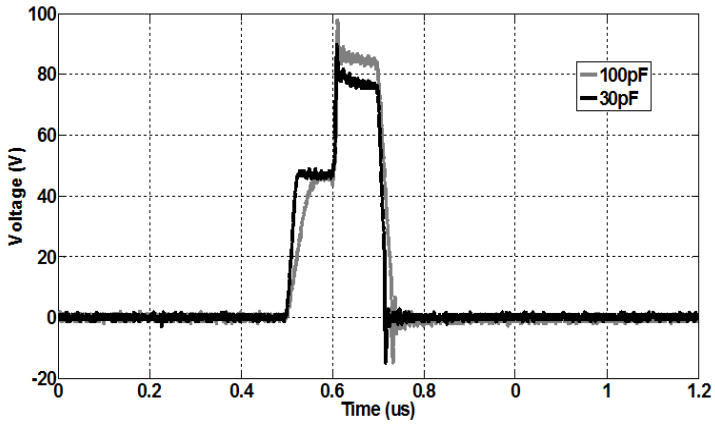



**Figure 9.** Measured output pulse with $C$ = 30 pF and 100 pF when CMUT loading is 8 pF.

The proposed pulser was designed and fabricated in a 0.18-μm 60 V power management 4M1P HV-CMOS process, and occupied a core area of 0.2 $mm^2$, as shown in Figure 8. The chip was mounted on a PCB inside a QFN package along with an off-chip surface mount capacitor, $C$. Figure 9 shows the measured output voltage with two different $C$ and more than 8 pF loading, including the input capacitance of a passive probe and parasitic capacitance of wire-bonding and PCB routing in parallel with 100 kΩ resistor. The measured waveform with $C$ = 100 pF, shows peak $V_{out}$ = 85 V and slew rates of 0.88

V/ns, 3.2 V/ns, and 2.44 V/ns during charging, doubling, and falling modes, respectively. Similarly, with $C = 30$ pF, peak $V_{out} = 78.6$ V was achieved with slew rates of 2.1 V/ns, 2.9 V/ns, and 4.7 V/ns, respectively. Figure 7 shows a sample measurement with non-zero $T_1$, $T_2$, and $T_3$ values overlapped for comparison with the simulations.

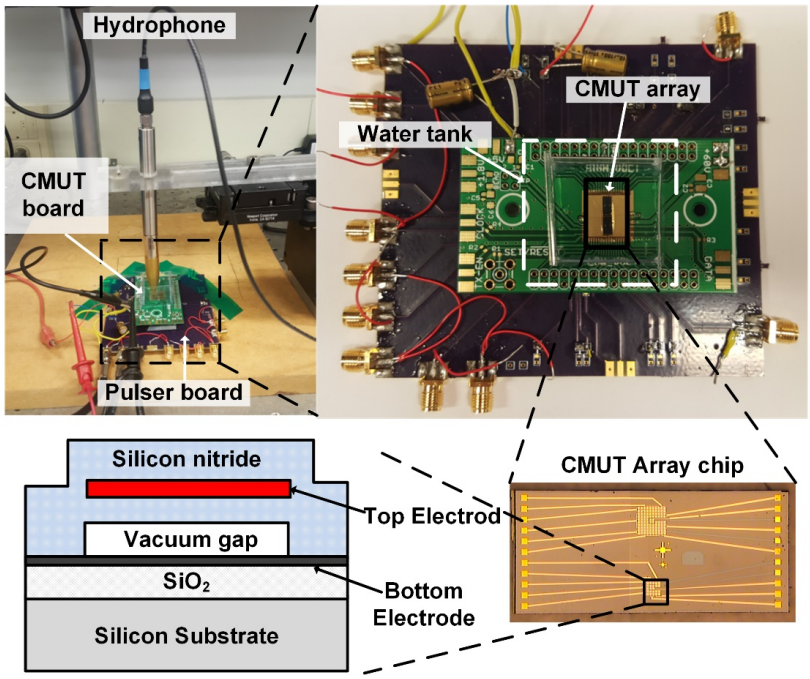
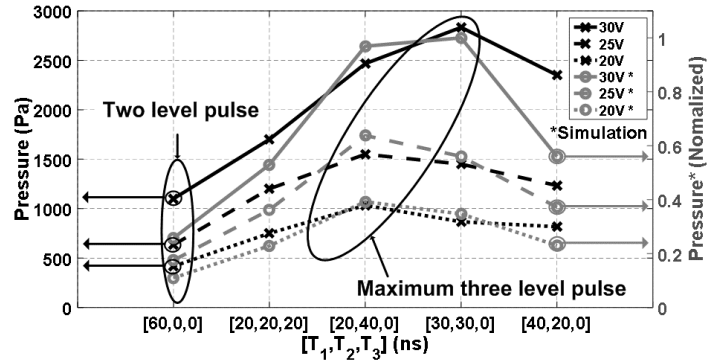
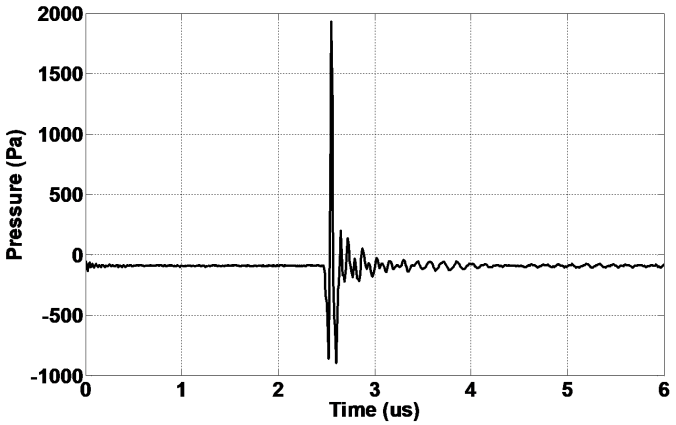



**Figure 10.** Acoustic pressure experimental setup with CMUT array board and pulser board.

An acoustic pressure measurement setup was used to measure the US-Tx pressure with an actual CMUT load, as shown in Figure 10. The CMUT used in this experiment occupied 100 × 100 $\mu$m$^2$ area on silicon and consisted of a 2 × 2 array of four 45 $\mu$m wide square membranes. It created a 2 pF element, ~1.8 pF of which was due to bond pads parasitic capacitance, with 8.33 MHz center frequency and -3 dB bandwidth of 5 MHz. It was part of a larger 2-D ICE imaging array, which was fabricated using a low temperature CMOS-compatible process.




(a)




(b)

**Figure 11.** (a) Transmitted peak-to-peak acoustic pressure measurement and simulation with different pulse shapes and supply voltages. (b) Measured transmitted pressure with $T_1$ = 30 ns, $T_2$ = 30 ns, $T_3$ = 0 ns, and $V_{DD}$ = 30 V.

The CMUT array, mounted on a separate PCB, was connected to the larger pulser board via header pins. The off-chip capacitor, C = 30 pF, was selected to obtain maximum output swing and fast slew rate as discussed. The CMUT array was submerged in a water tank, while a hydrophone (HGL-0085, Onda Corp) was placed above the CMUT array, 4.5 mm from its surface, to measure the US-Tx acoustic pressure. The measured peak-to-peak US-Tx pressure results are summarized in Figure 11. $V_{DD}$ in these experiments was reduced to 30 V because the CMUT breakdown voltage was 60 V. The maximum peak-to-peak

pressure of 2467 Pa was recorded with [30, 30, 0], as shown in Figure 11(b). Table 1 summarizes the pulser specs for the [30, 30, 0] pulse shape and benchmarks its performance against prior work.

Table 1. Benchmarking of the proposed pulser performance.

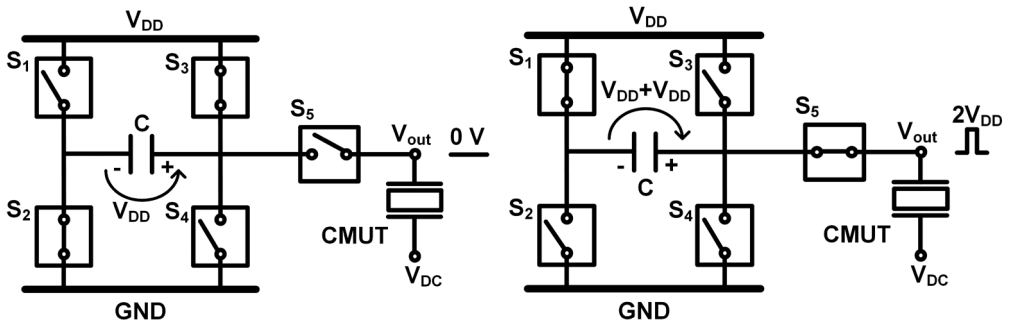
| **Parameter** | **This work** | **[47]** | **[59]** | **[65]** |
|---|---|---|---|---|
| **Input voltage (V)** | 5 | 3.3 | 3.3 | 1.8 |
| **Output voltage (V)** | 85 | 30 | 60 | 12.8 |
| **$V_{DD}$ (V)** | 45 | 30 | 60 | 12.8 |
| **Frequency (MHz)** | 8.33 | 2.5 to 5 | 1.38 | 1.25 |
| **Rise/fall time (ns)** | 26,16/18 | 30 | 68/68 | 40/50 |
| **Power (mW)** | 48.6 | 52.4 | 98.1 | |
| **Power (mA)** | 150 Dynamic * | - | - | 19.9 Dynamic * |
| **Chip area ($mm^2$)** | 0.2 | - | 0.08 | 0.022 |
| **Output load (pF)** | 2 | 40 | 18 | 15 |
| **Pulse shaping** | Y | Y | N | N |
| **Technology (μm)** | 0.18 | 0.18 | 0.35 | 0.18 |

This chpater presents an integrated voltage-doubling and pulse-shaping HV pulser circuit to interface CMUT ultrasound systems in a 0.18-μm 60 V 4M1P CMOS/DMOS process. The presented circuit overcomes process limitation by adopting HV protection techniques that generate 85 Vpp of output pulse with 45 V supply voltage. A three level pulsing scheme is successfully applied to a CMUT array element and optimized for maximum acoustic pressure, as predicted by a large signal CMUT model, paving the way for simulation-based CMUT pulser optimization. The prototype pulser ASIC measurements were conducted with an off-chip capacitor, which can be integrated with the

CMUT using high-K dielectric layers during CMUT fabrication. Ongoing research involves co-optimization of the pulser and CMUT arrays using CMUT-on-CMOS technology for very compact catheter-based ultrasound imaging systems.

## 2.2 Two Level Supply-Doubled Pulser

Unipolar digital pulsers have often been used in integrated ultrasound systems, but recently linear amplifiers and three-level pulser topologies have also shown good performance in terms of low harmonic content and power efficiency, respectively. However, these new circuits require additional auxiliary blocks, such as digital-to-analog converters (DAC) and DC-DC converters with extra capacitors, which would increase the overall system complexity. In the previous section, a 3-level supply-doubled pulser using boot-strapping circuit to overcome the HV supply limitation was described and used for pulse-shape optimization. However, that circuit requires three different input control signals, and unavoidably has to deal with middle level transitions.




(a) (b)

**Figure 12.** Simplified schematic diagram of the proposed pulser during (a) charging and (b) voltage doubling phases.

The proposed pulser is designed to generate two-level sharp pulses with supply-doubled voltage [66]. A simplified schematic diagram of the proposed pulser is shown in Figure 12. The operation of pulser is similar to a bootstrap switch. A capacitor, C, is charged to $V_{DD}$ during charging phase through HV switches, $S_2$ and $S_3$, while all the other HV switches are open, and $V_{out}$ stays 0 V. When C is fully charged, $S_1$ drives the negative terminal of $V_{DD}$ and $S_5$ connects the charged C to $V_{out}$ that theoretically reaches $2V_{DD}$ during the voltage doubling phase. Subsequently, $S_4$ and $S_5$ are closed to return $V_{out}$ back to 0 V, and the same sequence repeats after $S_5$ opens to detach Vout from the charging C. The CMUT is often modeled as a mainly capacitive load, which is connected to Vout. The actual output pulse voltage can be found from the capacitive voltage division between C and CMUT. Hence, deciding the optimal value of C, depending on the CMUT specs is quite important in design of this pulser. The proposed pulser also requires careful design because it can go beyond the process limitations. Therefore, the pulser features stacked dynamically gate-biased transistors, Schottky diodes, and Zener diodes to protect all the transistors from consequences of "out of range" operation. Figure 13 shows the detailed schematic diagram of two level suppy-doubled pulser.

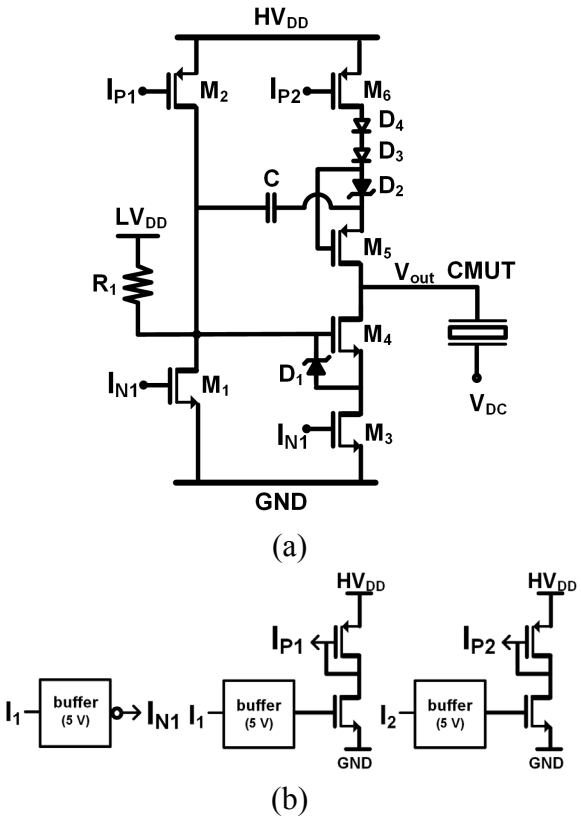



**Figure 13.** Schematic diagram of (a) the proposed pulser and (b) input driving buffers and level shifters.

The proposed pulser utilizes double-diffused metal oxide semiconductor (DMOS) transistors, Schottky diodes, and Zener diodes, as shown in Figure 13. The digital control logic from an external pulse generator control two 5 V input signals ($I_1$ and $I_2$), needed to control the pulser. Two N-type DMOS transistors, $M_1$ and $M_3$, are driven by 0 - 5 V control signals. Two P-type DMOS transistors, $M_2$ and $M_6$, are driven by level-shifted high voltage control signals. Level shifters are designed compactly to generate 40~45 V sharp signals ($I_{P1}$ and $I_{P2}$), when $HV_{DD}$ = 45 V, with little current consumption compared to the CMUT driving phase to drive high side of supply-doubled stage of pulser, as shown in Figure 13(b). $M_4$ and $M_5$ are dynamically gate biased during the voltage doubling phase.

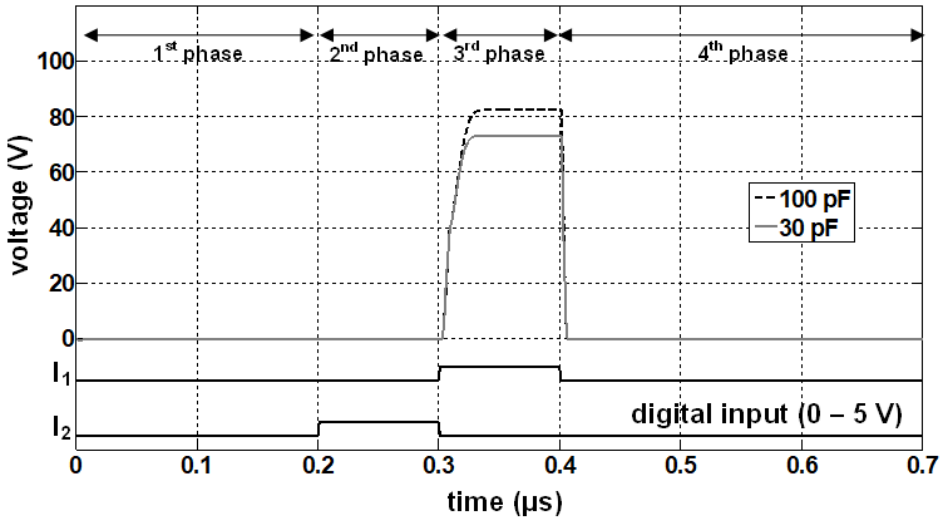



**Figure 14.** Simulation of the control inputs and output pulse with different *C* values, when CMUT loading is considered 8 pF, and $HV_{DD}$ = 45 V.

In a closer look, the circuit operation can be divided into four phases, as shown in Figure 14. During the first phase, $M_3$ is turned on to connect $V_{out}$ to 0 V. Note that the gate of $M_4$ is connected with pull-up resistor to $LV_{DD}$ = 5 V as its initial phase. In phase 2, the off-chip capacitor, *C*, is charged up to $HV_{DD}$ - ($V_{D2}$ + $V_{D3}$ + $V_{D4}$) by turning on $M_1$ and $M_6$ transistors, where ($V_{D2}$ + $V_{D3}$ + $V_{D4}$) is the forward voltage drop of two Schottky and a Zener diode of the same names in series. The forward voltage drop of $D_2$ also ensures that $M_5$ remains off during this phase, such that $V_{out}$ continues to stay at 0 V. Once *C* is fully charged, in the third phase, $M_2$ is turned on, while all other controllable transistors are turned off. This operation employs bootstrapping technique with the charged *C* connected in series with $HV_{DD}$ through $M_2$, resulting in $V_{out}$ to be boot-strapped to nearly 2 $HV_{DD}$. During this phase, Zener diode, $D_2$, is reverse biased with 5 V across it, turning on $M_5$, which is a P-type DMOS, to connect the charged *C* to $V_{out}$.

It is necessary to make sure that all devices in the circuit are operated in their safe operating conditions, considering the fact that in this 0.18 $\mu$m Bipolar-CMOS-DMOS (BCD) process, the maximum permissible drain to source and gate to source voltages are 60 V and 5 V, respectively. To ensure $M_6$, which is a P-type DMOS transistor, operates in the safe region, $D_3$ and $D_4$, which are HV Schottky diodes, are added in series to $D_2$. Each Schottky diode has a reverse break down voltage of 36 V, and together, they can protect against 45 V of reverse voltage during the voltage doubling phase by dividing the reverse voltage within their limits. Also $M_3$ and $M_4$, which are N-type DMOS transistors, are stacked to handle supply-doubled output signal while the gate of $M_4$ is dynamically biased to $HV_{DD}$. The Zener diode, $D_1$, keeps $V_{gs}$ of $M_4$ below 5 V, so that $M_3$ and $M_4$ can divide the supply-doubled voltage, which is above the process limit, among them.

The value of $C$ is an important parameter that determines $V_{out}$ according to,

$$V_{cap} = HV_{DD} - (V_{D2} + V_{D3} + V_{D4}) \tag{7}$$

$$V_{out} = HV_{DD} + V_{cap} \times \frac{C}{C + C_{CMUT}} \tag{8}$$

where $C_{CMUT}$ is the equivalent capacitance of the CMUT. Larger $C$ would increase $V_{out}$, resulting in higher voltage swing. However, it also increases the charging time in the second phase. Hence, $C$ should be selected carefully. Moreover, if in the future, $C$ is integrated with the CMUT by adding more layers with high-K dielectric in the MEMS process, the maximum available size would be limited by the area of the CMUT. Figure 14 shows the simulation results, while connecting the output node to equivalent CMUT

loading of 8 pF, which is the same as the input capacitance of the oscilloscope probe, P6139A (Tektronix, Beaverton, OR). The design target for the pulser would be to achieve maximum peak-to-peak voltage level of $1.8\times HV_{DD}$, while having rise- and fall-times less than a quarter period of the center frequency of the CMUT, which is 30 ns for 8.33 MHz. (1) and (2) suggest that the minimum required $C$ would be larger than $4\times C_{CMUT}$. However, considering the forward voltage drop across diodes, parasitic capacitances of the large DMOS transistors, and PCB parasitic capacitance, $C$ was chosen $\sim 12\times C_{CMUT}$. As simulation shows in Fig. 3, of $C$ = 30 pF was not sufficient to drive the 8 pF capacitive load up to $1.8HV_{DD}$, while $C$ = 100 pF resulted in $V_{out} > 1.8HV_{DD}$. The rise-time and fall-time are fast enough because during rise-time, charged $C$ is simply connected in series with $HV_{DD}$, while during fall-time, one node of $C$ is floating, and the load capacitance is only $C_{CMUT}$ and parasitic capacitance. The size of $M_6$ is selected such that it can deliver more than 100 mA to fully charge $C$ = 100 pF within the second phase, which is about 100 ns. During the 4th phase, $M_3$ pulls down $V_{out}$ to 0 V to complete generation of the sharp two-level pulse.

The proposed pulser is designed and fabricated in a 60 V 0.18-$\mu$m power management BCD process. The core of the pulser occupies 0.258 mm$^2$ of silicon area, as shown in Figure 15. The chip was mounted on a PCB within a QFN package with a 100 pF off-chip surface mount (SMD) capacitor. Figure 16 compares the measured output voltage with simulation results, which shows very good agreement. During measurement, $C_{CMUT}$ was replaced with an oscilloscope probe that has 8 pF parasitic capacitance (P6139A, Tektronix) and $HV_{DD}$ = 45 V. The measured waveform shows $V_{out}$ = 84.2 V, and

peak rise and fall slew rates of 2.52 V/ns and 7.5 V/ns, respectively, which are suitable for driving an 8 pF CMUT load with 8 MHz center frequency. Measurements from over 10 chips have shown consistent results with $V_{out}$ (mean±std) = 84.03 ± 1.28 V, indicating reliability of this HV pulser circuit.

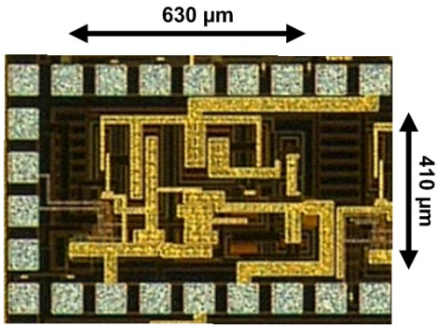



**Figure 15.** Microphotograph of the proposed pulser.

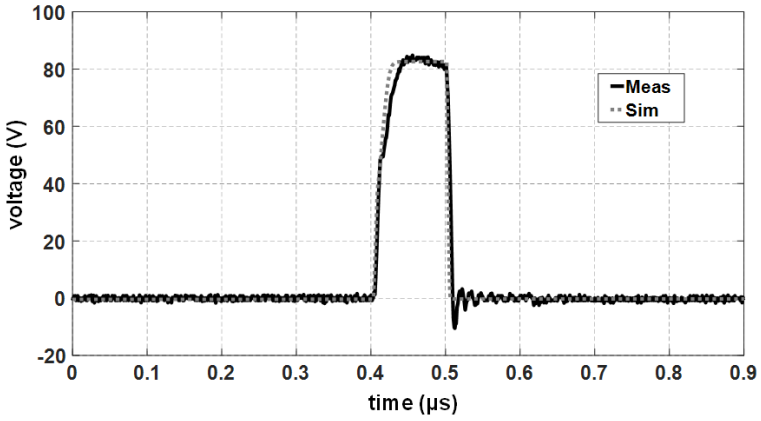



**Figure 16.** Measured and simulated supply-doubled pulse, when *C* and CMUT loading are considered 100 pF and 8 pF ($HV_{DD}$ = 45 V).

An acoustic pressure measurement setup was used to measure the transmitted ultrasonic pressure with a CMUT, fabricated in our in-house process. Figure 17 shows the layout and cross-sectional view of the CMUT. The CMUT used to test the pulser in this measurement occupies 100 × 100 $\mu m^2$ on silicon substrate and consists of a 2 × 2 array of

four 45 $\mu$m wide square membranes, fabricated using a low temperature CMOS-compatible process. The CMUT characterization shows 2 pF capacitance and 8.33 MHz of center frequency, with 5MHz of -3dB bandwidth. The CMUT array was mounted on a separate PCB and connected to the pulser PCB via vertical connection line, as shown in Figure 18.

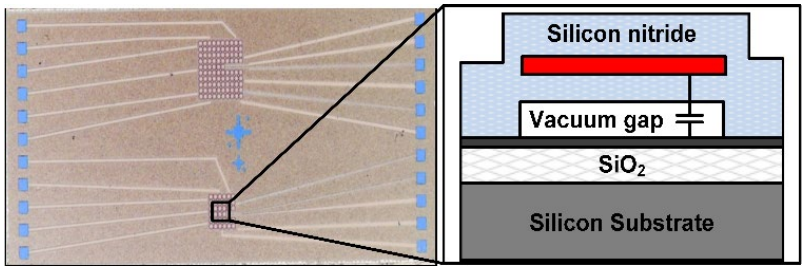



**Figure 17.** Layout of the CMUT array, and cross-section view of CMUT layers.

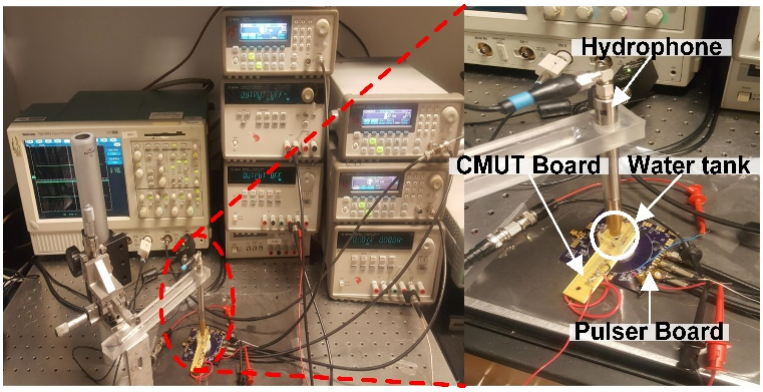



**Figure 18.** Acoustic measurement setup for testing the proposed pulser with a CMUT array.

By selecting $C$ = 100 pF, the pulse can drive up to 8 pF of capacitive loading with fast-enough output swings, considering large parasitic capacitance added to the CMUT setup by the interconnects and the PCB. The CMUT array was submerged in water in a small container, while a hydrophone (HGL-0085, Onda Corp, Japan) was aligned above

the CMUT array, 5.9 mm from its surface, to measure the transmitted ultrasonic acoustic pressure. $HV_{DD}$ in this measurement was lowered to 20 V, because the collapse voltage of the CMUT is ~40 V. The proposed supply-doubled pulser generates ~2 $kPa_{p\text{-}p}$ with $V_{out} \approx$ 36 V, which is more than twice the pressure pulse generated when the same CMUT was driven by a conventional supply-limited pulser (~0.92 $kPa_{p\text{-}p}$, $V_{out} \approx$ 20 V). This is because of the nonlinear CMUT characteristic in large signal operation, resulting in the proposed pulser being able to generate larger pressure in a limited-supply voltage environment.

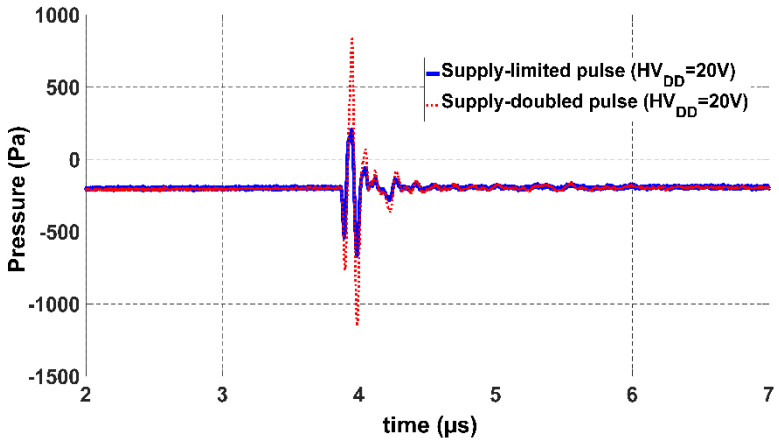



**Figure 19.** Measured transmitted pressure with CMUT. Blue line shows the pressure of conventional supply-limited pulser, red dot-line shows the pressure of supply-doubled proposed pulser.

The new pulser performance is summarized in Table 1, and compared with the prior work in the literature. Power consumption is calculated by assuming that the proposed pulser would be used in an imaging system up to a depth of 7.5 cm with 1 to 10 ratio of Tx and Rx periods with one pulse firing. The proposed pulser shows successful operation

beyond process voltage limits, while maintaining fast slew rates to drive CMUTs operating in 8.33 MHz range.

**Table 2.** Benchmarking of the proposed two level pulser performance.

| **Parameter** | **[47]** | **[58]** | **[65]** | **This work** |
|---|---|---|---|---|
| Input voltage (V) | 3.3 | 5 | 1.8 | **5** |
| Output voltage (V) | 30 | 85 | 12.8 | **84.2** |
| $V_{DD}$ (V) | 30 | 45 | 12.8 | **45** |
| Frequency (MHz) | 2.5 - 5 | 8.33 | 1.25 | **8.33** |
| Rise/fall slew rate (V/ns) | 1/1 | 1.73,2.5/4.7 | 0.32/0.25 | **2.52/7.5** |
| Power (mW) | 52.4 | 48.6 | - | **51.8** |
| Peak current (mA) | - | 150 Dynamic* | 19.9 Dynamic* | **160 Dynamic*** |
| Chip area ($mm^2$) | - | 0.2 | 0.022 | **0.258** |
| Output load (pF) | 40 | 8 | 15 | **8** |
| Technology (μm) | 0.18 | 0.18 | 0.18 | **0.18** |

* Simulation results

In conclusion, this section presented a HV pulser with the ability to drive CMUT arrays beyond the supply voltage. The new pulser has been implemented in a 0.18-μm 60 V Bipolar-CMOS-DMOS (BCD) process. The proposed circuit overcomes process limitation, adopting HV protection techniques and combining them with a bootstrap topology. In our measurements, the pulser generated 84.2 $V_{pp}$ of output swing with a 45 V supply voltage. The close to doubled supply voltage can be generated with only two control signals at low voltage logic levels, simplifying the system design by eliminating the need for auxiliary blocks, such as DAC or DC-DC converter. The required capacitor, *C*, is too

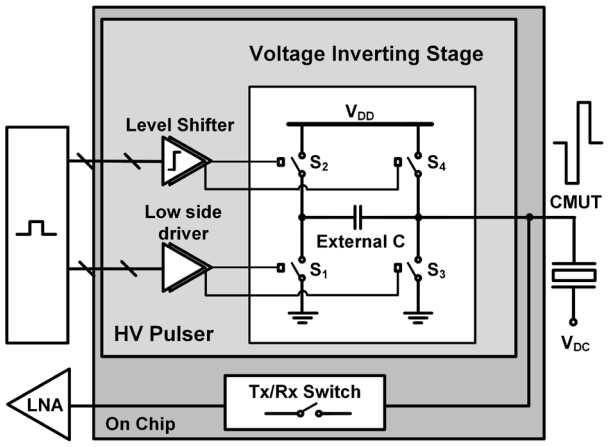
large to be integrated on-chip, but it can be integrated with the CMUT fabrication process using high-K dielectric layers. Therefore, the proposed beyond supply voltage pulser is expected to be an attractive candidate for highly-integrated CMUT-on-CMOS 2-D and 3-D ultrasound imaging architectures that are often supply voltage limited, and high drive pulses to improve CMUT output pressure and ultrasound image quality.

## 2.3 Supply-Inverted Pulser

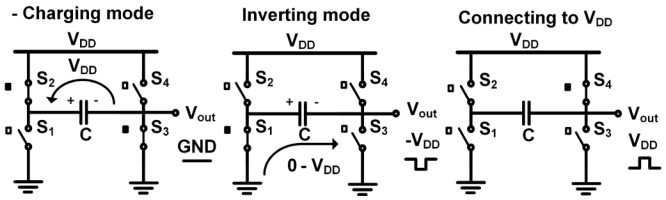
Two level high voltage (HV) digital pulsers are commonly used in CMUT ultrasound imaging systems for their simplicity. A three-level pulser with pulse shaping and charge recycling capabilities has also been reported in [47], saving power in the pulser at the cost of requiring multiple supply voltages, requiring HV DC-DC converters and extra capacitors and increasing the overall system complexity. Additionally, it is shown in [67] a differential three level pulser that achieves lower power consumption and area reduction compared to commonly used single ended pulsers. This differential pulser took advantage of the fact that each of the CMUT terminals can be connected to a different pulser obtaining a differential driving voltage. However, it still requires multiple HV supplies.

The integration of electronics with ultrasound transducer array would improve performance by reducing parasitic effect and removing long cable loading effect. A motivation for this pulser design is especially for compact catheter-based imaging applications, such as ICE and IVUS. This application can get advantages using this design by improving safety at lower cost by using lower voltages on the catheter without compromising the pulser voltage levels. One feasible solution is adopting bootstrapping

circuit in the pulser design, which is used in various applications such as improving accuracy for sample-and-hold circuits in analog-to-digital converters (ADC), and voltage level shifters of DC-DC converters. These circuits are widely used for generating twice the supply voltage to maximize the efficiency of circuit or to reduce ON-resistance of the switches. In cases where the CMUT fabrication processes allow HV capacitors to be built within their MEMS structure, these capacitors can be used in the pulser bootstrap circuit to further reduce the size and voltage drop across the long catheter wires by using a lower external supply voltage. Although this approach could also be applied to piezoelectric transducers, bootstrapping circuits requiring an extra HV capacitors would be more suitable for CMUT based catheters that utilize CMUT-on-CMOS or flip chip bonded CMOS electronics. A supply-doubled pulser using bootstrapping circuit for driving CMUT was proposed in previous sections, which showed pulse-shaping capability with a single HV supply. However, in that example it was limited to a positive unipolar pulse, and lacked a protection HV switch, prohibiting the use of the same CMUT element both for transmission and for reception.



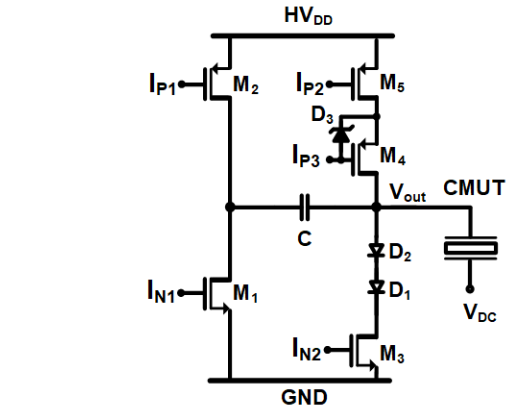

(a)



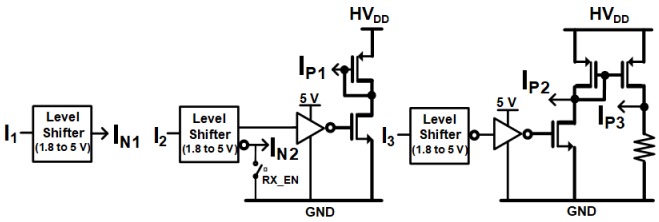

(b)

**Figure 20.** (a) Simplified schematic diagram of the proposed pulser and high voltage Tx/Rx switch, (b) the operation of voltage inverting stage.

In this chapter, a HV supply-inverted bipolar pulser combined with a Tx/Rx switch is presented. The pulser provides a HV output swing close to twice its supply voltage, and above the device breakdown, which is often limited by the CMOS process. The design goal of the supply-inverted pulser is to generate a bipolar pulse with peak-to-peak amplitude close to twice the supply voltage without requiring a negative HV supply. It is important to keep every circuit element operating in safe range, including receiver's low voltage (LV) devices during the supply-inverting operation. Figure 20(a) illustrates a simplified schematic diagram of the proposed pulser and Tx/Rx switch. The digital control logic from external pulse generators trigger low voltage control signals to drive N-type double-diffused metal oxide semi-conductor (DMOS) transistors to turn on/off low side switches. The level shifters convert the DC voltage levels of control signals to drive P-type DMOS transistors of the pulser to control high side switches. The Tx/Rx switch protects the low voltage receiver from HV signals including the negative part of the HV pulse. Blocking this negative HV pulse requires careful design as the output drops lower than the substrate voltage, which can cause parasitic diodes to switch on unexpectedly.




(a)




(b)

**Figure 21.** Schematic diagrams of (a) proposed supply-inverted pulser, (b) level shifters for high voltage NMOS/PMOS input signals of supply-inverted pulser

Figure 20(b) illustrates operation of the voltage inverting stage. A capacitor, *C*, which can be on-chip or integrated with the CMUT array, is charged to -$HV_{DD}$ during negative charging mode through $S_2$ and $S_3$. During this negative charging mode, $V_{out}$ is still at ground. After *C* is fully charged, then a HV switch, $S_1$, drives the positive terminal of *C* to *GND* during inverting mode, while all other switches are open, resulting in $V_{out}$ reaching -$HV_{DD}$. The CMUT can be regarded as a capacitive load, resulting in a capacitive voltage divider between *C* and the CMUT. All these circuits require careful design because they go beyond the normal process operating voltage. To ensure safe operation, stacked transistors, protection Zener diodes, and Schottky diodes are utilized to prevent any transistor from operating outside of its rated specifications.

Figure 21 shows a detailed schematic of the supply-inverted bipolar pulser, controlled by three 1.8 V input control signals ($I_1$, $I_2$, and $I_3$). These signals can be generated by on-chip control logic or an off-chip field-programmable gate array (FPGA). The N-type DMOS transistors, $M_1$ and $M_3$, are driven by 0 - 5 V control signals, while P-type DMOS transistors, $M_2$, $M_4$, and $M_5$, are driven by level-shifted HV control signals (note that in this case, $HV_{DD}$ = 45 V). Because of the large size of DMOS transistors, level shifters are designed as simple as possible, ensuring that $I_{P1}$ and $I_{P2}$ generate 40 – 45 V sharp pulses with small current consumption, compared to the CMUT driving stage, as shown in Figure 21. $M_4$, is driven by level-shifted 0 – 40 V control signal, $I_{P3}$, which ensures turning on $M_4$ when $M_5$ is on and protecting $M_5$ from the drain-source junction breakdown when $V_{out}$ is negative. The circuit operation is similar to the bootstrapping circuits. During negative charging mode, $C$ is charged up to $HV_{DD}$ - ($V_{D1}$ + $V_{D2}$) by turning on $M_2$ and $M_3$ transistors, where ($V_{D1}$ + $V_{D2}$) is the forward voltage drop across $D_1$ and $D_2$. When $C$ is fully charged, turning on $M_1$ and turning off all the other transistors drives $V_{out}$ to a negative voltage of -$HV_{DD}$ + ($V_{D1}$ + $V_{D2}$). During this inverting period, it is crucial to ensure that all devices in the circuit are operated in the safe zone, considering the fact that in this process, the drain-source junction breakdown and gate-oxide breakdown voltages are 60 V and 5 V, respectively. To prevent N-type $M_3$ from negative $V_{DS}$, two HV Schottky diodes, each of which can handle a maximum reverse voltage of 36 V, are added in series with $M_3$. When the output is inverted, these two diodes should handle 45 V of total reverse voltage between them, resulting in each diode having reverse voltage well below its limit. Two P-type $M_4$ and $M_5$ are stacked to ensure safe operation when $V_{out}$ is inverted. The gate of $M_4$ is biased

to 0 V during inverting period, while the Zener diode, $D_3$, keeps $V_{GS}$ of $M_4$ below 5 V, so that $M_4$ and $M_5$ can divide ~$2HV_{DD}$ across their designated drain-source voltage limit.

$$V_C = HV_{DD} - (V_{D1} + V_{D2}) \tag{9}$$

$$V_{out} = -V_C \times \frac{C}{C + C_{CMUT}} \tag{10}$$

The value of $C$ is a key factor in determining the inverted voltage of $V_{out}$ as shown in equations (9) and (10), where $C_{CMUT}$ is the equivalent capacitance of the CMUT. To achieve $V_{out} \approx -HV_{DD}$, we need $C >> C_{CMUT}$. However, large $C$ increases the RC time constant of the output during negative charging mode, limiting the operating frequency range and slew rate as in equation (11), where $I_{max\_negative}$ is the maximum current sourced to $C$ from P-type forward-biased $M_2$, which mainly depends on the size of driving DMOS transistors.

$$SR_{negative} = \max(\frac{dV}{dt}) = \frac{I_{\max\_negative}}{C} \tag{11}$$

It should also be noted that if $C$ is integrated in the CMUT, its value may be limited by the size of the CMUT, thus deciding the optimal value of $C$ is a key step the design of this supply-inverted pulser.

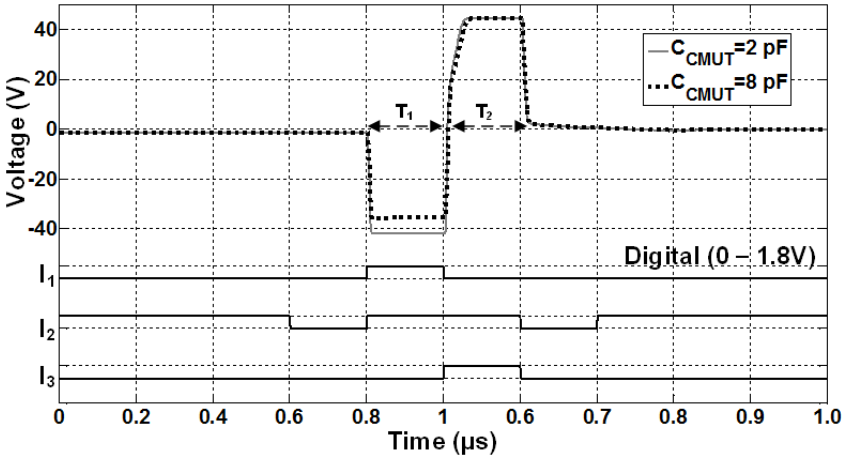



**Figure 22.** Simulation of the output pulse with different $C_{CMUT}$ values with 30 pF of $C$.

If we generate a bipolar pulse by firing the supply-inverted pulse first and positive pulse next, as shown in Figure 22, negative charging period happens before the firing, when $V_{out}$ is at *GND*. This time could be set to fully charge $C$ before firing, such that the slew rate during the negative charging mode would not be an issue. The supply-inverted pulse is generated by simply connecting the negatively charged $C$ in series with $C_{CMUT}$, in which case the output pulse voltage can be calculated as per equations (9) and (10). The pulse faces slow charging issue when $V_{out}$ needs to reach $HV_{DD}$ during the positive pulse generation, at which moment, $M_1$ and $M_2$ are turned off, and $M_4$ and $M_5$ are on. In the first part of this transition, when $V_{out}$ increases from $-HV_{DD}$ to *GND*, the voltage at the common drain of $M_1$ and $M_2$ goes from *GND* to $HV_{DD}$, because the charged capacitor drives this node at $HV_{DD}$ above $V_{out}$. This transition happens rapidly because the positive side of $C$, which is connected to the drain of $M_1$ and $M_2$, is floating. However, in the second part, when $V_{out}$ is going above *GND*, the positive side of $C$ tries to go over $HV_{DD}$, which results in reverse current in $M_2$ due to the negative $V_{SD}$ over this P-type DMOS, which is limited to around -0.7 V in this process. Therefore, reverse-biased $M_2$ connects the positive side of

$C$ to $HV_{DD}$, in parallel with $C_{CMUT}$, which is itself connected to another DC supply, $V_{DC}$. The slew rate of $V_{out}$ rising edge when it goes above *GND* is derived from equation (12), where $I_{max\_positive}$ is the maximum current of P-type $M_5$, which is partly flowing through $C$ and reverse-biased $M_2$ in series, and partly through $C_{CMUT}$. This indicates that larger values of $C$ could limit the rising edge slew rate during the positive $V_{out}$ transition. Therefore, the value of $C$ is a key factor that affects the pulser operating frequency.

$$SR_{positive} = \max(\frac{dV}{dt}) = \frac{I_{\max\_positive}}{C + C_{CMUT}} \tag{12}$$

In this prototype, we have considered the bipolar pulser for the application of driving a 2-D CMUT array in intracardiac echocardiography (ICE) with 8 MHz center frequency. The CMUT array element size is limited to 100 × 100 $\mu$m$^2$, resulting in $C_{CMUT}$ to be in the order of 2 pF. A realistic design target for the pulser would be to achieve negative peak HV level of at least -0.8 × $HV_{DD}$, with a rise time shorter than a quarter of the CMUT center frequency period, i.e. 31.25 ns for 8 MHz. According to (9) and (10), the minimum required $C$ would be larger than 4×$C_{CMUT}$. Considering the forward voltage drop across the diodes and parasitic capacitances of the large DMOS transistors, we chose $C$ = 30 pF for 2 pF of $C_{CMUT}$. Also to obtain $SR$ > 3 V/ns during the charging mode, $M_5$ is designed to have $I_{max}$ > 100 mA, based on (12). Since the size of large DMOS transistors mainly determine the layout size, $I_{max\text{-}positive}$ is chosen for driving a 2 pF CMUT load at 8 MHz operating center frequency. However, we also investigated the case for an 8 pF CMUT capacitance, represented by an oscilloscope probe (P6139A, Tektronix) in our characterization.

To verify the pulser design and compare with measurements, the voltage-inverted output pulse was simulated for 2 pF of CMUT load and 8 pF of passive probe loading, for which $C$ = 30 pF, as in Fig. 3. With 2 pF load, simulations show $V_{out}$ with 86.2 $V_{pp}$, 3.9 ns of first fall time, 25 ns of rise time, and 5.5 ns of second fall time, which is suitable for driving a CMUT array with 8 MHz center frequency. With 8 pF load, simulations show output pulses with 80.3 $V_{pp}$, 4.3 ns of first fall time, 31 ns of rise time, and 6 ns of second fall time. Note that in Fig. 3, the pulser operation begins from 0.6 $\mu$s by charging $C$. By controlling $I_1$, $I_2$, and $I_3$, the pulse shape and duty cycle of the output pulse can be fine-tuned to generate bipolar pulses with optimal shape that would maximize the acoustic pressure generated by the CMUT.

The Tx/Rx switch located between HV pulser and LV receiver, toggles between transmit and receive mode to prevent HV pulses from damaging the LV receiver circuits. This is a critical circuit in highly integrated ultrasound imaging systems when the ultrasound pulse transmitting and echo receiving circuits interface with the same CMUT element. Since the proposed supply-inverted pulser generates negative HV pulse, which is lower than the ASIC substrate voltage, the Tx/Rx switch requires a careful protection scheme. Conventional Tx/Rx switches consist of two NMOS transistors requiring several level shifted control signals and both positive and negative HV supplies to block HV bipolar pulse during Tx mode. This approach increases the design complexity. The proposed Tx/Rx switch does not need extra level shifted control signals and protects the LV circuits without dual HV supplies, simplifying the design, as a result.

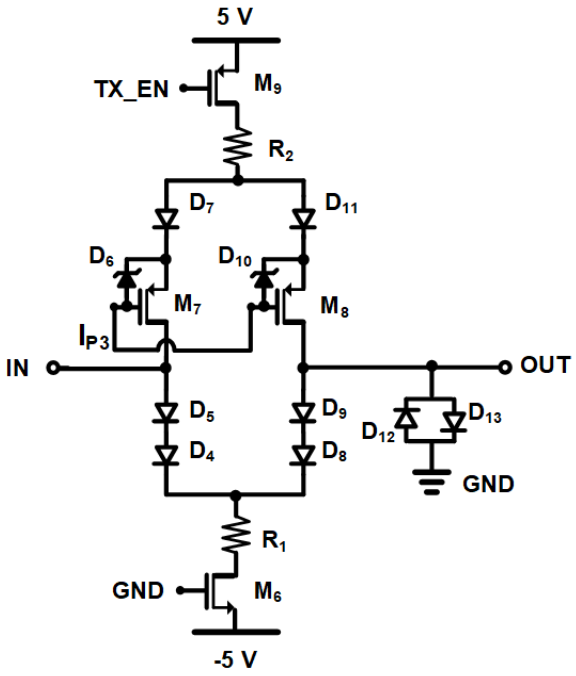



**Figure 23.** Schematics of proposed protection Tx/Rx switch for voltage-inverted pulser.

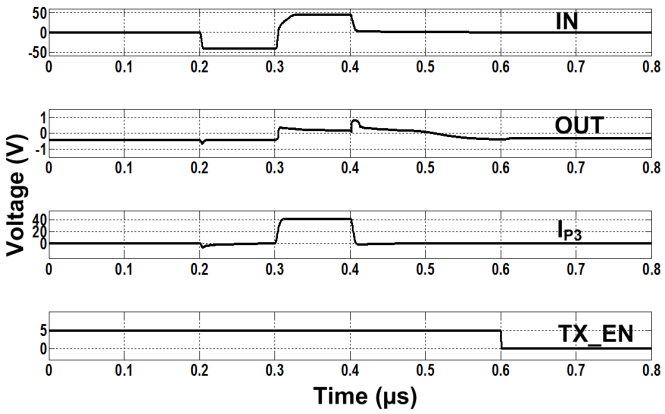



**Figure 24.** Simulation result of the Tx/Rx switch, IN is connected to the output of supply-inverted pulser during Tx period.

Figure 23 shows the proposed Tx/Rx switch schematic, which consists of a diode-bridge, biasing current sources, and clamp diodes, similar to off-the-shelf ultrasound switches [69], [70]. However, it also includes P-type DMOS transistors, $M_7$ and $M_8$, each

with a Zener diode for negative HV pulse protection. All diodes in this design are HV Schottky diodes except for $D_5$ and $D_6$, which are protection Zener diodes. The two paths of the diode-bridge are symmetrical for balancing the current. The switch requires 2 control signals, one of which is *TX_EN* that goes from 0 V to 5 V during Tx HV pulse generation, and the other one, $I_{P3}$, is the same control signal that is also used in the supply-inverted pulser in Figure 21.

To turn off the Tx/Rx switch to block the HV bipolar pulse, *TX_EN*, which is at 5 V, turns off $M_9$, which in turn shuts down the Tx/Rx switch. During this period, all transistors are off, and the input side of the Tx/Rx switch does not load the supply-inverted pulser. The power down period can be divided into two conditions, when the input is a negative HV pulse and when it is a positive HV pulse. During the negative HV pulse, $I_{P3}$ = 0 V, which turns $M_7$ off, while $D_6$ keeps it in the safe operating region. HV Schottky diodes, $D_4$ and $D_5$, can divide 45 V of total reverse voltage between them, resulting in each diode having reverse voltage well below its breakdown limit. It should be noted that without $M_7$, the negative pulse would turn on $D_7$, and affect the output HV pulse by lowering the impedance. During the positive HV pulse, $I_{P3}$ = 40 V, which keeps $M_7$ in the safe operating region by limiting $V_{SG}$ of $M_7$ to be less than 5 V. $D_4$ and $D_5$ pass the positive HV pulse to $R_1$ to reach $HV_{DD}$ - ($V_{D4}$ + $V_{D5}$), where ($V_{D4}$ + $V_{D5}$) is the forward voltage drop across $D_4$ and $D_5$. $D_8$ and $D_9$ can divide 45 V of total reverse voltage between them, resulting in almost 0 V at the output of the Tx/Rx switch. Figure 24 shows post-layout simulation of the Tx/Rx switch operation, showing that 86.2 $V_{pp}$ of bipolar pulse at the

input of the switch is blocked and limited to only 0.8 V at the switch output during Tx period.

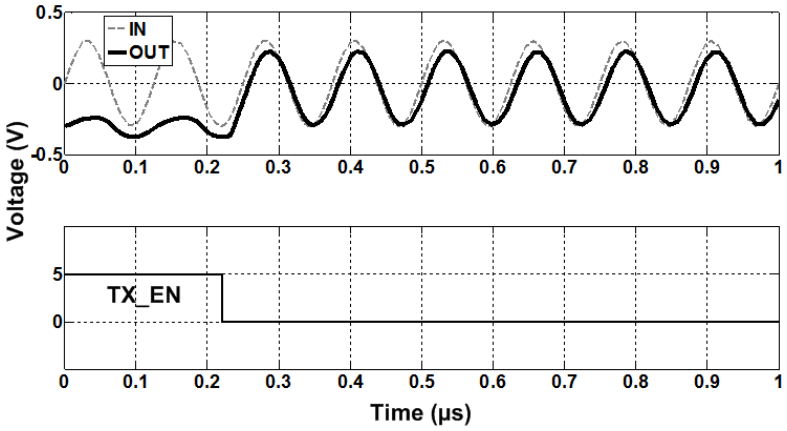



**Figure 25.** Simulation results of the Tx/Rx switch with 8 MHz of sinusoidal input. The load condition of the output node is 5 pF.

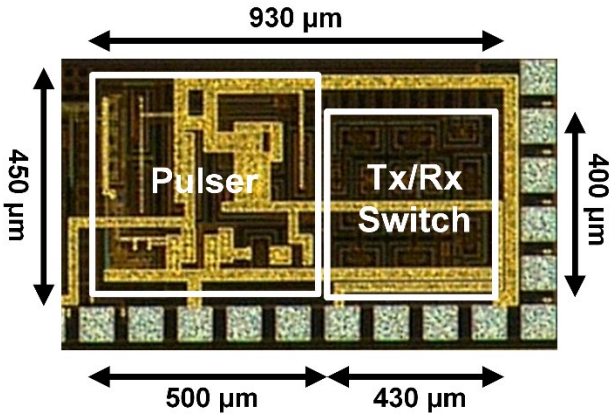



**Figure 26.** Microphotograph of the proposed supply-inverted pulser and Tx/Rx switch.

To turn on the Tx/Rx switch to pass through the received echo signal, *TX_EN* is pulled down to turn on $M_9$. At this moment, the external *C* would not affect the input loading of the Rx path, because $M_1$ and $M_2$ are turned off, floating one side of *C*. We

designed the Tx/Rx switch assuming that a high input impedance voltage amplifier stage follows this circuit [71], with the load condition of 5 pF, including the interconnection and amplifier input impedance. The transistor sizes of $M_6$ and $M_9$ are selected considering the static current of 288 $\mu$A during Rx period, layout size, and ON-resistance of the Tx/Rx switch. Depending on the type of amplifier, such as resistive feedback or capacitive feedback (low input impedance stage), the optimal size of transistors could be different. Figure 25 shows simulation result of the Tx/Rx switch with 0.6 $V_{pp}$ sinusoidal input at 8 MHz, achieving -0.8 dB of insertion loss at 8 MHz.

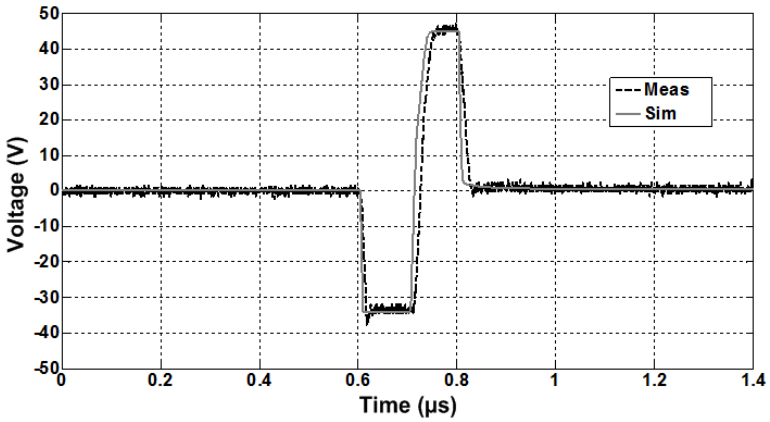



**Figure 27.** Measured and simulated supply-inverted output pulse along with three input control signals. $C$ = 30 pF, equivalent $C_{CMUT}$ = 8 pF.

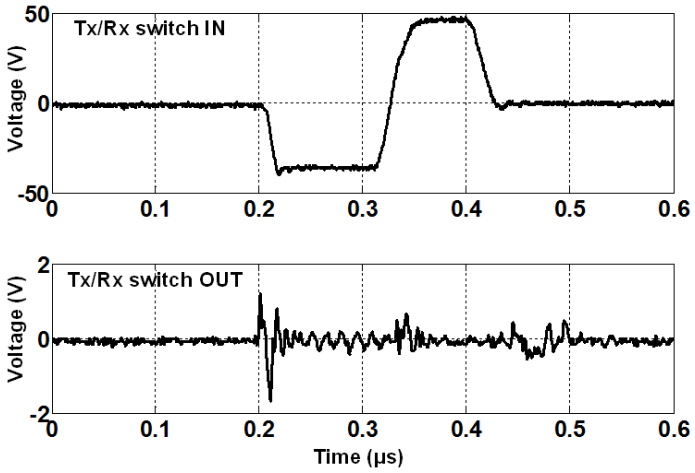



**Figure 28.** Measured Tx/Rx switch input and output during supply-inverted pulse firing period. $C$ = 30 pF and equivalent $C_{CMUT}$ = 8 pF.

The proposed pulser and Tx/Rx switch were fabricated using a 0.18-$\mu$m 60 V power management 4-metal 1-poly HV-CMOS process, a micrograph of which is shown in Figure 26. The occupied core area of the supply-inverted pulser and Tx/Rx switch are 0.225 mm$^2$ and 0.172 mm$^2$ respectively. The chip is wire-bonded in a QFN package and mounted on a PCB along with the off-chip surface mount capacitor, $C$. Figure 27 compares measurement and simulation of the supply-inverted pulser output with $C$ = 30 pF, and $C_{CMUT}$ = 8 pF. With $HV_{DD}$ = 45 V, the output shows -34.6 V negative and 79.6 V peak-to-peak voltages, and slew rates of -3.11 V/ns, 2.18 V/ns, and -2.02 V/ns during the first fall time, rise time, and second fall time, respectively. Measurements from over 10 chips have shown consistent results with $V_{out}$ (mean±std) = 79.03 ± 1.19 $V_{pp}$, demonstrating the reliability of this HV pulser. The good agreement between simulation and measurements, lead us to extrapolate ~85 $V_{pp}$ of output pulse with 2 pF of CMUT loading.

The Tx/Rx switch was also tested together with the supply-inverted pulser. Figure 28 shows that the switch does not noticeably affect the output of the supply-inverted pulser

during firing, and the HV signal is blocked with only 1.6 V of feedthrough. In this prototype, the Tx/Rx switch is placed close to the pulser as shown in the Figure 26 layout, and the HV pulse affects the Tx/Rx switch output though the substrate, creating the spikes shown in Figure 28 during HV pulser transitions. This can be reduced by placing these blocks further from one another and adding substrate contacts or shielding between the supply-inverted pulser and the Tx/Rx switch. The overall performance of Tx/Rx switch is benchmarked against prior work in Table 3.

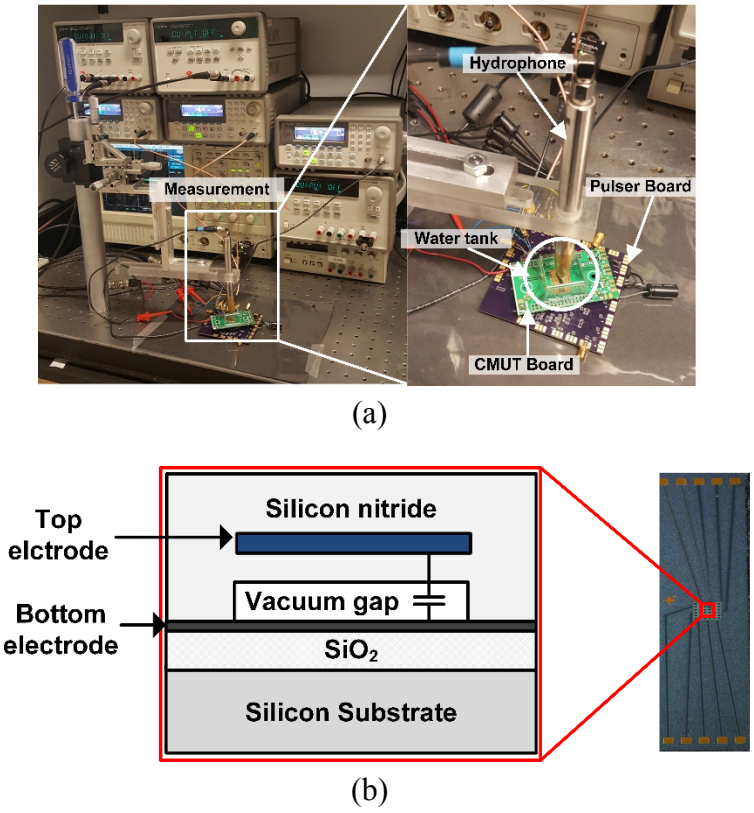



**Figure 29.** (a) Experimental setup with CMUT array board and pulser board for acoustic measurements. (b) Cross section view of CMUT layers and layout of the CMUT array which one element consists of 4 membranes.

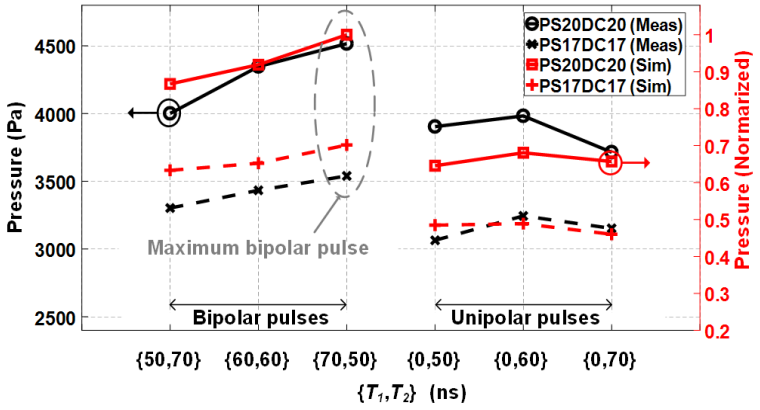
Transmitter acoustic pressure with an actual CMUT load was also measured using a setup shown in Figure 29. The CMUT used in this experiment was designed for an 8 MHz center frequency and occupied a 100 × 100 $\mu m^2$ area on silicon. The element consisted of a 2 × 2 array of four 45-$\mu$m wide square membranes, creating a 2 pF element, 1.8 pF of which is the parasitic capacitance due to bond pads. The fabrication was part of a larger 2-D ICE imaging array, fabricated using a low temperature CMOS compatible process. The CMUT array, mounted on a separate PCB and made water resistant by a 3 $\mu$m layer of Parylene-C coating, was connected to the larger pulser board via header pins. The off-chip capacitor, $C$ = 30 pF, was selected to obtain maximum output swing.

**Table 3. Benchmarking of the proposed Tx/Rx switch performance.**

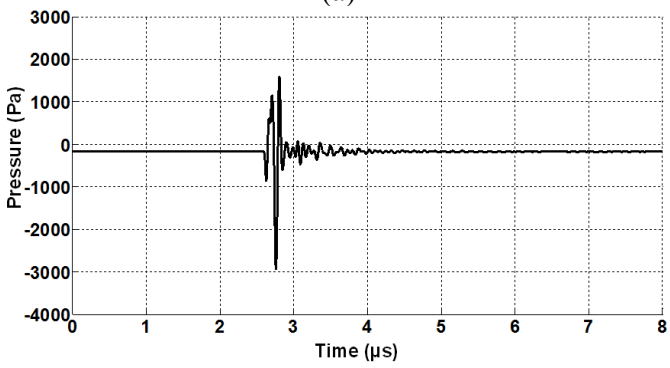
| **Parameter** | **This work** | **[68]** | **[69]** | **[72]** |
|---|---|---|---|---|
| Supply voltage (V) | ±5 | ±25 | ±5 | ±25 |
| Static power (mW) | 3 | 0 | 90-560 | 1 |
| Off-isolation (dB) | -28 | -53 | -40 | -90 |
| Limit range (V) | ±45 | ±25 | ±100 | ±25 |
| Number of control signals | 2 | 6 | 3 | 6 |
| Technology ($\mu$m) | 0.18 | 0.18 | - | 0.35 |

The CMUT array was submerged in a water tank, while a hydrophone (HGL-0085, Onda Corp) was positioned right above the CMUT array, 5.6 mm from its surface, to measure the Tx acoustic pressure. Different pulse shapes were generated to evaluate the

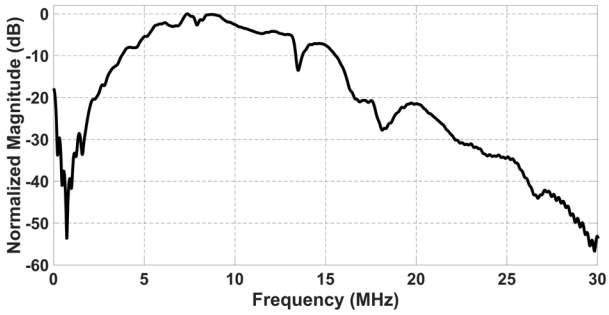
impact of the bipolar pulse waveform on the Tx output pressure. The pulse shape is defined by $\{T_1, T_2\}$, as shown in Figure 22. Note that when $\{0, T_2\}$ is applied, a positive unipolar pulse is generated. The bottom electrode of CMUT is connected to DC bias, $V_{DC}$, as shown in Fig. 2a. While using the same CMUT for Tx/Rx operation, a $V_{DC}$ needs to be applied across the CMUT for Rx operation with high sensitivity. $V_{DC}$ of the CMUT was changed from 17 V to 20 V, while $HV_{DD}$ was changed from 17 V to 20 V because the breakdown voltage of the CMUT in these experiments was limited to 40 V. The maximum peak-to-peak pressure of 4517 Pa was measured with {70 ns, 50 ns} of bipolar pulse shape, $HV_{DD}$ = 20 V, and $V_{DC}$ = 20 V (peak- to-peak pulse was ~40 V). Bipolar pulses show larger acoustic pressure compared to positive unipolar pulses, as shown in Figure 30(a), because during the first negative pulse, the potential difference on the CMUT is increased and the gap is further reduced for 70 ns. After the membrane passes through the minimum gap, the positive pulse cancels the DC bias across CMUT and completely releases the membrane for maximum upward gap swing. The unipolar pulse only releases the membrane from fixed gap, which is determined by $V_{DC}$, and its upward motion is also resisted by the DC bias. Therefore, a bipolar pulse is expected to generate higher peak pressure. The timing between pulling ($T_1$) and releasing ($T_2$) the membrane would also affect the peak pressure. In this measurement, three types of bipolar pulses and three types of unipolar pulses were measured to find the maximum pressure condition.




(a)




(b)




(c)

**Figure 30.** (a) Transmitted peak-to-peak acoustic pressure measurement and simulation with different CMUT bias, pulse shape and supply voltages. (b) Measured transmitted pressure with $T_1$ = 70 ns, $T_2$ = 50 ns, $HV_{DD}$ = 20 V, and CMUT bias = 20 V. (c) Frequency spectrum of the transmitted pressure signal shown in (b).

Figure 30(b) and Figure 30(c) show the time domain transmit signal and its spectrum for the case of maximum pressure, showing a center frequency of 7.8 MHz with

-3 dB bandwidth of 4.5 MHz. Figure 30(a) also shows the comparison between simulation and measurements, where the simulations are performed using a large signal CMUT model. The comparison with normalized pressures from simulations show good agreement in terms of trends and maxima as a function of pulse parameters for both unipolar and bipolar pulses at different bias voltages. Most of the mismatch comes from the dielectric charging effect in CMUT that degrades the transduction efficiency as the induced polarization reduces the effective bias across the CMUT. In our future work, we will investigate pulse optimization with co-design of the pulser and large signal CMUT model. Table 4 summarizes specification of the proposed supply-inverted pulser and compares it with previous works. Using positive HV supplies only, the proposed pulser can successfully generate a bipolar pulse above the process limit. Another advantage of this pulser is that without negative HV supply, it can generate a bipolar pulse with a peak-to-peak value surpassing the maximum operating voltage level (60 V in this case) imposed by the process. Therefore, this pulse was able to generate larger acoustic pressure from the CMUT than conventional pulsers that generate a pulse within the supply voltage range.

**Table 4. Benchmarking of the proposed pulser performance.**

| Parameter | This work | [47] | [58] | [73] | [65] |
|---|---|---|---|---|---|
| Input voltage (V) | 1.8 | 3.3 | 5 | 3.3 | 1.8 |
| Output voltage (V) | (-)34.6 - 45 | 0 - 30 | 0 - 85 | 0 - 60 | 0 - 12.8 |
| Supply voltage (V) | 45 | 30 | 45 | 60 | 12.8 |
| Frequency (MHz) | 8.33 | 5 | 8.33 | 1.38 | 1.25 |
| Rise/fall time (ns) | 36/11,23 | 30 | 26,16/18 | 68/68 | 40/50 |
| Power (mW) | 35.7 | 52.4 | 48.6 | 98.1 | |
| Power (mA) Dynamic * | 170 | - | 150 | - | 19.9 |
| Chip area ($mm^2$) | 0.225 | - | 0.2 | 0.08 | 0.022 |
| Output load (pF) | 2 | 40 | 2 | 18 | 15 |
| Bipolar pulse | Y | N | N | N | N |
| Technology ($\mu$m) | 0.18 | 0.18 | 0.18 | 0.35 | 0.18 |

* Simulation results

The multi-level pulsing circuit has advantages in terms of better power efficiency when driving CMUTs. However, it requires several supply voltages or DC-DC converters with large capacitors. Since the capacitors required for DC-DC converters are often quite large, using off-chip components would be inevitable. A potential advantage of the proposed pulser is that, to generate a bipolar pulse, it requires a capacitor that, while it is an order of magnitude larger than $C_{CMUT}$, can be implemented during microfabrication underneath the CMUT. This is schematically shown in Figure 31, where a CMUT element is built over a fixed capacitor, *C,* with approximately the same area, and connected to the

CMOS electronics using CMUT-on-CMOS technology. While the CMUT capacitor, $C_{CMUT}$, has a vacuum gap, $C$ is formed by filling a similar gap with a high-K dielectric, such as hafnium dioxide with $\varepsilon_r = 16$. With non-collapsed CMUT operation, one can easily satisfy the required $C >> C_{CMUT}$ condition in this approach, considering that in CMUT-on-CMOS implementation the parasitic capacitance will be minimized. For instance, a breakdown voltage of 60 V can be achieved with hafnium dioxide with a typical gap/dielectric thickness of 150 nm. This approach would enable fabrication of a high voltage capacitor in the CMUT layer for compact ultrasound analog front end design in imaging applications.

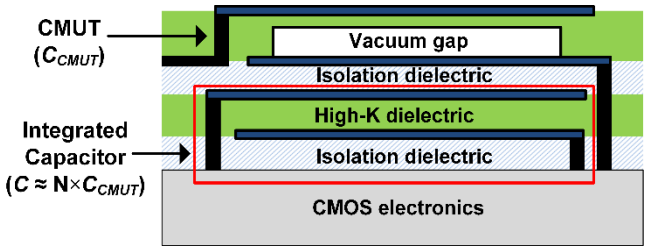



**Figure 31.** Schematic cross section view of a CMUT-on-CMOS device with integrated co-microfabricated capacitance, $C$. Lower relative permittivity dielectric layers (SiNi, $SiO_2$) are used for isolation, and the high K-dielectric has a relative permittivity of $\varepsilon_r = N$. Black lines are metal connections to the CMOS electronics.

In this section, an integrated supply-inverting HV pulser with Tx/Rx switch is presented in a 0.18-$\mu$m 60 V HV-CMOS process to interface with CMUTs in ultrasound systems. The presented circuit overcomes process limitation by adopting HV protection and bootstrap techniques. The supply-inverted pulser generates 79.6 V of peak-to-peak voltage swing using 45 V of positive supply with 8 pF of equivalent CMUT loading and 30 pF of external capacitance. A bipolar pulse was successfully applied to a CMUT array

element and optimized for maximum acoustic pressure. The output followed predictions by a large signal CMUT model, paving the way for large signal simulation-based CMUT-pulser optimization. The proposed Tx/Rx switch effectively blocks the HV swing of the supply-inverted pulser without degrading the performance of the proposed pulser. While the prototype pulser and Tx/Rx switch measurements were conducted with an off-chip capacitor, the technology exists to allow this capacitor to be integrated with the CMUT, using high-K dielectric layers, during CMUT fabrication.

# CHAPTER 3. SINGLE-CHIP REDUCED WIRE CATHETER SYSTEM

We have developed a single-chip reduced wire catheter system, which achieved a significant cable reduction by adopting both of the Tx and Rx cable reduction schemes in proposed ASIC. This proposed ASIC is designed for driving a 64 channel piezo-transducer array, which adopts 8:1 TDM Analog Rx with direct digital de-multiplexing (DDD) [74], and Tx-beamformer, which can be programmed with a single low voltage differential signaling (LVDS) data line for loading whole channels' beamforming profile and controlling Rx gain as well. The ASIC fits in 10 F catheter size, which occupies 2.6×11mm2. The proposed system reduces the number of wires from more than 64 to 22. The 64 channel received raw echo signals are reduced to 8 through TDM, and sent to analog-to-digital converters (ADC) in the backend system through 3 m long of Ethernet cables, where DDD is performed in field-programmable gate array (FPGA) for real-time image processing in the digital domain.

## 3.1 System Architecture

To reduce the number of wires, the proposed system integrates ASIC on the catheter tip to implement Tx-beamformer and Rx TDM circuits in a single chip. Figure 32 shows the simplified block diagram of the proposed ICE catheter system. HV pulsers are implemented after Tx beamformer to generate 60 Vpp pulse to drive comparable large sized 1-D piezo-transducer array based on the beamforming profile of each channel. Tx/Rx

switch is located between pulser and Rx circuits to protect low voltage (LV) devices during transmitting operation. Variable gain LNA compensates the attenuation of reflected echo signal by adjusting gain which is called TGC.

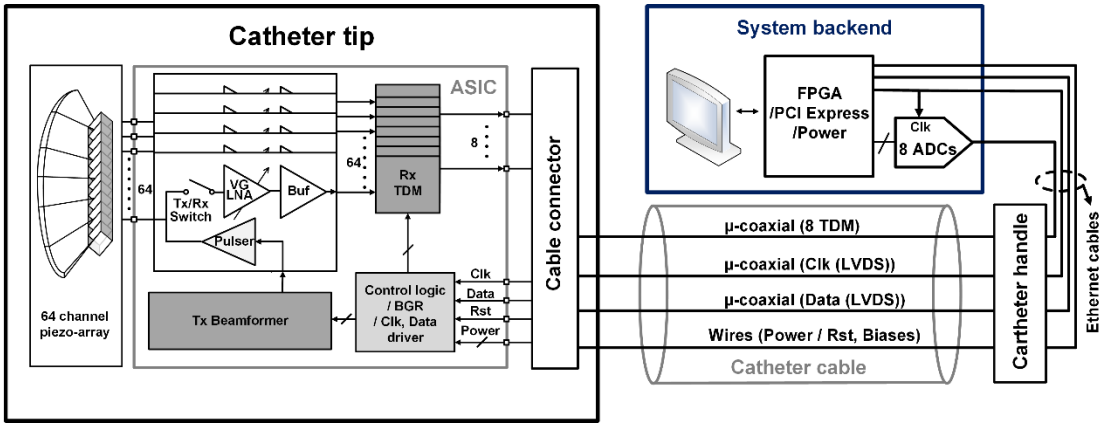



**Figure 32.** Simplified block diagram of the proposed ICE catheter system which includes backend system.

The 8 pairs of 8:1 TDM circuitry reduces the output signals from 64 to 8, which the high frequency (HF) buffers drive output signals via Ethernet cables to the backend system. The ADC in the backend system samples the corresponding channel in the right time. The key idea of TDM in this system is the clock synchronization between the ADC and multiplexer in ASIC, which the details will be described in the next Section. In this system, 64 channel of piezo-array elements are used to interface with proposed ASIC for this proof-of-concept implementation. This array can be directly mounted on top of the front-end ASIC using flip-chip bonding or PZT-on-CMOS integration for future implementation [23]. Also the proposed ASIC is designed to be compatible with CMUT-on-CMOS application, which the array is fabricated using a low temperature process on top of CMOS wafer.

The catheter cable consists of μ-coax cables (~48-AWG), which can be used to deliver 200 MHz of clock, data, and TDM output signals and wires to deliver power lines, biases and control signals. After the catheter cable, the TDM signals are amplified via catheter handle to be sent across the long Ethernet cables to ADCs in backend system, where DDD is performed in FPGA for advanced imaging processing in the digital domain.

The backend system consists of the custom ADC board to support 8 TDM signals, FPGA board from Altera, power supply module which employs filters, AC-DC converters, and DC-DC converters, and finally PCI express card which delivers data from FPGA to personal computer via optical fiber. In this paper, the main scope of proposed system is ASIC design, that the next Sections describes the circuit level implementation and details of operation for each blocks of ASIC.

## 3.2 Transmitter Beamformer and Pulser

The proposed Tx-beamformer requires a single LVDS data line to load 64 channels of beamforming profile. It can create a maximum delay of 10.235 μs with a resolution of 5 ns, using an 11-bit global counter. This beamformer is designed to generate different pulse-width of each channel to enable pulse-width apodization, which improves ultrasound image quality by suppressing the side lobe effects [75]. Also, it can generate multiple number of pulses up to 8, which has narrower band frequency response than single pulse, to find Doppler shift frequency easily. It also can change the pulse repetition frequency during Doppler mode operation.

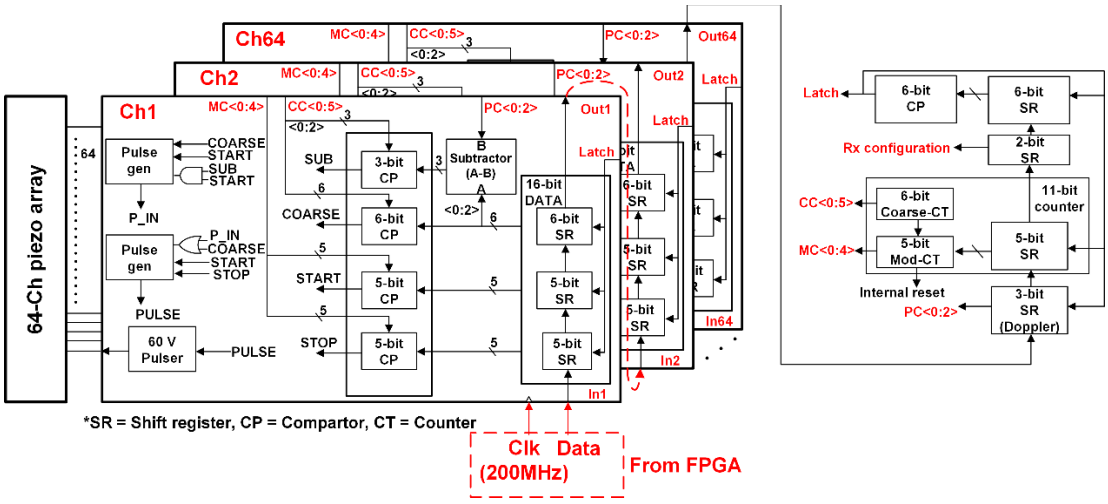



**Figure 33.** Detailed block diagram of the Tx-beamformer.

Figure 33 shows the detailed block diagram of transmit beamformer. In global control logic block, 11-bit global counter consists of 6-bit course counter (CC) and 5-bit mod counter (MC). During the data loading sequence, the initial counting to 0000002 to find the coarse delay of each channel, while 5-bit MC can be programmed to set the exact start time, width of a pulse, and number of pulses for each channel. Each of 64 channels has 16-bit serial-in parallel-out (SIPO) shift register that stores delay and pulse width information respectively. Top 6-bit shift register is used for checking proper data loading by comparing the value with 1111112. Once the data is loaded properly, the latch signal locks the whole shift registers that the counters start to count for pulse generation. A 2-bit shift register is used for Rx gain control configuration, and the last 3-bit shift register stores the number of firing pulses for Doppler operation. Each channel has a 3-bit subtractor which is used to keep track of how many pulses are fired during each transmitting cycle. Each channel has 19-bit comparator that can calculate exact beamforming profile to deliver LV pulses to the input of pulser.

To program all the delay profile for 64 channels, each programming cycle requires a 1040-bit data packet (64×16+2+3+5+6), which corresponds to 5.2 μs. Before programming the Tx-beamformer, all shift registers are reset to set initial values, following which the data packet is generated and sent from an FPGA in backend system through the high speed Ethernet cables.

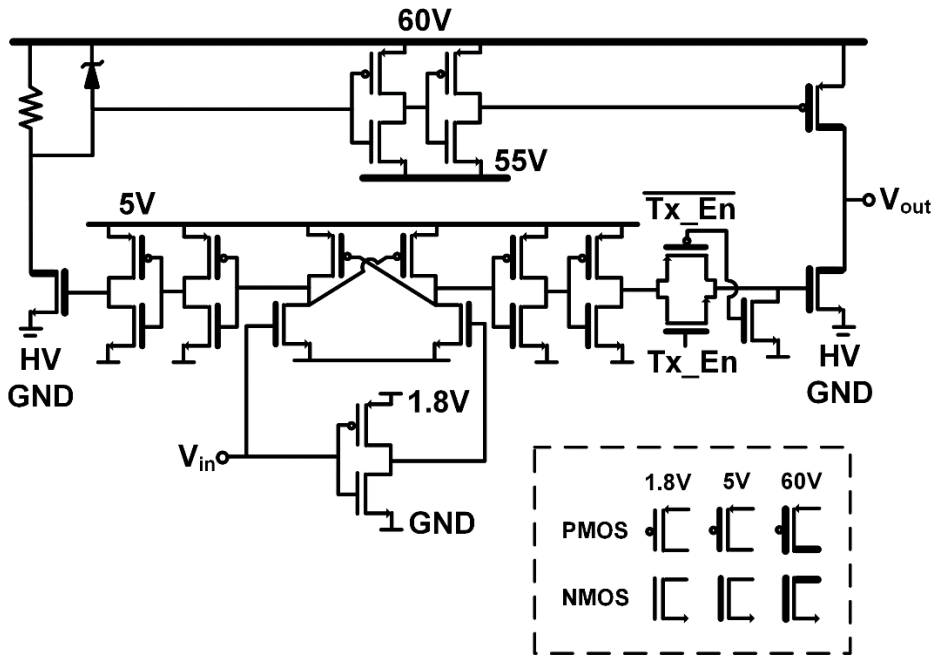



**Figure 34.** Schematics of proposed 60 V pulser.

Ultrasound pulse generator, aka pulser, is one of the key building blocks of ultrasound imaging systems, which drives ultrasound transducers such as piezoelectric material or CMUT with HV output swing to create an ultrasound pressure pulse towards the tissues. Recent research shows several pulse-level shifting techniques to overcome limited supply voltage such as voltage doubler or multilevel pulse generator in ultrasound application [47], [58]. However, these approach require multiple number of control signals

and occupies comparable area that integrating in the ICE catheter with many numbers of channel is challenging.

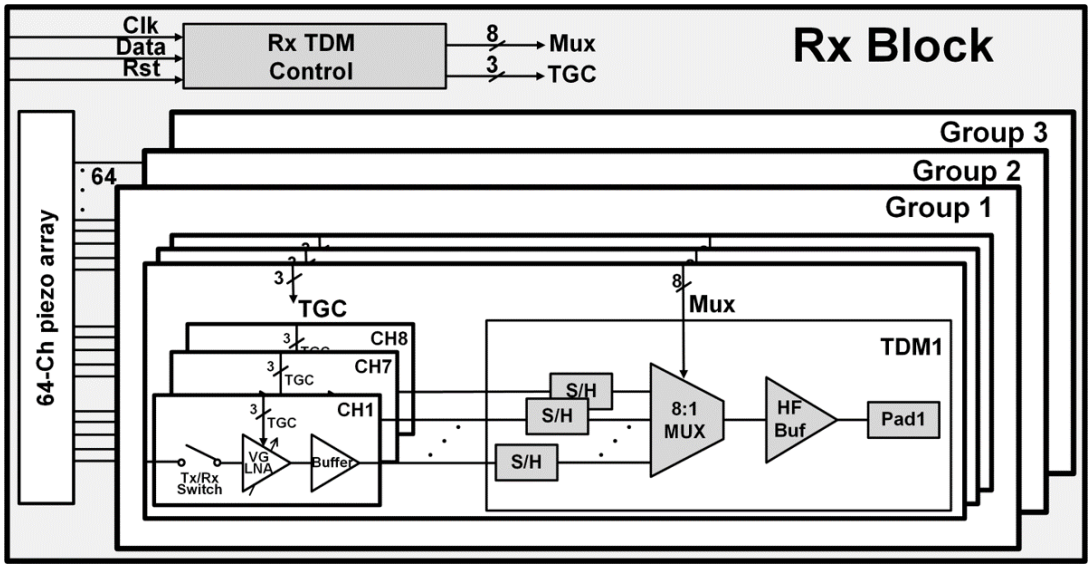



**Figure 35.** Simplified receiver TDM circuitry.

In this proposed system, for design simplicity, simple digital pulser is implemented using 60 V double-diffused metal oxide semiconductor (DMOS) transistors as shown in Figure 34. The input of pulser is generated from transmit beamformer with 1.8 V supply. The pulser level-shift this signal to 5 V to have enough input swing for DMOS transistors, and finally drive the output node with 60 V pulse. It is crucial to ensure that all devices in the circuit are operated in their safe operating conditions, considering the fact that in this process, the drain-source junction breakdown and gate-oxide breakdown voltages are 60 V and 5 V, respectively. Considering that P-type DMOS occupies quite big area, resistor is selected in level-shifter stage with protection Zener diode. This level shifter is designed to limit the peak current to 5 mA from 60 V supply by adding 55 V supply and 5 V buffer

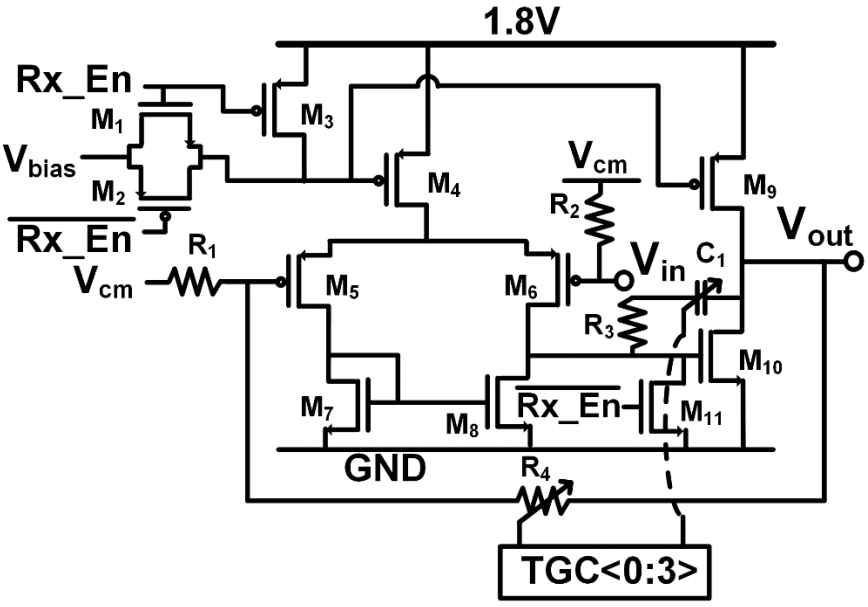
chain, avoiding voltage drop across 6.7 mm on-chip power routing. The pulser is designed to drive 15 pF of capacitive loading at 7 MHz with 60 V pulse, which is the equivalent capacitance of comparably large sized 1-D ICE piezo-array.

## 3.3 Receiver TDM Circuitry

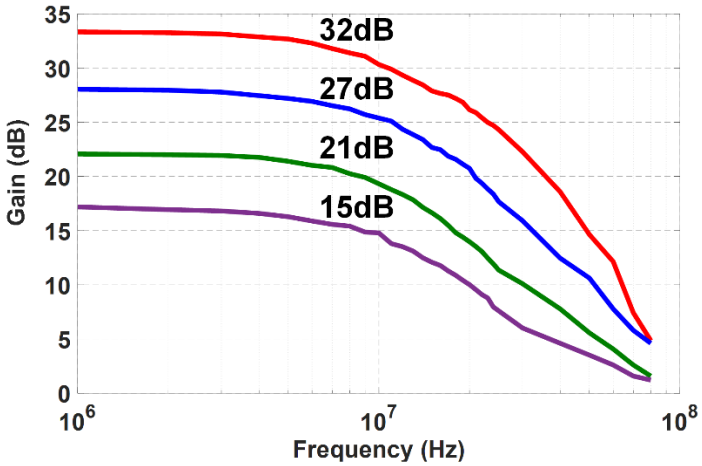
The simplified schematic of Rx AFE is shown in Figure 35. 64 channels of Rx circuitry consists of Tx/Rx switch, Variable gain LNA, buffer and TDM circuitry. The echo signal received from piezo-array elements have a dynamic range of 76 dB, and the gain of Rx circuitry is set to compensate the attenuation by 4 stages to meet the dynamic range of ADC in backend system. During transmitting mode, Tx/Rx switch protects LV circuits from HV pulses. Variable gain LNA amplifies the echo signal based on the traveling depth for compensation, buffer drives the amplified signal to TDM circuitry, and finally TDM circuitry samples and combines the output signals with 8:1 ratio to the backend system. The key blocks are described details as following paragraph.

Rx front-end topology is usually depend on the electrical impedance of ultrasound transducer type. The transimpedance amplifier (TIA) is a commonly used topology in CMUT application because the equivalent electrical model of CMUT has comparably high impedance [76]-[80]. For implementing AFE for piezo-array, LNA structure is preferred because of relatively low impedance nature of 1-D array piezo elements [23]. Considering the area efficiency which in this process, the required capacitor occupies larger area than resistor, and minimizing a low-frequency shift of the pulse-echo response, the resistive feedback LNA structure is selected for this system [81]. Also instead of implementing LNA

and time gain control (TGC) circuit separately, this system adopts variable gain LNA structure for system simplicity.




(a)




(b)

**Figure 36.** (a) Schematics of variable gain LNA, and (b) measured frequency response of variable gain LNA with different 4 gains.

Figure 36(a) shows the schematic of variable gain LNA structure. The gain is controlled by 4-bit TGC signal through data line, which is generated by FPGA from

backend system. Figure 36(b) shows the measured frequency response of different gain stages, which shows 15 dB, 21 dB, 27 dB, and 32 dB at center frequency of 7 MHz with 3 dB bandwidth of 11 MHz. The measured input referred noise at 7 MHz shows average less than 4.1 nV/√Hz. The Miller compensation leg capacitor of $C_1$ is also controlled by TGC signal to push the second pole of this 2-stage op-amp well beyond the closed-loop bandwidth to keep phase margin above 60º in every gain stages. Rx_EN signal and switch transistors ($M_1$, $M_2$, and $M_{11}$) are required for power saving mode during transmit data loading period.

TDM technique has been used in communication systems to reduce the number of output channels [35], [37]. This approach allows multiple channels to share the same cable by assigning corresponding time slot to each channel. Analog TDM requires a relatively simple design and less power because it needs an analog multiplexer and digital counting logic in addition to sample and hold circuits, which is suitable in compact ICE application. Also in this proposed system, by using DDD technique, ADC can sample TDM output signals using the same frequency with the TDM circuitry in the ASIC. This results in less data processing to increase efficiency in backend system.

The target center frequency of this research is around 7 MHz, and the fractional bandwidth is assumed as 80 % in case for CMUT application as well, which usually has broader bandwidth than piezo-array. It requires sampling rate more than 20 Msps considering the Nyquist requirement. In this system, the clock frequency is chosen as 200 MHz, resulting in 25 Msps for each channel of 8:1 TDM circuitry. Also for minimizing the

cross-talk level, high frequency (HF) buffer is designed to have more than 400 MHz bandwidth.

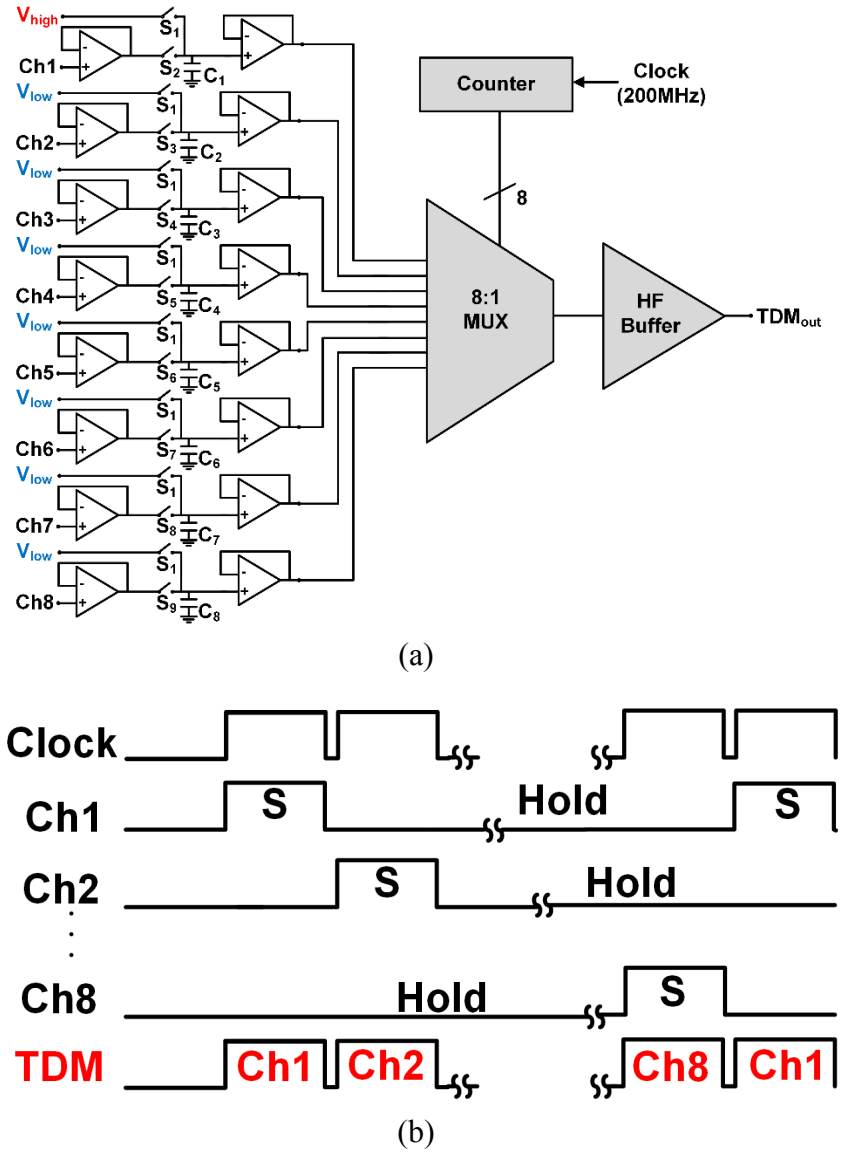



**Figure 37.** (a) Simplified block diagram of TDM block for 8 channels, and (b) TDM sampling clock diagram.

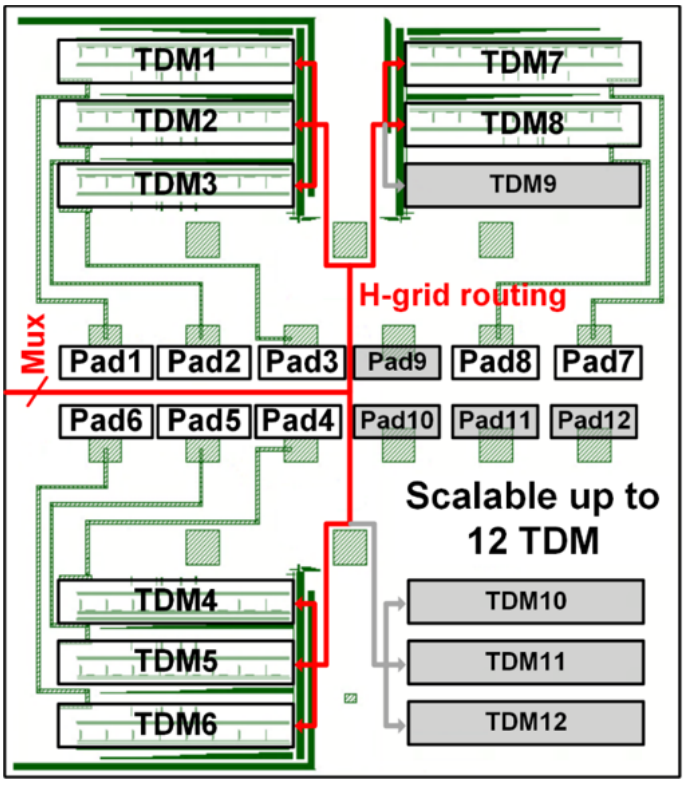



**Figure 38.** The symmetrical layout of the TDM block.

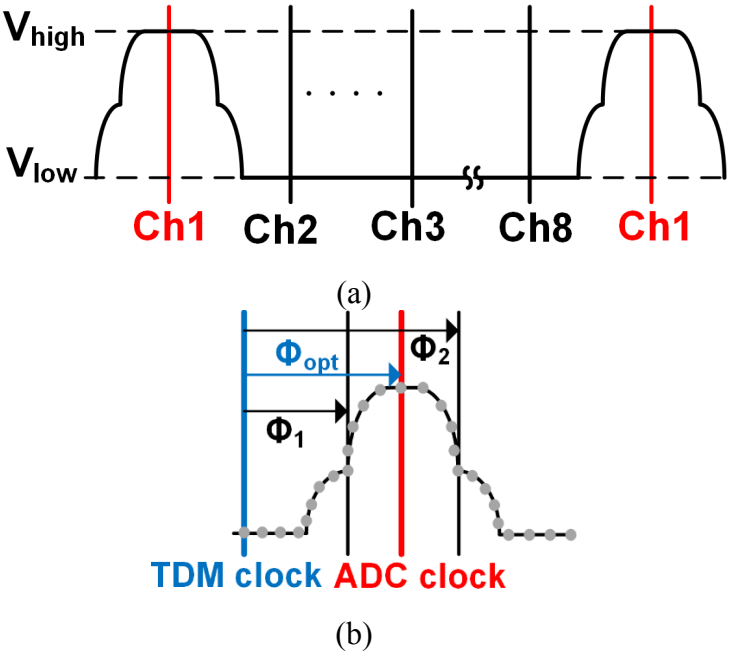



**Figure 39.** (a) Link training waveform of channel number synchronization, and (b) phase synchronization.

The TDM circuitry consists of 8 sets of TDM block, and each TDM block consists of 8 channels of sample and hold switches, link training switches, analog 8:1 multiplexer, high frequency buffer as shown in Figure 37(a). The counter logic generates sample clocks and the analog multiplexer selects signals for corresponding channel, which keeps track of which channel is to be connected, as shown in Figure 37(b). The 8 sets of TDM circuitry, which can be scalable up to 12 TDM system, was placed with symmetric layout, which reduces mismatch as shown in Figure 38. A critical part of the DDD is the clock synchronization between the TDM analog multiplexer in the ASIC and the ADC in the backend system with the same frequency. For this reason, the system requires two training sequences before TDM block starts working. One is channel number synchronization, and another is clock phase synchronization. These training sequences are called link training to ensure that the samples are correctly digitized in backend. During the link training process, firstly channel 1 is connected to a fixed voltage level of Vhigh while other channels are connected to another lower fixed voltage of Vlow, by adding another switch in parallel with the sample and hold switch for each channel as shown in Figure 37(a). During this operation, $S_1$ is connected and all the other switches from $S_2$ to $S_9$ are open that the corresponding timing of channel 1 can be detected during de-multiplexing in the backend system. By performing this, the timing of the first channel of each TDM block can be ensured that the order of channel timing can be figured out as shown Figure 39(a).

The clock phase synchronization is used to ensure that the ADC and TDM multiplexer clocks are correctly phase synchronized to compensate for the propagation delays in the cabling. This is important to guarantee that the ADC takes the samples when

the signal through the interconnection has stabilized rather than during switching transients. The TDM clock phase can be adjusted using a phase-locked loop (PLL) in the FPGA to determine the optimum phase shift, as shown in Figure 39(b). The phase of TDM clock is changed until finding the half maximum points of channel 1's amplitude such as Φ1 and Φ2. These two points show when the switching transients are occurring, so optimal phase shift should be the middle of these two points, which is Φopt. The HF buffer is designed using current feedback source degenerated push-pull type buffer with ~400 MHz bandwidth with 75 Ω of cable termination [82]. The simplified block diagram of proposed 8:1 TDM with DDD system is shown in Figure 40.

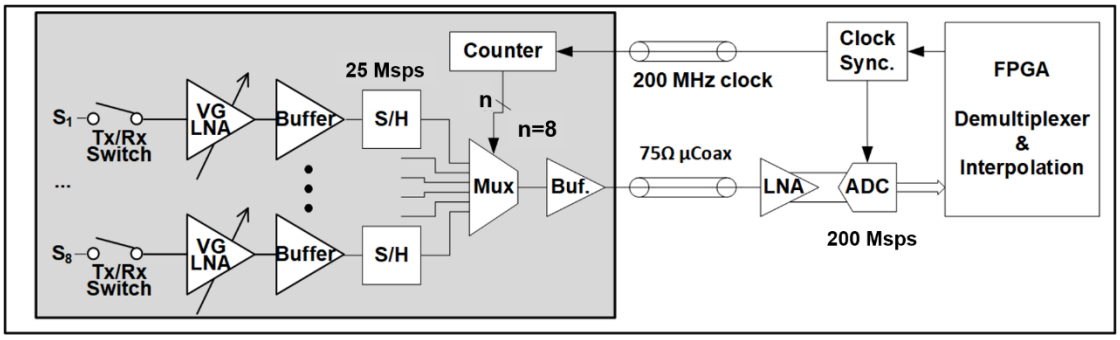



**Figure 40.** Simplified block diagram of TDM with DDD system.

### 3.4 Experimental Results

The ASIC is fabricated in 0.18-μm 60 V power management 4M1P HV-CMOS process. The ASIC consists of 64 channel analog front-end (pulser, Tx/Rx switch, LNA, and buffer), transmit beamformer, and symmetrically designed TDM which occupies 2.6×11 $mm^2$ as shown in Figure 41. It consumes 439 mW of averaging power for B-mode imaging using phased-array beamforming including HV power consumption. Figure 42

shows the timing diagram of the proposed system. The ASIC requires clock, reset, and data. Once the transmit data is loaded properly after link training from the TDM side, the transmit beamformer triggers pulsers to fire HV pulse based on the beamforming profile, and Rx circuits are receiving at the same time. TGC signal can be loaded through data line to control Rx gain. After receiving the whole echo signals, reset triggers all the system to have initial state, being ready to load another beamforming data.

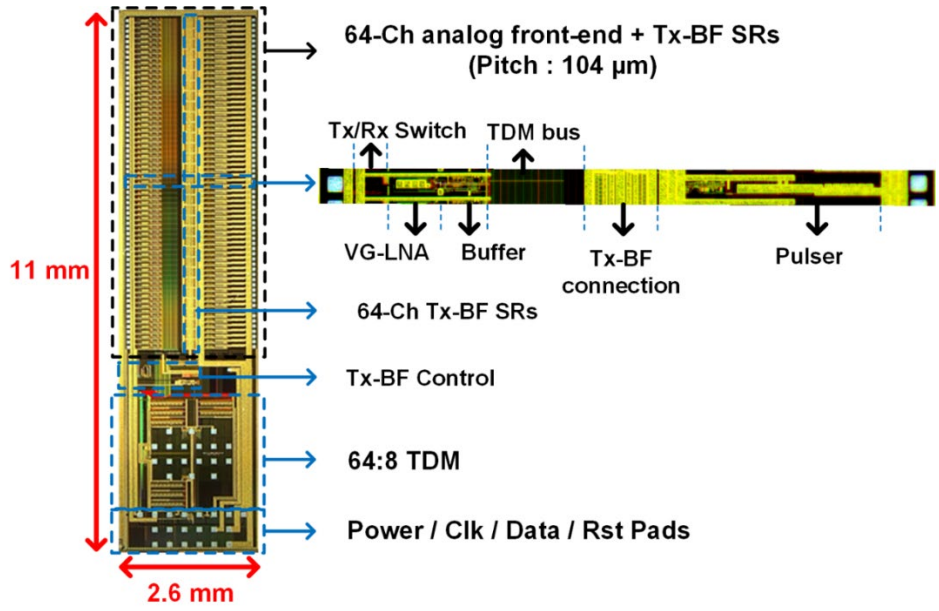



**Figure 41.** Microphotograph of 64 channel ICE ASIC.

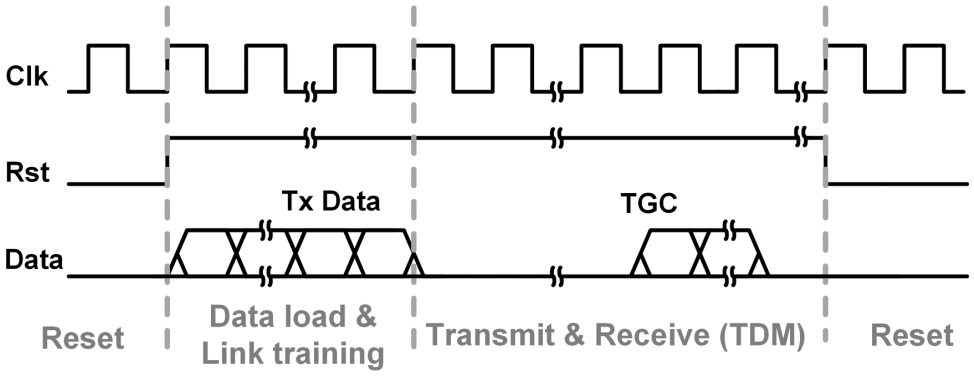
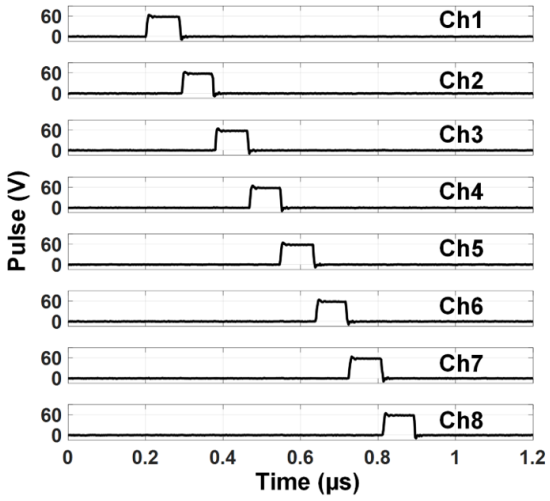


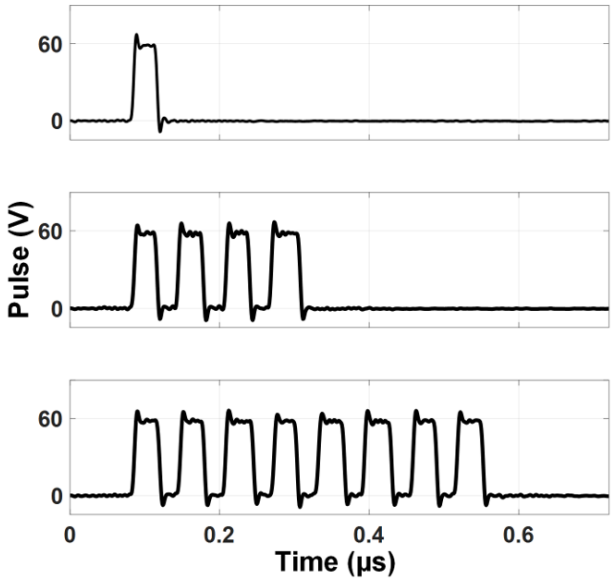

**Figure 42.** Timing diagram of the proposed system.

### *3.4.1 Electrical Characterization for Tx Circuitry*

To characterize the Tx-beamformer and HV pulser, the ASIC was tested with backend system. The FPGA generates beamforming profile of which each channel has the pulse width of 80 ns, and is delayed to 80 ns consecutively. The ASIC is wire-bonded to a custom printed circuit board (PCB) to probe the output of the pulsers with the effective loading of ~15 pF which is the equivalent capacitance of 1-D piezo-array. Figure 43(a) shows the measured pulse output from channel 1 to channel 8, which the pulser successfully generate 60 V pulse with rise and fall time of 6 ns, showing that it is good enough to drive 7 MHz pulse. The Tx-beamformer can generate multiple pulses up to 8 for Doppler operation, that the multiple pulses are generated to show functionality as shown in Figure 43(b).




(a)




(b)

**Figure 43.** (a) Measured pulser output from adjacent 8 channels, and (b) multiple consecutive pulse generation for Doppler imaging.

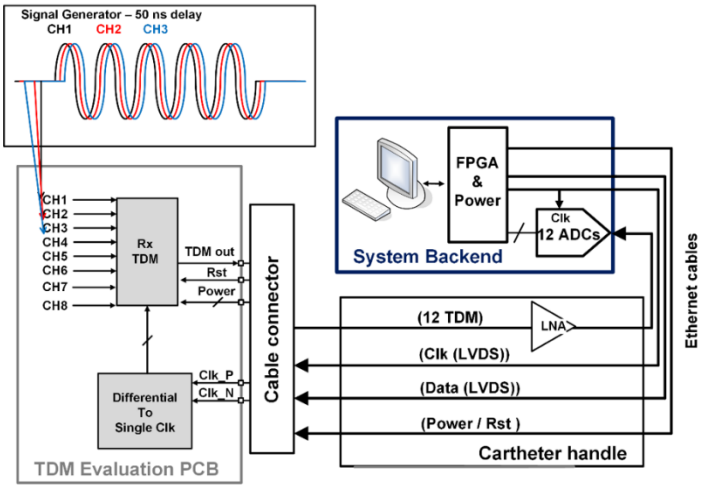



**Figure 44.** Simplified block diagram for testing TDM block with back-end system.

### *3.4.2 Electrical Characterization for Rx TDM*

The electrical characterization of the proposed Rx TDM system has been fully investigated with a separate test IC. The test IC is designed to evaluate 8 channels of TDM

block as shown in Figure 37 with the control block for link training. The custom PCB is designed to interface 8 input signals with external signal generators and TDM output signal is connected to one of the backend TDM input terminal as shown in Figure 44. The ADC samples the corresponding channel signals, then FPGA performs DDD and further digital processing for interpolation, decimation, phase correction and filtering to recover the original input data [74]. Channel 1, 2, and 3 are connected with the signal generators which generate 7 MHz sine waves with 50 ns delay, respectively. Figure 45 shows the comparison between the signal generator and TDM output signals after advanced digital processing, which shows good agreement. The mismatch between the TDM outputs and signal generator outputs from the first and the last burst is from effects of band pass filtering.

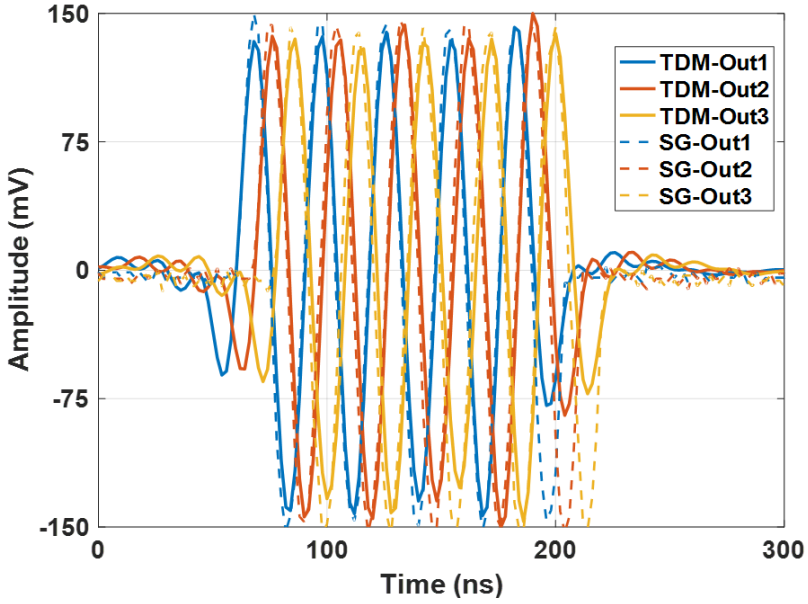



**Figure 45.** Simplified block diagram for testing TDM block with back-end system.

Also, for analyzing the crosstalk level of the TDM block, 7 MHz of sine wave is induced to channel 1, and the recovered whole TDM signals are analyzed using fast Fourier

transform (FFT), while other channels are connected to ground. Figure 46 shows that the maximum crosstalk level is -36.7 dB when compared to the channel 1, which is good enough in ICE application. It is noteworthy that this measurement of the crosstalk is between the signals of the same TDM block as a results of the multiplexing scheme. The crosstalk level between the TDM blocks was measured to be below -60 dB which is neglectable. Considering that this FFT was obtained with 1200 points with full bandwidth of 12.5 MHz, for real imaging bandwidth of 4 MHz, this results corresponds to effective number of bits (ENOB) of 8 bits.

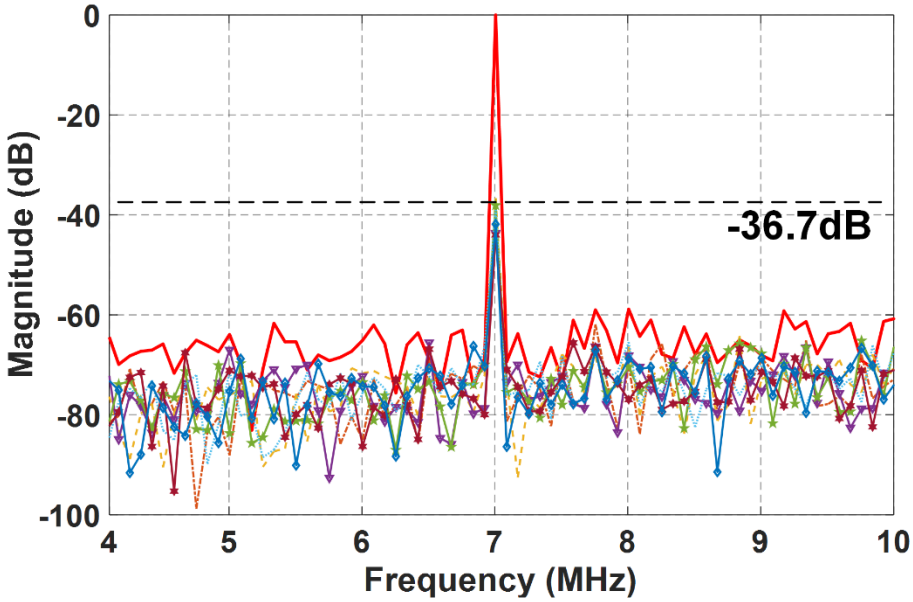



**Figure 46.** Crosstalk measurement of 8 channels of TDM circuitry.

The ideal Gaussian pulses with center frequency of 7 MHz and bandwidth of 40 % was induced to the full system input, since the real pulse echo signal would not look like just sinewave. Figure 47 shows three ideal Gaussian pulses which has 7 MHz of center frequency with 50 ns delay for each.

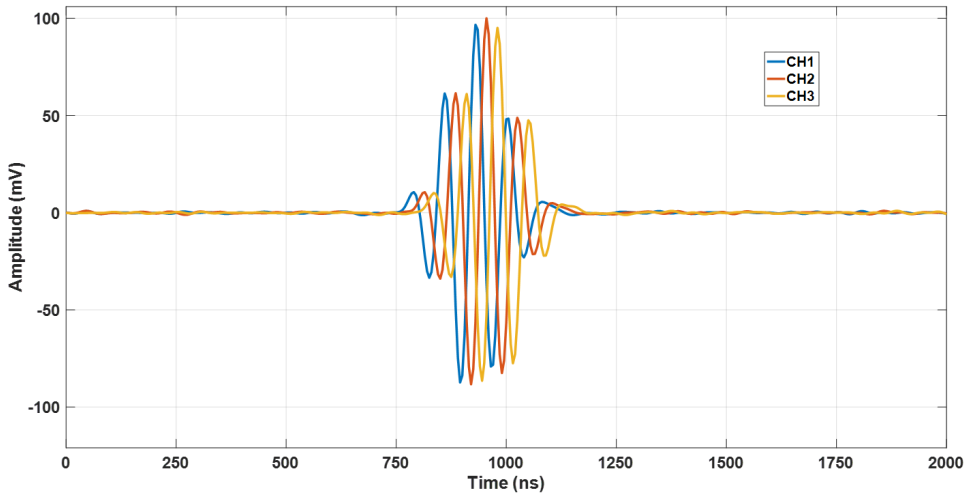



**Figure 47.** The measurement of three ideal Gaussian pulses from signal generator.

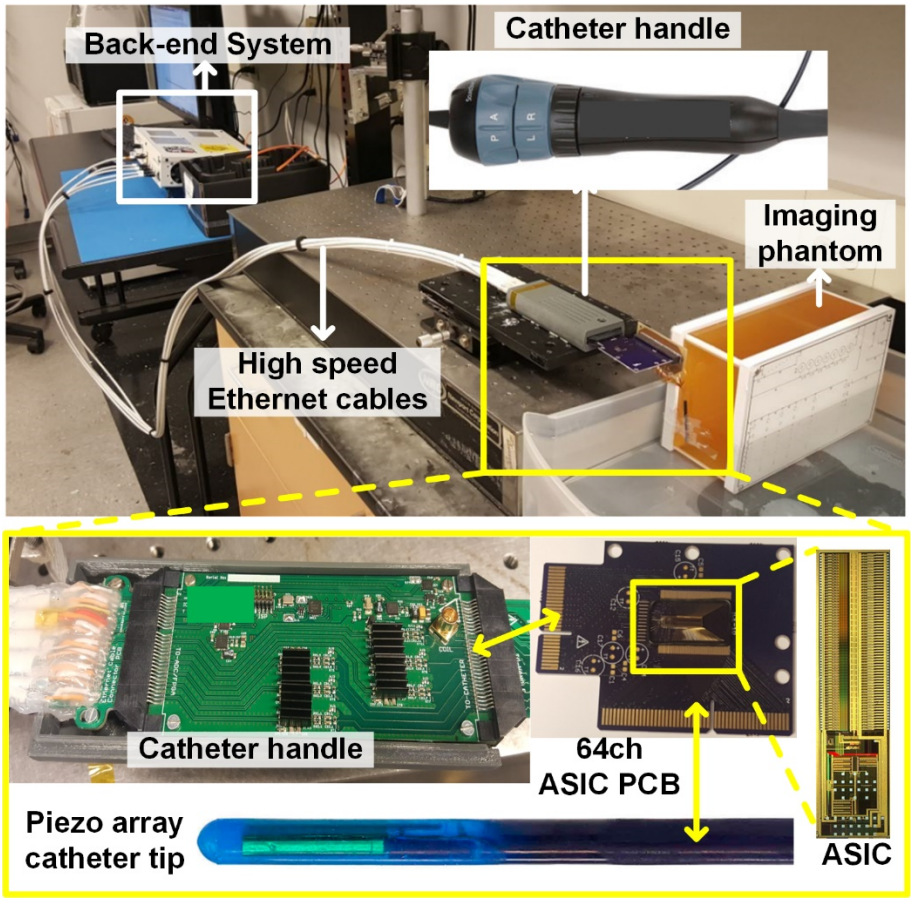
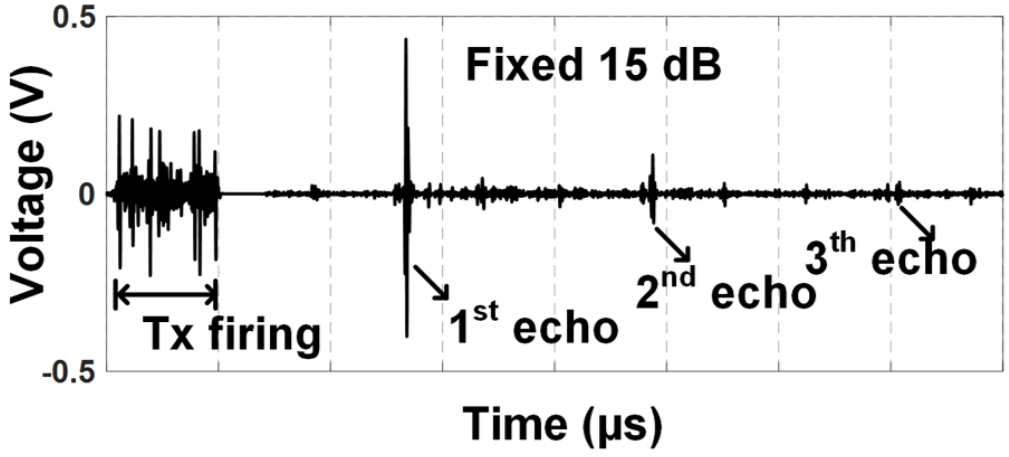


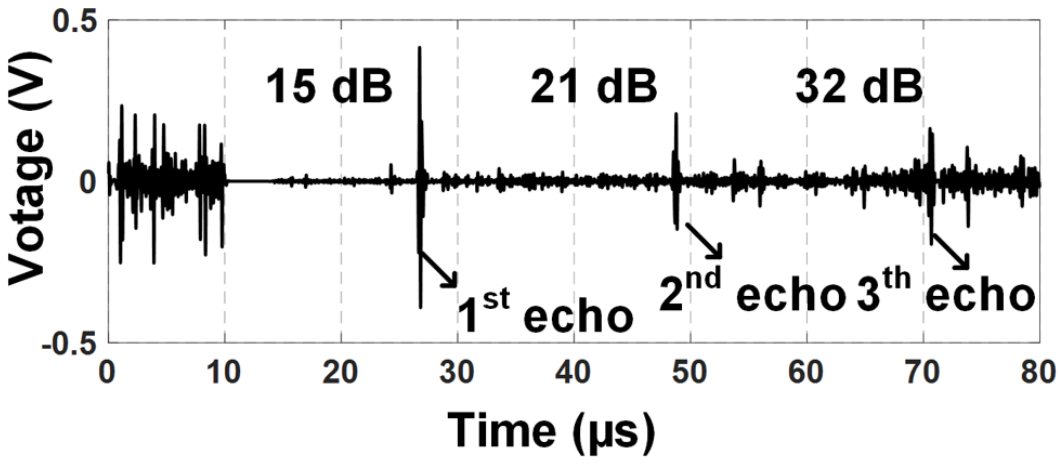

**Figure 48.** Ultrasound imaging measurement setup with piezo-array immersed in the water facing standard phantom.

### *3.4.3 Acoustic Measurement with Full System*

The proof-of-concept imaging experiments are performed by connecting the ASIC wire-bonded on a PCB, to a 64 channel piezo transducer array at the tip of an ICE catheter using flex cables as shown in Figure 48. The ASIC PCB is connected to catheter handle, which the TDM signals are amplified prior to passing through to the ADCs in the backend system via 3 m of Ethernet (Cat7A) cable to allow the system to theoretically be placed away from an MRI system. For future implementation, the piezo-array will be either flip-chip bonded to ASIC or CMUT-on-CMOS technique will be applied for compact design to fit in the catheter size. The piezo transducer array is immersed in the water tank facing the standard imaging phantom (N-365, Kyoto kagaku).




(a)




(b)

**Figure 49.** (a) Measured echoes reflected from a metal reflector at 1.6cm without TGC after TDM and DDD, and (b) with TGC control.

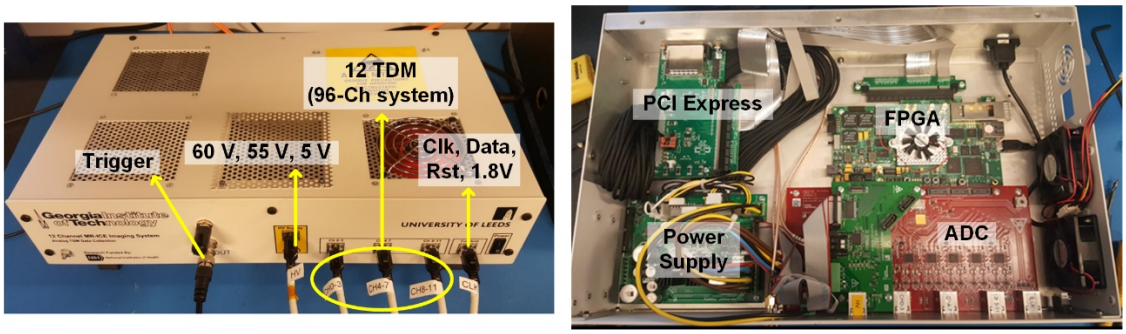
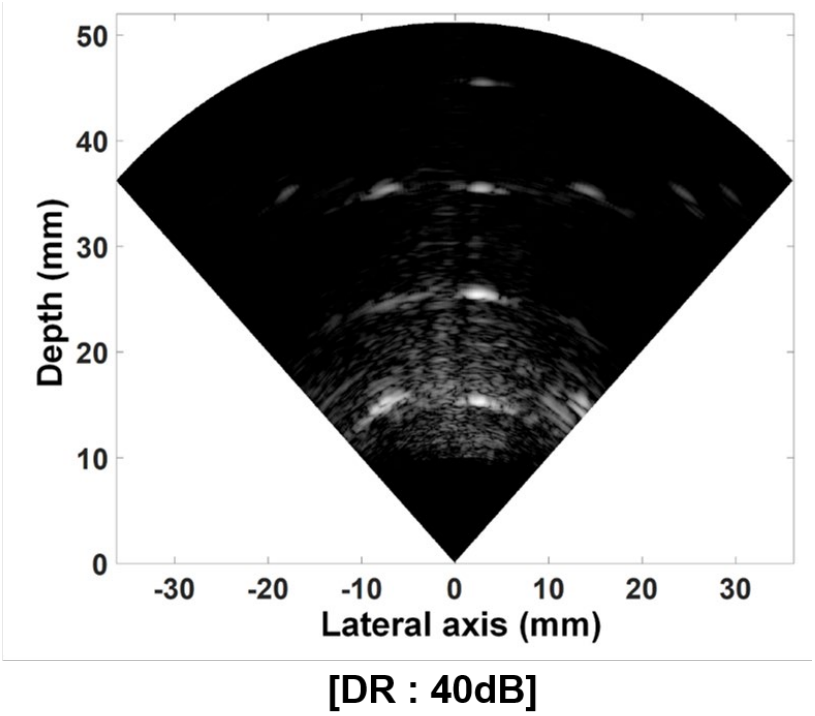


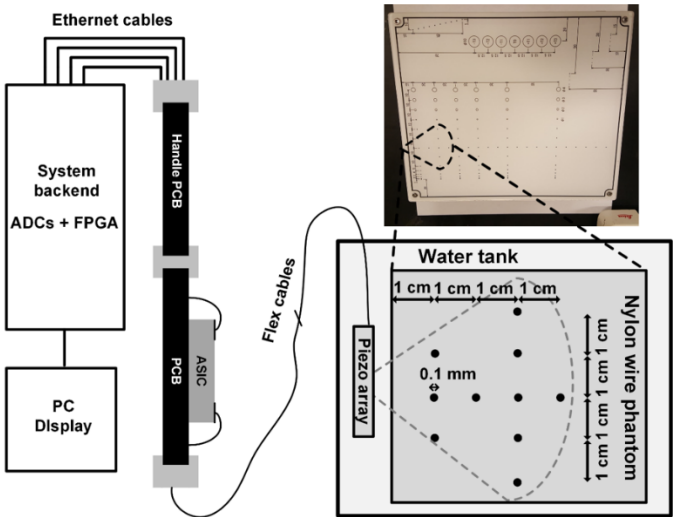

**Figure 50.** ICE System back-end setup.

Figure 49 compares the pulse echo measurement results with and without TGC control, from metal reflector located at 1.6 cm away from piezo array. Figure 49(b) shows that with higher gain of VG-LNA, the echo signals from farther shows high amplitudes compared to the fixed gain operation. The gain increases over time from 15 dB to 21 dB, and 32 dB to compensate for attenuation in the water. Figure 50 shows the system back-end consisting of twelve 200 Msps ADCs (ADC16DX370 from TI), embedded in a custom PCB to support up to 12 TDM signals, a FPGA board (5SGSMD5K2F40C2N from Altera),

power supply module, and a PCI express card, which delivers data from FPGA to PC via optical fiber to shield the MRI machine from external noise.




(a)




(b)

**Figure 51.** (a) Measured B-mode image of 10 nylon wires in a standard phantom and (b) imaging setup diagram with phatom.

**Table 5.** Benchmarking table of state-of-the-art ultrasound array ASICs.

| | **This Work** | [22] ISSCC'17 | [23] JSSC'17 | [30] ISSCC'17 | [83] TBCAS'12 | [73] ISSCC'14 |
|---|---|---|---|---|---|---|
| Integrated Tx-BF | **Yes** | Yes | No | No | No | No |
| Rx wire reduction | **TDM** | S/H analog | S/H analog | ADC + FIFO | Analog filter | S/H + Digital |
| Rx raw data accessibility | **Yes** | No | No | Yes | No | No |
| Delay min (ns) | **5** | 25 | 30.3 | 8.33 | 1.75 ~2.5 | 6.25 |
| Delay max (us) | **10.235** | 0.750 | 0.272 | 1.067 | 0.035 | 8 |
| Die area ($mm^2$) | **28.6** | 416.64 | 37.21 | 9.37 | 0.36 | 19.35 |
| Die dimension($mm^2$) | **2.6×11** | 22.4×18.6 | 6.1×6.1 | 2.93×3.2 | 1.2×0.3 | 4.5×4.3 |
| Power consumption / channel | **6.26mW** | 0.7mW | 0.27mW | 17.5mW | 4.62mW | 17.81mW |
| # of channels | **64 Tx / 64 Rx** | 128 Tx / 3072 Rx | 1024 Rx | 16 Rx | 8 Rx | 64 Rx |
| # of wires | **22** | > 128 | > 160 | - | - | - |
| Tx amplitude | **60 V** | 136 V | - | - | - | - |
| Transducer | **PZT / CMUT** | 2D PZT | 2D PZT | 2D CMUT | Annular CMUT | 2D CMUT |
| Process | **0.18µm HV** | 0.18µm HV SOI | 0.18µm | 28nm | 0.35µm | 0.13µm |

Figure 51 shows the simplified measurement diagram and the B-mode images obtained showing 10 nylon wires of 0.1 mm, which is 1 cm away from each other with 40 dB of dynamic range. Table 5 benchmarks the state-of-the-art ultrasound ASIC designs. This work integrates both TX beamforming and RX cable reduction in a single chip, reducing the number of wires from more than 64 down to 22, with 5ns of delay resolution within a span of 10.235ms, while providing the backend image processing engine with access to the entire raw echo data from every channel. This is the equivalent of ~65% reduction in the diameter of the catheter which significantly improves its flexibility and reach. The complete backend system is designed with the capacity to handle up to 12 TDM signals from a 2-D transducer array, which occupies the same footprint on the ASIC, as shown in the Fig. 10.6.4 layout, while supporting a 96-channel system. Since the size of

the pulser often limits the minimum size TX/RX elements on the ASIC, the reduced capacitive loading helps with matching the transducer unit area. This architecture is also compatible with subarray beamforming with switched-capacitor delay, which will pave the way to further reduction in the number of wires in ICE catheters, while supporting higher resolution 3D images.

# CHAPTER 4. SINGLE-CHIP REDUCED WIRE CMUT-ON-CMOS ICE SYSTEM

One of the important advantages of Capacitive micromachined ultrasound transducer (CMUT) technology is the ease of electronics integration which is particularly important for catheter-based imaging such as intracardiac echocardiography (ICE) and intravascular ultrasound (IVUS). Using a low temperature fabrication process, CMUT arrays can be fabricated directly on CMOS wafers containing the imaging electronics to realize a single chip imaging system. This compact single chip integration approach can provide less complex and lower cost catheter structures as compared to piezoelectric transducer-on-CMOS integration. Current commercial ICE catheters have limitations of large number of interconnections, since each channel element of transducer requires a separate connection to external ultrasound system. This is a barrier to improve the image quality by limiting the number of elements. Also for utilizing ICE catheters during magnetic resonance imaging (MRI), the interconnection number should be minimized to reduce RF-induced heating of the conducting lines. Furthermore cable reduction is required to implement 3D ICE imaging using 2D transducer arrays. Figure 52(a) shows the transducer, ASIC, flex circuits, catheter cable and connection scheme of state-of art piezo-on-ASIC approach, which requires complicated, expensive, and multiple layers implementation. CMUT-on-CMOS package, as shown in Figure 52(b), can provide with simple implementation with compact package by using single CMUT-on-CMOS chip.

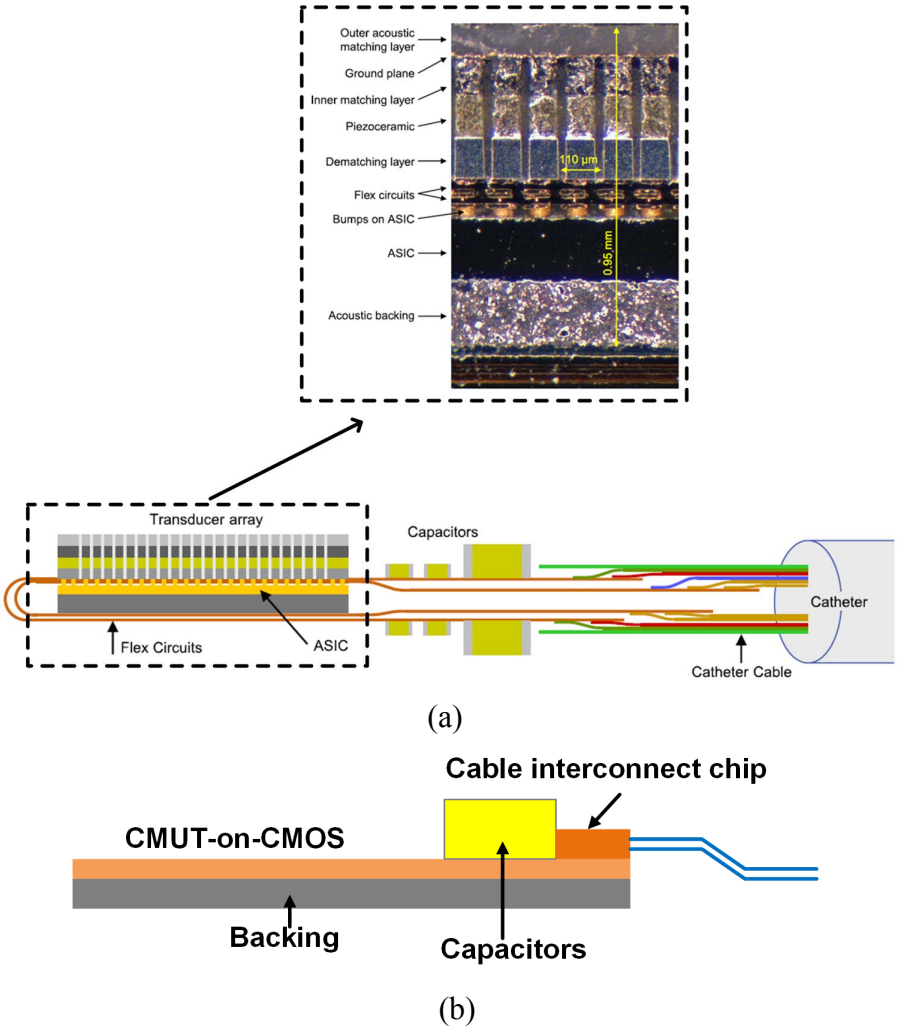



**Figure 52** (a) Connection scheme and complicated side section view of state of art piezo-on-ASIC, and (b) CMUT-on-CMOS.

In this chapter, the CMUT-on-CMOS based ICE imaging concept is demonstrated on a 64 element array designed for 2D ICE imaging. Cable reduction on the transmit (Tx) side is achieved by integrating a fully programmable Tx beamformer, whereas 8:1 time division multiplexing (TDM) is used on the receive (Rx) side. This approach allows access to raw channel data so that imaging performance is not compromised, and the Tx and Rx apertures are matched with each element having a dedicated high voltage (HV) pulser for best lateral resolution. The proposed catheter tip structure is schematically shown in Figure

53. With reduced number of cables, this approach would yield a mechanically flexible catheter which can potentially be cooled when used under MRI.

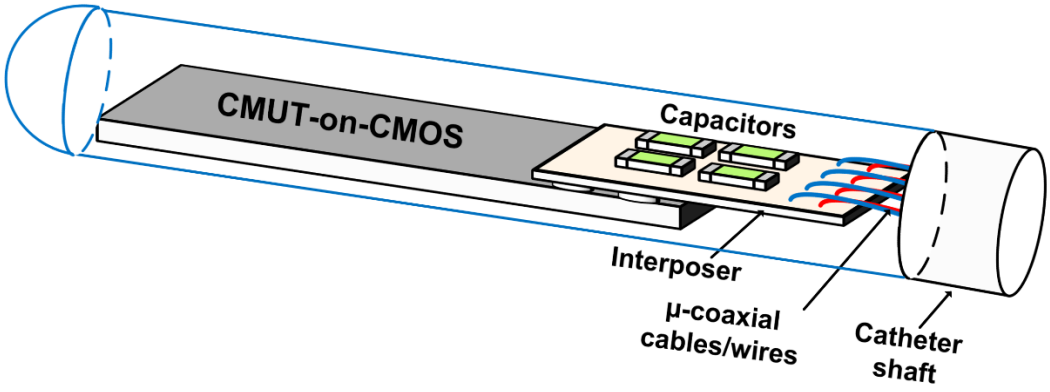



**Figure 53.** Schematic drawing of the ICE catheter tip using a single chip CMUT-on-CMOS system. The chip would be connected to the catheter cables using an interposer.

## 4.1 System Architecture

The proposed system aims to reduce the number of wires at the catheter tip by implementing Tx beamformer and Rx TDM circuits in a single-chip for ICE application. Fig. 2 shows the simplified block diagram of the proposed ICE system. Each of 64 CMUT elements is driven by a HV pulser, which can generate 60 V unipolar pulse. The beamforming profile can be loaded during each firing to steer and focus ultrasound beam over the desired ±45° field of view with a single low-voltage differential signaling (LVDS) data line. A Tx/Rx switch protects low voltage (LV) circuits from HV pulser during Tx operation period. Variable gain low noise amplifier (VG-LNA) compensates for the attenuation of reflected echo signal by adjusting gain at 4 levels to implement simple time gain compensation (TGC), which does not require extra TGC circuits in addition to LNA. The TDM circuitry reduces the number of output signals from 64 to 8, and the high

frequency (HF) buffers drive the TDM signals to catheter handle. After that, the TDM signals are delivered through Ethernet cables to the backend system. The ADC in the backend system samples the corresponding channel at the right time to implement direct digital demodulation (DDD) [74]. The CMUT array is directly fabricated on top of the ASIC as shown in Fig. 1, and the interposer is placed at the end of the chip with pads to connect the ASIC with $\mu$-coaxial cables and wires to the catheter. The catheter cables consists of a μ-coaxial cables for 200 MHz of clock, data, and TDM output signals and single wires for power, bias and control lines. The received multiplexed echo signals are delivered through catheter handle to ADCs in the backend system, where DDD is performed in the FPGA for advanced imaging processing in the digital domain.

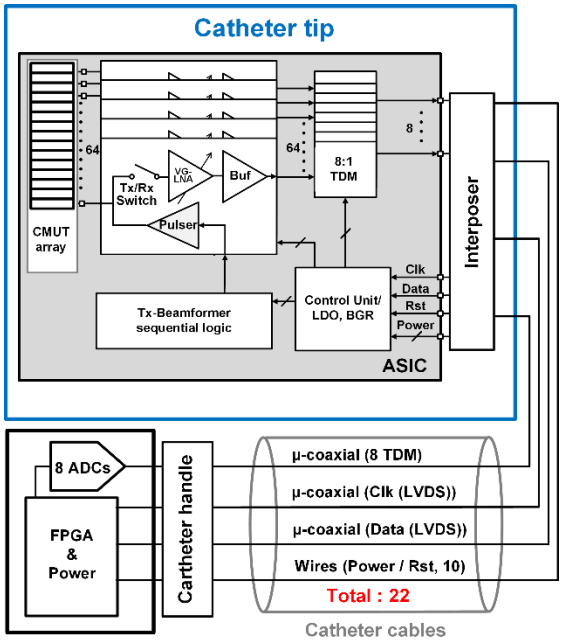



**Figure 54.** Simplified block diagram of the proposed CMUT-on-CMOS system.

The backend system consists of a power supply module which has AC-DC converter, DC-DC converters, an FPGA board, an ADC board to support 8:1 TDM system,

and PCI express interface to deliver data from FPGA to a computer via an optical fiber, to provide MRI compatibility.

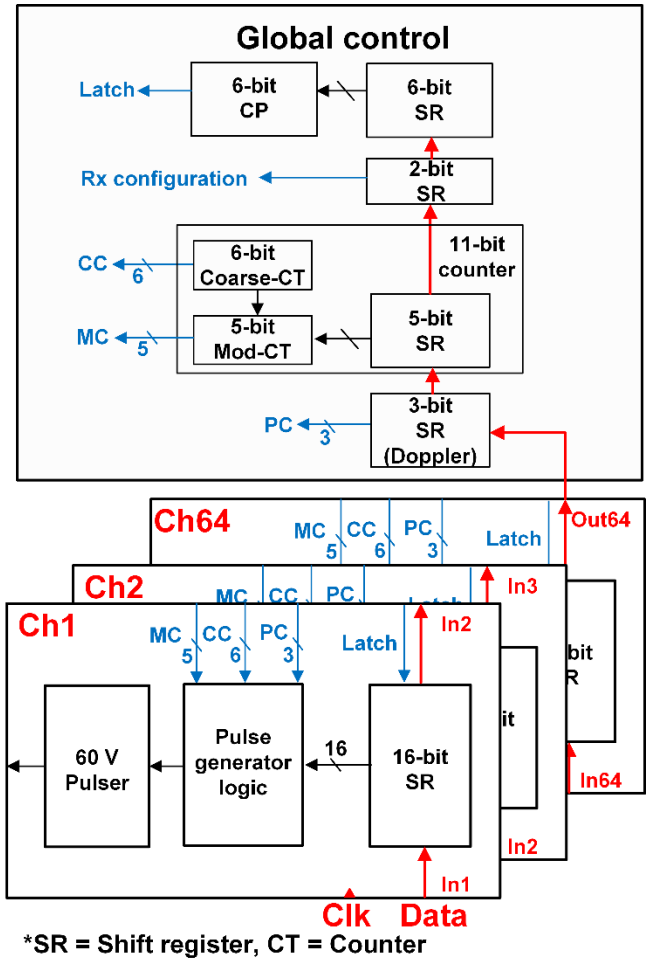



**Figure 55.** Simplified block diagram of the Tx beamformer with Pulser.

### *4.1.1 Tx Beamformer Operation*

Tx beamformer is designed to reduce the number of cables by implementing serial-in parallel-out (SIPO) shift registers for each of the 64 channel, which only one LVDS data line is required to load the data. It creates a maximum delay of 10.235 $\mu$s with a resolution of 5 ns, which enables the desired view angle of ±45°. This beamformer features pulse-

width apodization, so that each Tx element can be driven with a different pulse width [75]. Also for pulsed wave Doppler operation, the beamformer can create multiple pulses up to 8, for narrow band and higher signal-to-noise ratio (SNR) operation. Figure 55 shows the simplified block diagram of Tx beamformer with pulser. In global control logic block, 6-bit of course counter (CC) and 5-bit of mod counter (MC) generate the control information that the shift registers of each channel can determine the exact delay, pulse width, and number of pulses for each channel, respectively. Each of the 64 channels has 16-bit SIPO shift register that stores beamforming profiles. Once the data is loaded properly, the latch signal locks the shift registers and the counters start to count for pulse generation. It also includes a 2-bit shift register for Rx gain control configuration, since the beamformer knows the timing of TGC control. To program the delay profile for all the channels, each programming cycle requires a 1040-bit data packet, which corresponds to 5.2 $\mu$s. All the registers are reset before programming Tx beamformer, and the data packet is generated and sent from the FPGA from backend system.

### *4.1.2 Rx Circuitry*

As shown in Figure 54, 64 channels of Rx circuitry consist of Tx/Rx switch, VG-LNA, buffer, and TDM circuitry. The LNA is designed to have 4 different gain stages (15 dB, 21 dB, 27 dB, and 32 dB) to meet the dynamic range of ADC in the backend system with the assumed input echo signal dynamic range of 76 dB. Rx front-end topology in ultrasound system usually depends on the electrical impedance of transducer type. The transimpedance amplifier (TIA) is a commonly used topology in CMUT because the equivalent electrical model of CMUT is comparably high impedance. However, for this

particular application with comparably large 1D CMUT array elements, the impedance level is low. Therefore a LNA structure is adopted for driving relatively large capacitance (~10 pF) [81]. During the Tx period, the LV circuits should be protected by Tx/Rx switch from HV pulse. After HV pulse generation period, VG-LNA amplifies the echo signals based on the traveling time for compensation, the buffer drives the signal to TDM circuitry. The TDM circuitry samples and combines the output signals with 8:1 ratio to the backend system. The TDM technique allows multiple channels to share the same cable by assigning a corresponding time slot to each channel. Analog TDM requires a relatively simple design and less power because it needs analog multiplexer, digital counting logic which can be shared with Tx beamformer, in addition to sample and hold circuits, which is suitable ICE application. Also in this proposed system, by using DDD technique, ADC could sample TDM output with the same frequency. This results in less data processing to increase efficiency in the backend system [74]. In this system, the clock frequency is chosen as 200 MHz, resulting in 25 MS/s for each channel of 8:1 TDM circuitry. To reduce the cross-talk level due to inter symbol interference, the HF buffer is designed to have around 400 MHz bandwidth. The TDM circuitry consists of 8 sets of TDM blocks, and each TDM block consists of 8 channels of sample and hold switches. The link training switch is used to optimize the sampling time and identifying the channel numbers. Phase synchronization for the TDM sampling is performed in FPGA of backend system, so that ADC takes samples when the signal through the interconnection has stabilized rather than during the switching transients.

Note that this TDM approach can be combined with well-known subarray beamforming (SAB) techniques as the frequency content of the subarray beam-formed signals is the same as the raw data [84]. This would be particularly useful in 2D arrays where cable reduction is a requirement. With a typical 3x3 subarray, cable reduction ratio of 72:1 can be achieved with using TDM cascaded with SAB. Alternatively, SAB size can be reduced for better imaging performance as TDM will provide the desired overall cable reduction ratio.

The ASIC for this CMUT-on-CMOS system is fabricated in a 0.18-$\mu$m 60 V power management 4M1P HV-BCD CMOS process. It consists of 64 channel AFE (pulser, Tx/Rx switch, LNA, and buffer), Tx beamformer, and symmetrically designed TDM, which occupies 2.6×11 mm$^2$, as shown in Figure 56. The pads for power supply, control signals, and TDM outputs are located on the right side, on which an interposer will be bonded to connect $\mu$-coaxial cables and wires.

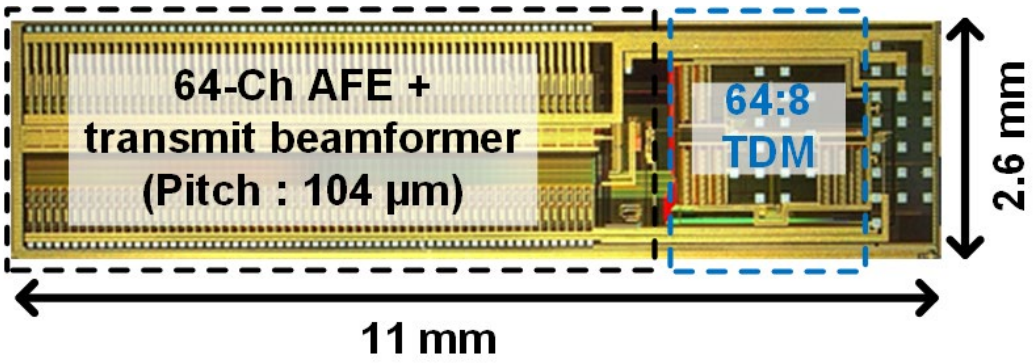



**Figure 56.** Microphotograph of the ASIC.

## 4.2 CMUT Design and Fabrication

Most of the commercial medical ultrasound imaging utilizes piezoelectric transducer. However, the catheter based application such as ICE and IVUS need to be inserted and navigate the vascular system requires a flexible tip of the catheter which carries transducer and associated electronics. Due to this consideration, the size of the tip should be small enough, and transducer and electronics should have short width and length. Thus, integration of transducer and electronics are highly desired to reduce dimension and interconnections, but, because of fabrication characteristics of a piezoelectric transducer, it is not easy to be integrated with CMOS. From the needs for addressing those limitations, a capacitive micromachined ultrasound transducer (CMUT) was introduced [85]-[89].

The early concept of CMUTs was announced in the same age of early piezoelectric transducers [90]. However, the CMUT's requirement of strong electric field strength ($10^6$ V/cm), which was difficult to be achieved with the silicon technology of the time. As time goes on, semiconductor fabrication technology has been rapidly advanced, and the strong electric field strength has become a viable option. CMUTs have several advantages against to the piezoelectric transducer such as, low-cost, ease of large array fabrication, and integration with electronics. All the merits are coming from the nature of CMUT fabrication methodology that is processed by following steps. First, a silicon wafer is heavily doped to work as a bottom electrode of the transducer. Then, silicon nitride that is a dielectric material is deposited on the doped silicon as a protective insulator. Amorphous silicon is deposited on the insulator, patterned by photolithography, and etched to make a sacrificial layer for the vacuum gap. Silicon nitride is deposited over the surface, and

narrow through-holes are etched to make a passage for the etchant to access the sacrificial layer. After the etchant removes all the sacrificial layer, the membrane is released, a silicon nitride is deposited again to block the holes. Then, Aluminum top electrodes are placed above the sacrificial layer by metallization, and a low-temperature-oxide is deposited as a passivation layer [91], [92]. All the steps are the same as the semiconductor technology that is already matured to fabricate dense small arrays with sufficient yield and reduced cost. In addition, because the CMUT fabrication steps do not require high-temperature process and can be fabricated with integrated circuit (IC), the CMUT can be easily fabricated on the electronics without external interconnections [93].

In this research, the CMUT arrays are fabricated using low-temperature CMUT-on-CMOS process [56], [85]. The arrays are processed on the CMOS substrate which is passivated with 3 $\mu$m of Plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN). 250 nm of Cr is deposited for bottom electrode, followed by 120 nm of Cu deposition for the sacrificial layer that eventually forms gap height. 250 nm of SiN is then deposited as the isolation layer to ensure that the top and the bottom electrodes do not short during large membrane displacement. 200 nm of AlSi is sputtered on the isolation layer for the top electrode. The SiN is then deposited to form the actual membrane thickness followed by membrane release, etching sacrificial layer, and drying process.

Figure 57. Microphotograph of the membranes of 1D CMUT-on CMOS element. shows the micrograph of CMUT membranes. Each of 64 element consists of 92 (2×46) membranes, which shows a pitch of 104 $\mu$m with length of 2.392 mm, and each 2 $\mu$m thickness membrane occupies 45×45 $\mu m^2$.

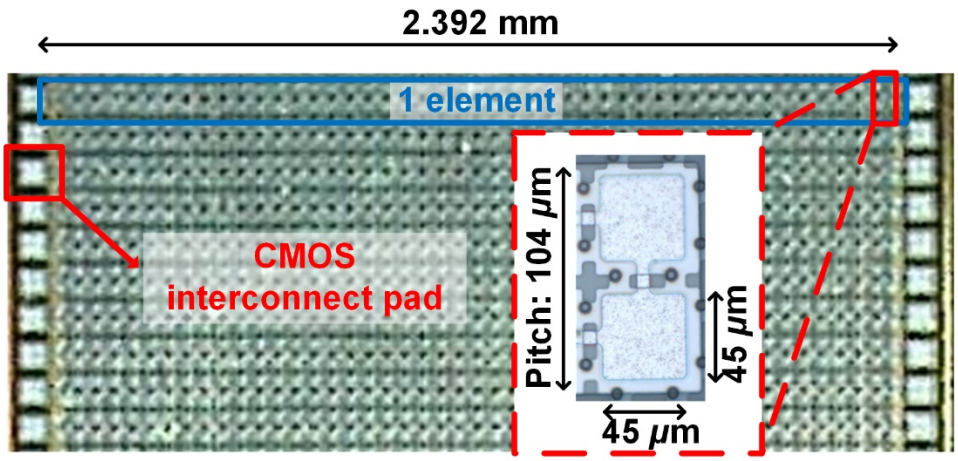
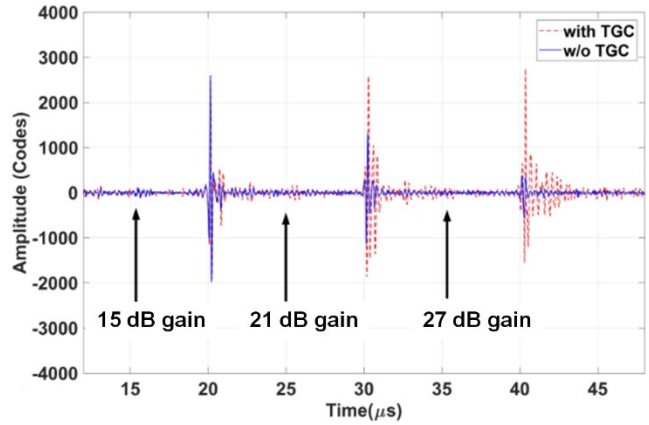
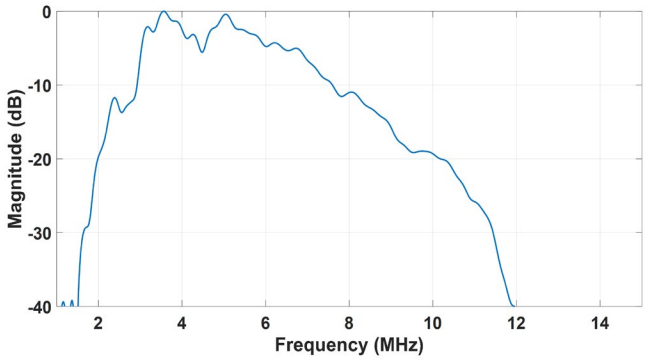



**Figure 57. Microphotograph of the membranes of 1D CMUT-on CMOS element.**




(a)

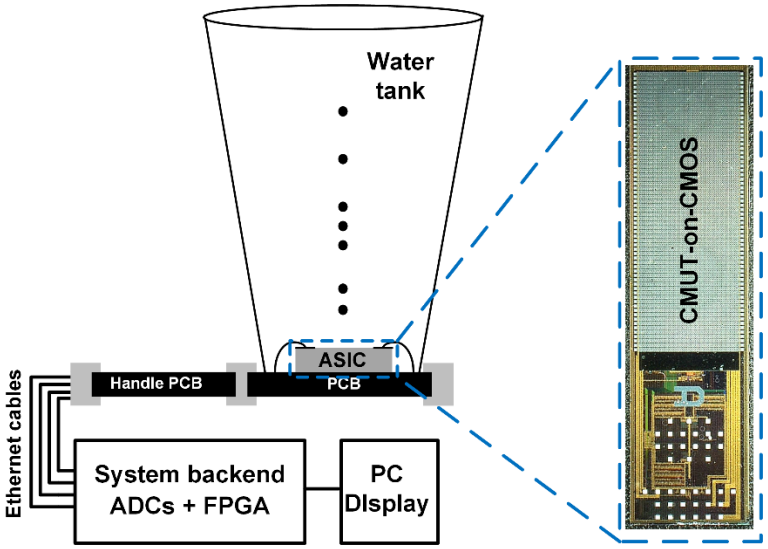



(b)

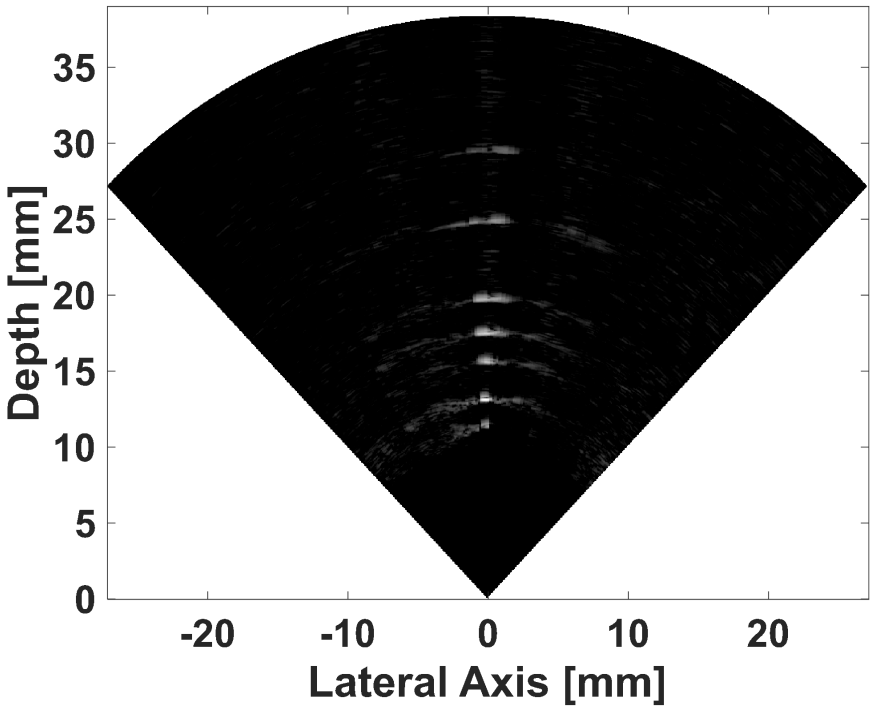
**Figure 58.** (a) Received pulse-echo signals with or without TGC, and (b) frequency spectrum of the echo signals from plain reflector.

## 4.3 Experimental Results

Figure 58(a) shows the pulse echo measurement results in oil using the CMUT-on-CMOS chip. The results are shown with and without applying the TGC gains indicating the functionality of the system. The results show 5 MHz center frequency with 80 % of -6 dB fractional bandwidth (Figure 58(b)), suitable for ICE catheter imaging. Imaging experiments are also performed using 7 metal wires (38 AWG, 101 $\mu$m in diameter). In these experiments, 3 $\mu$m Parylene coated CMUT-on-CMOS chip is immersed in the water facing 7 wires vertically as shown in Figure 59(a). Tx beamformer is programmed to generate 123 focused and steered beams to scan ±45° sector image. The obtained image is shown in Figure 59(b) with 40 dB of dynamic range, clearly showing the expected details of the imaging target.




(a)




(b)

**Figure 59.** (a) Imaging experiment setup diagram with micrograph of CMUT-on-CMOS, and (b) B-mode image of 7 metal wires in the water.

CMUT-on-CMOS approach is used to implement a single chip, reduced wire ICE imaging system. Cable reduction is achieved by integrating both Tx beamformer and TDM based Rx circuitry in a single chip for a 64 element 2D imaging ICE catheter. The Tx beamformer is capable of steering and focusing the Tx beams in a wide angular range and can be programmed with single LVDS data line. TDM based Rx cable reduction has the potential for integration with other channel count reduction techniques for use in 2D arrays for 3D imaging catheters. The electrical and acoustical experimental results confirm the functionality of the complete system and indicate the potential of the approach for cable

count reduction and simple catheter construction leading to lower cost, mechanically flexible ICE catheters with improved image quality and MRI compatibility.

# CHAPTER 5. $\mu$-BEAMFORMER WITH TDM SYSTEM FOR MASSIVE CABLE REDUCTION

In the previous chapters, we described single-chip reduced wire catheter system, which achieved a significant cable reduction by adopting both of the Tx and Rx cable reduction schemes. To further reduce the number of connections for 3-D real-time visualization of moving structures, which usually requires thousands of elements, we propose a reduced cable method which combines $\mu$-beamformer with TDM system.

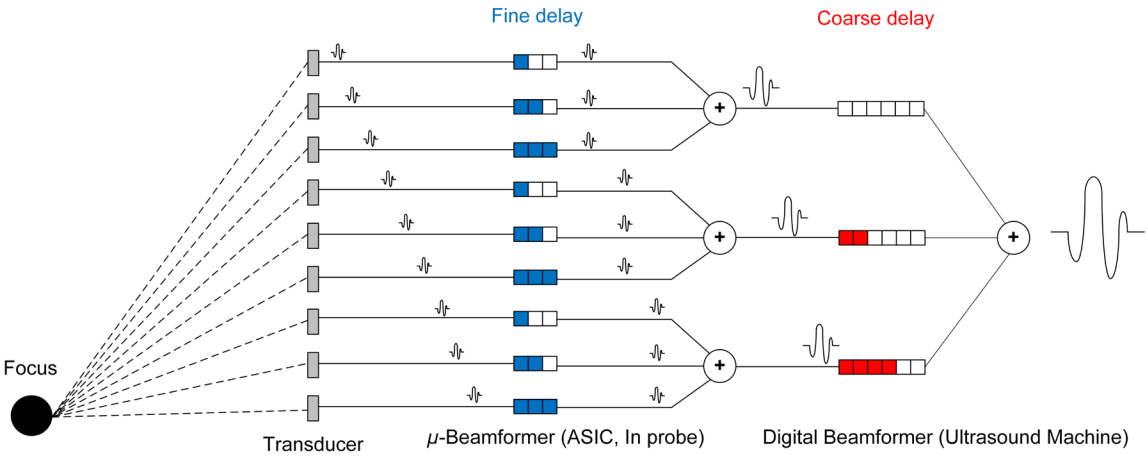



**Figure 60.** $\mu$-beamformer architecture for ICE application.

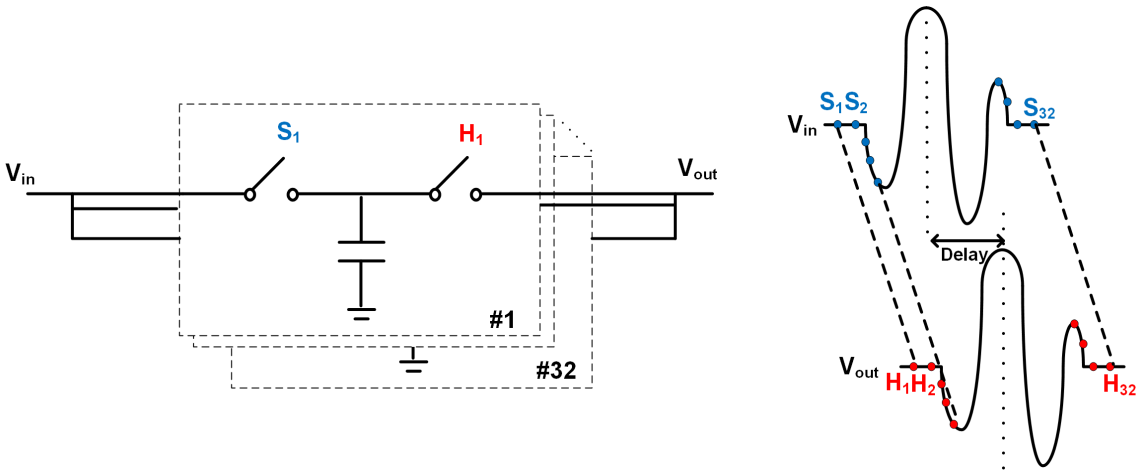



**Figure 61.** Analog delay circuit implementation using switched capacitor.

The sub-array beamforming, *aka.* $\mu$-beamforming, is well known architecture in ultrasound signal processing methodology [21]- [30]. The whole system chain is divided into a front-end, which is implemented within ASIC in the ICE probe tip for fine delay (less than 1 $\mu$s), and a back-end, which is normally designed in an external imaging system for coarse delay as shown in Figure 60. The receiver transducer array is divided into sub-groups, each of them contains N elements (N is 3 in Figure 60). The front-end electronics for each of sub-group include LNA, $\mu$-beamforming circuitry, HV pulser, and Tx/Rx switch. During Tx phase, the pulser is on, and other blocks are all off. During Rx period, signals from transducer are passed through Tx/Rx switch, amplified with variable gain LNA, which the gain depends on the attenuation of traveling time. After that, each element of the sub array is properly fine-delayed and summed to one signal. For implementing fine-delay in ASIC, Analog delay chains which adopt switched-capacitor-based delay has been demonstrated [21]-[29]. This technique is performed by delaying the signals relative to each other in such a way that waves from a certain focal point, arrive simultaneously and can be coherently summed in a sub-array block by using sample and hold circuit as shown

in Figure 61. To enable 3-D real time imaging and to perform increased image quality, lots of considerations should be calculated. For example, the transducer array should be sampled at less than a half wave-length pitch (for fully populated array) [21]. This will conclude that the number of transducers must be increased to the order of thousands, which will require massive cable reduction, since connecting all channels with commercial coaxial cables would not be feasible. Basically, the $\mu$-beamformer provides delaying and summing circuitry, reducing the number of cables.

## 5.1 $\mu$ -Beamformer Design

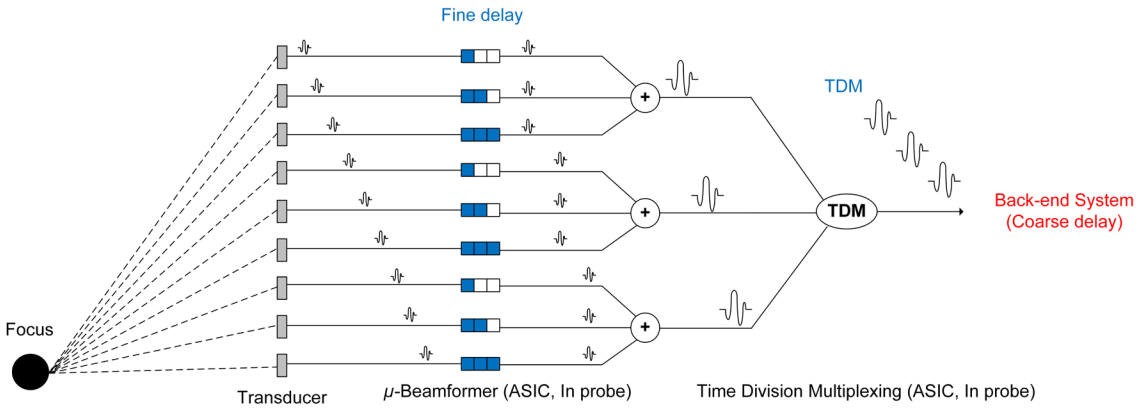



**Figure 62.** Simplified block diagram of proposed $\mu$-beamformer with TDM system.

The $\mu$-beamformer should provide enough delay, adaptable delay step, and at the same time, it should be designed simply for consuming small area and power. For implementing $\mu$-beamformer with current TDM back-end system, the total receive delay is divided into coarse delay and fine delay as shown in Figure 62. First, the total delay is calculated based on focal point and view depth, then the total delay is divided into coarse delay and fine delay. Since the coarse delay can be implemented with external high

performance back-end system, the on-chip fine delay part can be simplified to have less than 1 $\mu$s range for each element of the sub-array, which significantly reduce the system complexity in ASIC side. The sub-array size is determined based on the center frequency, beamforming direction in lateral and elevation directions. A larger sub-array will reduce more cable counts, whereas it also required greater maximum fine delay and higher grating lobe level [23]. We select the 3×1 sub-array size for proof-of-concept, targeting the same 1-D array ICE transducers in previous chapters. Considering the fact that we have already developed 8×1 TDM structure, this $\mu$-beamformer combined with TDM will give a cable reduction factor of 24. This will give us the system with current 64 elements will result in 3 cables, 120 elements with only 5 cables. The maximum fine delay can be calculated based on view angle and number of elements, and pitch size. For example, with 150 $\mu$m of pitch size for center frequency of 5 MHz (wave-length($\lambda$) of ultrasound in the body is ~300 $\mu$m), 45 degree beam steering will require ~1.4$\lambda$, meaning that it needs at least 280 ns of maximum fine delay (The period of $\lambda$ is 200 ns). The step of fine delay is also important. The recent study shows that for the angles of 0°, 17°, and 37° with similar center frequency specification, 30 ns step can show reasonable grating lobe of -20 dB relative to the main lobe based on Field II simulator [26]. For our 1-D array application for ICE, we chose the step size of 10 ns, maximum delay of 320 ns, so that we can have -20 dB of grating lobe level and fine angles of 0°, 4°, 9°, 13°, 17°, 22°, 26°, 31°, 34°, 39°, 43° and 47°, which will have higher freedom of focusing angles.

Implementing a new system which combines sub-array beamformer (SAB) and TDM system that can massively reduce the number of cables. For example, if we can

implement 5:1 SAB with 8:1 TDM system, it can provide 40:1 cable reduction, thus it could be good solution for cable reduction of 2-D array system. For proof-of-concept, we designed a 3:1 SAB and 5:1 SAB with 8:1 TDM system with single data line implementation as shown in Figure 63. If we adopt this system with current 64 channel system with 3:1 SAB and 8:1 TDM, it would require 3 received echo signal lines instead of 64 raw echo signals, 1 reset cable, 1 data cable, and power lines including grounds connection resulting in massive cable reduction.

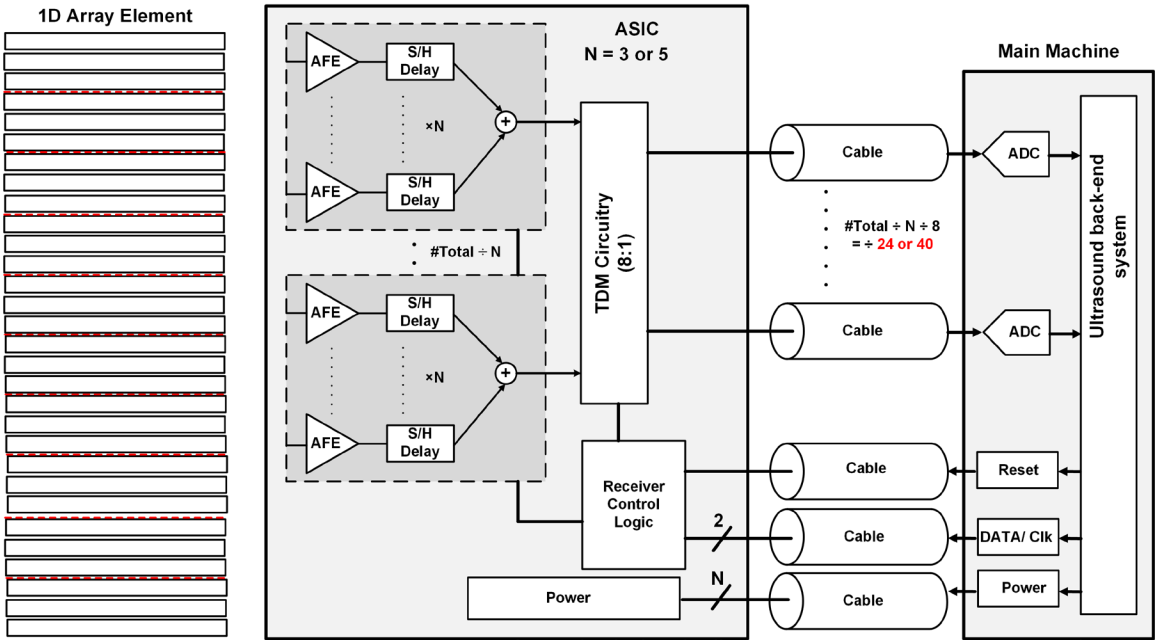



**Figure 63.** Proof-of-concept of $\mu$-beamformer with TDM system.

## 5.2 System Architecture

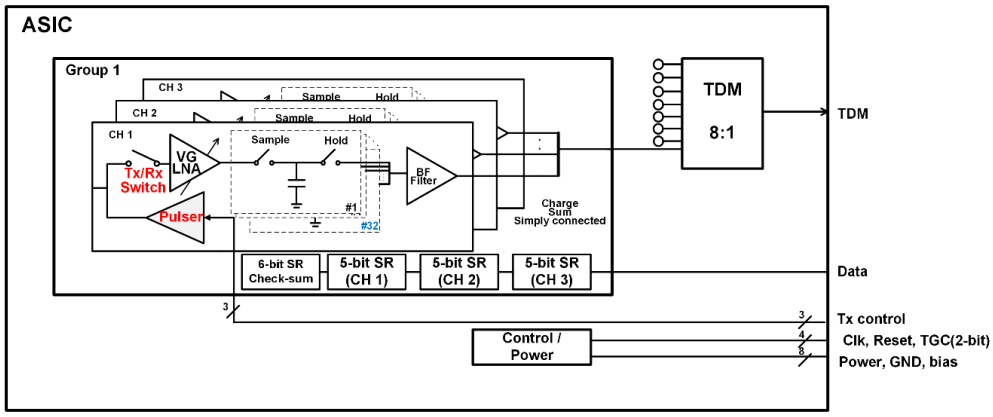
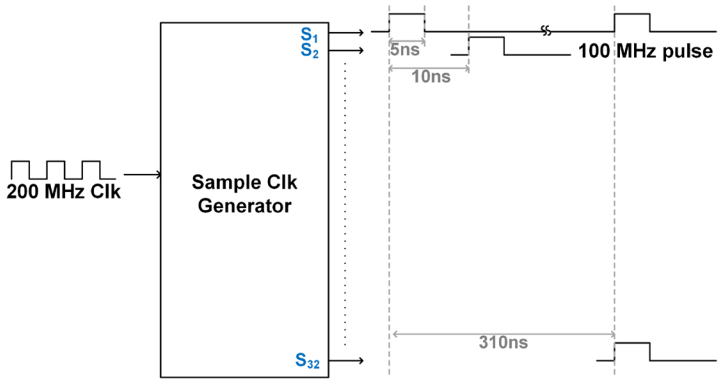
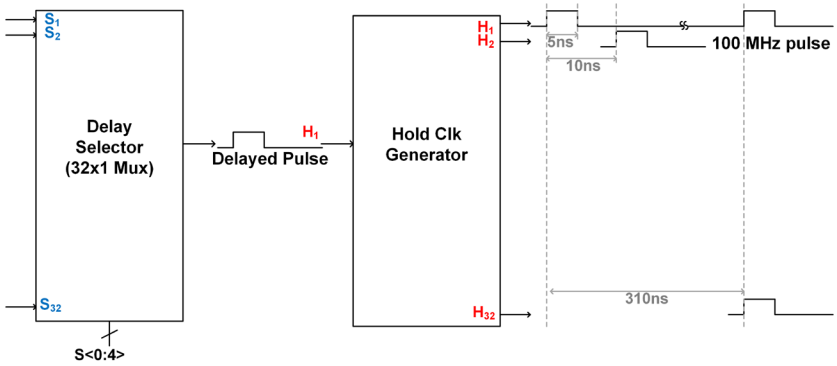



**Figure 64.** Circuit implementation of AFE, $\mu$-beamformer with TDM system.




(a)




(b)

**Figure 65.** (a) Simplified block diagram of global sample clock generation, and (b) local hold clock generation for switched capacitor delay cell.

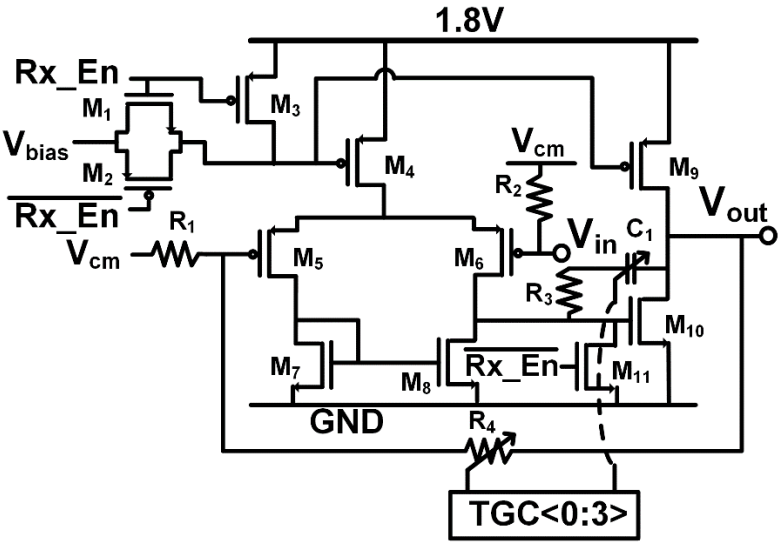
Figure 64 shows the circuit implementation of proof-of-concept for hybrid Rx cable reduction system, which consists of Analog Front-End (AFE), 3×1 sub-array with TDM system. AFE of each channel of sub-array consists of HV pulser, Tx/Rx Switch, and variable gain LNA, followed by $\mu$-beamformer, and band-pass (BF) filter. As shown in Figure 64, a sub array group has 3 sub elements, and these elements are properly controlled by serial-in-parallel-out (SIPO) shift registers to accomplish calculated fine delay. Each sub-array group requires 15 bit of delay data, 3 of 5 bit shift register (SR) is for fine delay control for each of sub array elements, and top 6 bit SR is needed to check whether the received data is valid or not. The operation of receive beamformer is similar to previous transmit beamformer [94]. The FPGA code of back-end system needs to be modified to generate Rx delay data signal, instead of generating 1040 (64×16+2+3+5+6) data packet of Tx delay profile. For loading Rx delay profile of 1 sub-array, 21 (3×5+6) data packet is required. For example, if data packet of "111111,00010,00100,01000" is generated from back-end FPGA, then the first element will be delayed 20 ns, second element will be 40 ns, and the last one will be 80 ns (Each of 5 bit SR load the fine delay profile, if this has "00000" data, then the delay is 0 ns. If it has "00100", it will have 4*10 ns delay). Figure 65 shows the simplified control block diagram for sample and hold clock generation of switched capacitor Analog delay block (shown in Figure 61). For designing the delay control block of a sub array, sample clock generation block of Figure 65(a) can be shared, and hold clock generation block of Figure 65(b) is needed separately for each of the elements of sub array. For summary, implementing 1 sub array elements with 3 elements, 1 of global sample clock generation block and 3 of local hold clock generation blocks are

required. In this proof-of-concept design, each pulser is driven from external Tx control input pulse signals, requiring 3 different input pulse (1.8 V of input pulse shape will be level-shifted to output of 70 V of HV pulse). TGC control signal is 2-bit signal, which can control LNA with 4 different gain stages. In contrast to the previous TDM only structure, BF buffer is added to cancel out the DC offset, which can cause significant variation in TDM input. The TDM block is connected to BF buffer through port number 1, and other 7 ports are designed to be connected with other $\mu$-beamformer chips if needed. Only one group of sub-array is connected to TDM input, and 7 of other inputs are connected to test pad, so that it can be wire-bonded to test structure of other sub-array group, due to limited area of silicon implementation. The main target of this study is the implementation of massive cable reduction, keeping the back-end ultrasound system same. Instead of using data line for transmit data loading, this circuitry utilized data line for receive beamforming, thus we do not need to change back-end hardware system. In this system, Pulser, LNA, Tx/Rx switch, and TDM are designed with the same topology as in [95]. We also implemented 5:1 SAB with 8:1 TDM system, with the same concept.

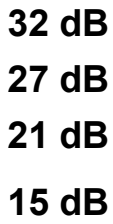
## 5.3 Circuit Implementation

The ASIC for this $\mu$-beamformer combined with TDM system is fabricated in a 0.18-$\mu$m 70 V power management 6M1P HV-BCD CMOS process from TSMC. Most of the circuits of AFE (LNA, Tx/Rx Switch, and Pulser), and TDM are properly scaled and modified to be transferred from TowerJazz process to TSMC. For receiver circuitry, as mentioned in chapter 3, LNA structure is preferred because of relatively low impedance nature of 1-D array piezo elements [23]. Considering the area efficiency which in this

process, the required capacitor occupies larger area than resistor, and minimizing a low-frequency shift of the pulse-echo response, the resistive feedback LNA structure is selected for this system [81]. Also instead of implementing LNA and time gain control (TGC) circuit separately, this system adopts variable gain LNA structure for system simplicity.

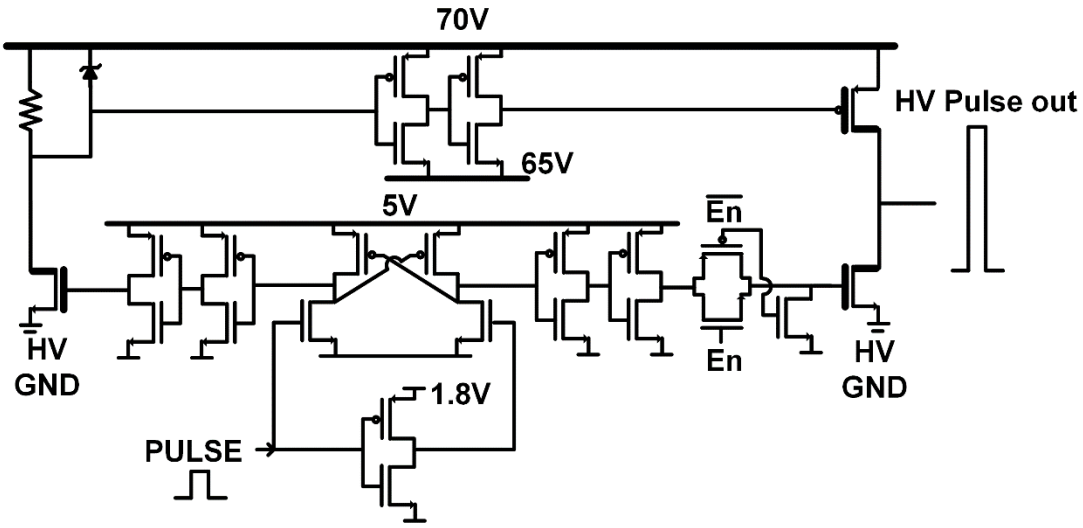



(a)

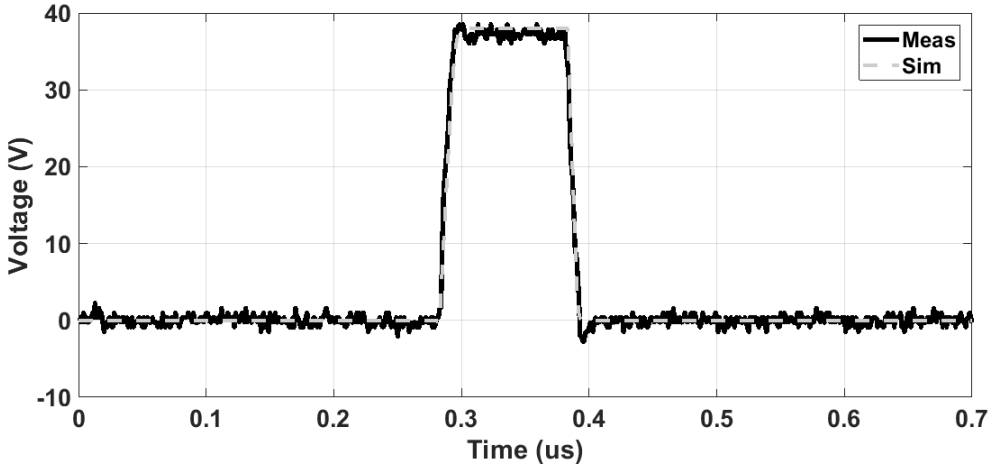



(b)

**Figure 66.** (a) Schematics of variable gain LNA, and (b) measured frequency response of variable gain LNA with different 4 gains.




(a)




(b)

**Figure 67.** (a) Schematics of proposed 70 V pulser, and (b) the simulated and measured result of pulser with 38 V supply.

Figure 66(a) shows the schematic of variable gain LNA structure. The gain is controlled by 4-bit TGC signal through data line, which is generated by FPGA from backend system. Figure 66(b) shows the measured frequency response of different gain stages, which shows 15 dB, 21 dB, 27 dB, and 32 dB at center frequency of 5 MHz with 3 dB bandwidth of 12 MHz. The simulated input referred noise at 5 MHz shows average less

than 8.6 nV/√Hz. The Miller compensation leg capacitor of $C_1$ is also controlled by TGC signal to push the second pole of this 2-stage op-amp well beyond the closed-loop bandwidth to keep phase margin above 60º in every gain stages. Rx_EN signal and switch transistors ($M_1$, $M_2$, and $M_{11}$) are required for power saving mode during transmit data loading period. Pulser is one of the key building blocks of ultrasound imaging systems, which drives ultrasound transducers such as piezoelectric material or CMUT with HV output swing to create an ultrasound pressure pulse towards the tissues. Figure 67(a) shows the implemented schematic of pulser. Figure 67(b) shows the comparison of measured and simulated results of pulser with 38 V peak-to-peak (Supply: 38 V), and rise time and fall time are 10 ns, respectively.

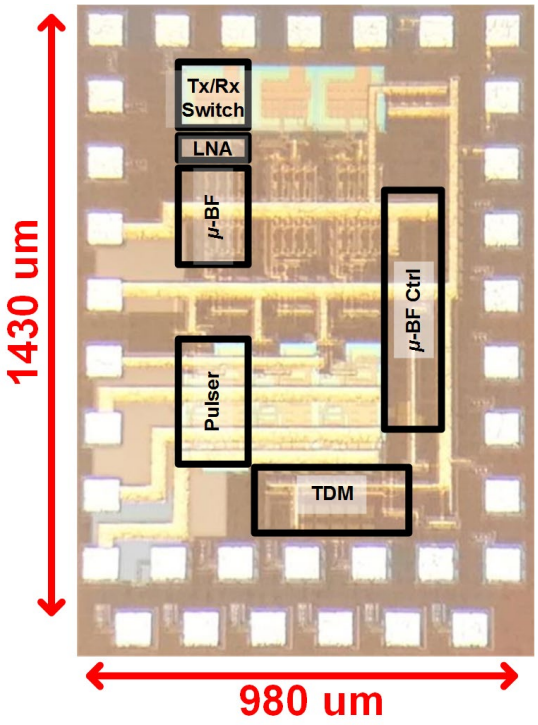



**Figure 68.** Micrograph of $\mu$-beamformer combined with TDM system.

Figure 68 shows the proposed 3×1 sub-array with TDM system. The proposed system paved the way to further reduce the cable count. The system is adoptable with the previously proposed back-end system [95], so that it can be simply plugged in with data modification, without any hardware change. Even though this proposed circuit is only for proof-of-concept, the main idea and implementation could be implemented with full array, so that it can propose the massive cable reduction.

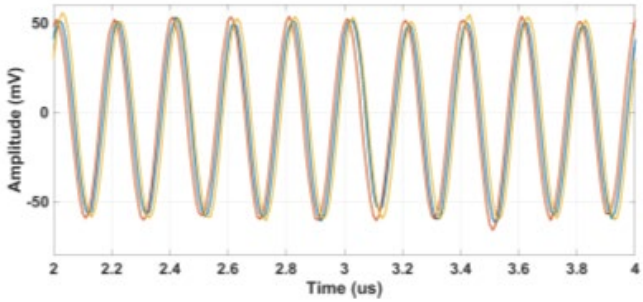



**Figure 69.** Measurement results of delayed 3 received signals with step size of 10 ns.

Figure 69 shows the measurement results of $\mu$-beamformer output signals. Each signal is delayed 10 ns, which is the minimum delay resolution. This sampled signal is sent to BF buffer to TDM signals, and the output of TDM signal will be sent to back-end system for demultiplexing each of 8 channels on the screen.

# CHAPTER 6. CONCLUSION AND FUTURE WORK

This dissertation focused on developing a new silicon level system for intracardiac echocardiography, which resulted in several innovative circuits [58],[66],[94]-[97]. The single chip ICE system reduced a number of interconnections, which is crucial in integrating the transducer with ASIC in catheter-based ultrasound application. With the impact of cable reduction, this system can improve mechanical flexibility, lower cost, and be compatible with MRI operation, since it can minimize the RF-induced heating. In addition to the system level design, this dissertation also described various voltage doubling technique for driving ultrasonic transducers, which can apply maximum pulse voltages afforded by IC process. This can improve safety with lower voltages on the catheters while not compromising the pulser voltage level.

## 6.1 Conclusion of Supply-Doubled/Inverted Pulser Design

This chapter presented an integrated voltage-doubling, voltage-inverting, and pulse-shaping HV pulser circuit to interface CMUT ultrasound systems in a 0.18-μm 60 V 4M1P CMOS/DMOS process. The presented circuit overcomes process limitation by adopting HV protection techniques that generate ~85 $V_{pp}$ of output pulse with 45 V supply voltage. A three level pulsing scheme is successfully applied to a CMUT array element and optimized for maximum acoustic pressure, as predicted by a large signal CMUT model, paving the way for simulation-based CMUT pulser optimization. The prototype pulser ASIC measurements were conducted with an off-chip capacitor, which can be integrated with the CMUT using high-K dielectric layers during CMUT fabrication.

The supply-inverted pulser generates 79.6 V of peak-to-peak voltage swing using 45 V of positive supply with 8 pF of equivalent CMUT loading and 30 pF of external

capacitance. A bipolar pulse was successfully applied to a CMUT array element and optimized for maximum acoustic pressure. The output followed predictions by a large signal CMUT model, paving the way for large signal simulation-based CMUT-pulser optimization. The proposed Tx/Rx switch effectively blocks the HV swing of the supply-inverted pulser without degrading the performance of the proposed pulser. While the prototype pulser and Tx/Rx switch measurements were conducted with an off-chip capacitor, the technology exists to allow this capacitor to be integrated with the CMUT, using high-K dielectric layers, during CMUT fabrication.

## 6.2 Future Work of Supply-Doubled/Inverted Pulser Design

On-going research involves co-optimization of the pulser and CMUT arrays using CMUT-on-CMOS technology for compact catheter-based ultrasound imaging systems. Also during CMUT fabrication, the capacitors can be implemented in the CMUT layer on top of IC. Specifically, the required capacitor is usually an order of magnitude larger than $C_{CMUT}$, can be implemented during microfabrication underneath the CMUT. This is schematically shown in Figure 31, where a CMUT element is built over a fixed capacitor, $C$, with approximately the same area, and connected to the CMOS electronics using CMUT-on-CMOS technology. While the CMUT capacitor, $C_{CMUT}$, has a vacuum gap, $C$ is formed by filling a similar gap with a high-K dielectric, such as hafnium dioxide with $\varepsilon_r$ = 16. With non-collapsed CMUT operation, one can easily satisfy the required $C >> C_{CMUT}$ condition in this approach, considering that in CMUT-on-CMOS implementation the parasitic capacitance will be minimized. For instance, a breakdown voltage of 60 V can be achieved with hafnium dioxide with a typical gap/dielectric thickness of 150 nm [98] . This approach would enable fabrication of a high voltage capacitor in the CMUT layer for compact ultrasound analog front-end design in imaging applications.

## 6.3 Conclusion of Single-Chip Reduced Wire Catheter System

The proposed ASIC has integrated both transmit beamformer and Rx cable reduction in a single chip, reducing the number of wires from more than 64 down to 22, with 5 ns of delay resolution within a span of 10.235 $\mu$s, while providing the backend image processing engine with access to the entire raw echo data from every channel. This is the equivalent of ~65% reduction in the diameter of the catheter which will significantly improve its flexibility and reach. The complete backend system is designed with the capacity to handle up to 12 TDM signals from a 2-D transducer array, which will occupy the same footprint on the ASIC, while supporting a 96-Ch system. Since the size of pulser often limits the minimum size Tx/Rx elements on the ASIC, the reduced capacitive loading helps with matching the transducer unit area. This architecture is also compatible with subarray beamforming with switched-capacitor delay, which will pave the way to further reduction in the number of wires in ICE catheters, while supporting higher resolution 3D images. The ASIC successfully was assembled with 64 channel piezo-transducer array, showing 50 dB of dynamic range.

## 6.4 Conclusion of Single-Chip Reduced Wire CMUT-on-CMOS ICE System

CMUT-on-CMOS approach is used to implement a single chip, reduced wire ICE imaging system. Cable reduction is achieved by integrating both Tx beamformer and TDM based Rx circuitry in a single chip for a 64 element 2D imaging ICE catheter. The Tx beamformer is capable of steering and focusing the Tx beams in a wide angular range and can be programmed with single LVDS data line. TDM based Rx cable reduction has the potential for integration with other channel count reduction techniques for use in 2D arrays for 3D imaging catheters. The electrical and acoustical experimental results confirm the functionality of the complete system and indicate the potential of the approach for cable

count reduction and simple catheter construction leading to lower cost, mechanically flexible ICE catheters with improved image quality and MRI compatibility.

## 6.5 Future Work of Single-Chip Reduced Wire CMUT-on-CMOS ICE System

Developing the CMUT-on-CMOS fabrication process at Georgia Tech has been challenging, and this CMUT-on-CMOS design is on-going. Due to limited facility and environment, we have also decided to work with commercial company such as Vermon or Phillips for CMUT array [99],[100]. With the current working ASIC, we can design the interposer layer between the commercialized CMUT array and ASIC, so that we can deliver one-chip solution for ICE application transducer. The package required flip-chip bonding and $\mu$-coaxial cable design, and this problem can be solved with the help from TE connectivity. The final product from this project will have compact package as shown in Figure 53.

## 6.6 Conclusion of $\mu$-beamformer with TDM system for massive cable reduction

The proof-of-concept $\mu$-beamformer combined with TDM system was designed and fabricated in a 0.18 $\mu$m 70 V power management process from TSMC. The proposed system shows that the combined system can result in 24:1 or 40:1 cable reduction, which can benefit the catheter based application such as ICE and IVUS. The cable reduction is achieved by integrating receive beamformer with single data line. The proposed fine delay shows 10 ns of delay step, and 320 ns of maximum delay for 5 MHz of Tx frequency operation. The proposed system also integrate HV pulser with LV circuitry, enabling the same element transmitting and receiving performance.

## 6.7 Future Work of $\mu$-beamformer with TDM system for massive cable reduction

Based on the proof-of-concept design, the future system can be completed with 64 element 1-D array transducer or 2-D array transducer. The current data cable is assigned for only Rx delay data loading. However, this data cable can be shared with Tx beamformer. For implementing the Tx beamformer, simply shift registers can be added serially, so that it can load Tx and Rx beamforming data altogether. Since most of the Analog front-end design is transferred from TowerJazz to TSMC, new design can be implemented with 0.18 $\mu$m 70 V power management process, providing with the single-chip solution with massive cable reduction.

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