30.4 A 370μW 5.5dB-NF BLE/BT5.0/IEEE 802.15.4-Compliant Receiver with >63dB Adjacent Channel Rejection at >2 Channels Offset in 22nm FDSOI

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Upcoming Internet-of-Things (IoT) applications require low-power multi-standard RF receiver (RX) front-ends. Interference rejection becomes increasingly important as ever more devices compete in the scarce low-GHz spectrum. Typically, low-power RXs do not possess very steep filtering [1-6]. On the other hand, very selective RXs – e.g. using analog FIR or Filtering-by-Aliasing [7] – have very high power consumption, not suitable for IoT applications. A recent Analog Finite-Impulse-Response (AFIR) filter [8] shows promising results to improve channel filtering. [8] uses a much lower FIR update rate than [7] to considerably reduce power consumption. This comes at the cost of a filter alias, but the inherent windowed integration sinc filtering mitigates this filter alias. Achieving low RX Noise Figure (NF), while improving selectivity is challenging at ultra-low power, where all blocks tend to contribute significantly to the total power consumption [1-6].

In this paper, a 370μW RX with very strong interference rejection exploiting AFIR filtering is presented. The RX employs a novel "windmill" divider architecture that provides 25%-duty-cycle clocks through a single gated LO buffer – at only 41μW. The programmable AFIR filter makes the RX compliant with multiple (IoT) standards in the 2.4GHz ISM band: Bluetooth Low Energy (BLE, 1Mb/s), Bluetooth 5.0 (BT5.0, 2Mb/s) and 802.15.4 (verified via 2Mb/s raw-data half-sine-shaped OQPSK to compare fairly to [3,5]).

Figure 30.4.1 shows the proposed zero-IF RX. The RF input is passed to a Low-Noise Transconductance Amplifier (LNTA). Low power consumption and NF are achieved by an inductively degenerated common-source LNTA utilizing a push-pull transconductor to double supply current efficiency [9]. A passive mixer downconverts the RF signal to baseband; where it is converted to voltage using a Transimpedance Amplifier (TIA). Channel filtering is implemented by an AFIR filter running at 16MHz for BLE and 32MHz for BT5.0 and 802.15.4. The AFIR filter significantly improves the channel selection compared to a conventional, e.g. 3rd-order Butterworth filter, and increases flexibility. Both 4.8GHz and 16MHz/32MHz clocks are provided externally, but all clock distribution and the 25%-duty-cycle LO divider are integrated. All filtering – including channel filtering – is performed in the analog domain, which significantly reduces the dynamic range and sampling-rate requirements on the subsequent Analog-to-Digital Converter (ADC).

Figure 30.4.2 shows the baseband channel filtering in detail. Highly selective channel filtering is achieved by a 32-tap AFIR filter similar to [8]. A 10bit transconductor Digital-to-Analog Converter (g_mDAC) is varied over time according to the FIR coefficients stored in the memory. During φ_i the input signal is integrated via the g_mDAC on capacitors C_i. Different time instances of the input signal are weighted differently and are integrated (summed) similarly as in a digital FIR filter. In this way, a very sharp filter response is obtained by a *single* transconductor, providing very high SNR for a given (analog) power consumption. After integration, the capacitor voltage is sampled to the output (φ_s). After sampling, the output is reset (φ_r), where φ_s and φ_r partially overlap to ensure that the parasitic capacitors of the measurement probe and PCB are also reset. The filter consists of two time-interleaved integration paths to double the integration time; thereby halving the filter bandwidth for a given output sample rate. The AFIR filter output is inherently sampled on C_i, which can be readily reused as the sampling capacitor of a low-power SAR ADC – eliminating the need for a buffer. The output common mode of the g_mDAC is set by a common-mode-feedback (CMFB) circuit. The g_mDAC is 5bit thermometer coded and 5bit binary coded for reduced mismatch and control-logic power consumption [8]. The FIR code is provided at 16MHz(1Mb/s) and 32MHz(2Mb/s) – resulting in filter aliases at integer multiples of 16MHz/32MHz. A TIA prefilter attenuates these AFIR aliases by about 46dB, allowing for 80dB filtering at the first alias. The AFIR filter consists of only switches, switched transconductors and digital logic – it directly benefits from technology scaling. Back-biasing is employed to compensate for differential offsets in the TIA.

In most IoT RXs, the mixer clock generation contributes significantly to total power consumption (e.g. one third in [4]). The proposed RX employs 25%-duty-cycle mixer clocks to downconvert a single-ended RF current to differential I/Q outputs. To minimize power consumption, a *single* logic gate converts input LO (50% duty-cycle at $2f_{in}$) to the output clock (25% duty-cycle at f_{in}). Figure 30.4.3 shows the proposed "windmill" 25%-duty-cycle frequency divider, indicating the rotating nature of the gate-enable signals E_x and outputs Q_x (x=1…4). It consists of 4 NORs acting as gated LO buffers (big). When enabled (E_x is low), they act as inverting buffers from LO to output. Two pairs of NORs act as latches (small) that enable the appropriate output. The operating principle for an output pulse Q_1 is as follows: Assuming that E_1 is low, an LO- low is passed to the output as a Q_1-high. The Q_1-high flips the E_2-E_4 latch activating the LO+ to Q_2 while disabling LO+ to Q_4. In short, the latches toggle the LO-, LO+ to Q_1/Q_3, Q_2/Q_4, respectively. The divider outputs directly drive the mixer switches – *no buffers* are required. Only the big gates are scaled to drive the mixer switches, all other gates are minimum size. In this way, very low power consumption is achieved while also realizing good phase noise and mismatch as only a single gate contributes to timing uncertainty. The windmill divider does not require additional start-up circuitry – eliminating possible start-up issues. RX NF degradation due to uncorrelated noise in the mixer is reduced by sharing the NOR top-PFET via nodes a and b [10]. In addition, since the PFET is shared, a single PFET is used to create two rising edges; resulting in reduced power consumption of the preceding buffer.

The RX is fabricated in 22nm FDSOI and is wire-bonded in a QFN package. It has an active area of 0.50mm^2. The chip has a power consumption of 370μW from a 700mV supply. All measurements are at maximum gain. Figure 30.4.4 shows the measured S_{11}, sensitivity, IIP3 and power-consumption breakdown. The S_{11} is <-15dB across the 2.4GHz ISM band. The sensitivity is measured for 0.1% BER, demodulating the received IQ signal using Matlab. The sensitivities are -99dBm (BLE), -96dBm (BT5.0) and -96.5dBm (802.15.4). The maximum variation of about 0.5dB is within the measurement error. The IIP3 in BLE mode is -7.5dBm for interferers at 4.01MHz and 7.98MHz offset frequencies. The power consumption is dominated by the LNTA to obtain a 5.5dB RX NF. The 25% divider consumes only 41μW; excluding the preceding buffer.

The measured adjacent-channel rejection (ACR) is shown in Fig. 30.4.5. The ACR is measured as follows: The wanted signal has an input power of sensitivity+3dB. The power of a modulated interferer (using the same standard) is swept until the 0.1% BER is reached. This measurement is performed for different blocker-offset frequencies. The ACR for BLE and BT5.0 is >65dB for frequency offsets of >3MHz and >6MHz, respectively. The filter alias is almost fully suppressed by the TIA prefilter as expected. The ACR of 802.15.4 is limited by the broadband TX spectrum, since it is not Gaussian filtered as in BLE/BT5.0. In comparison to prior art, the BLE ACR is improved by >27dB for frequency offsets >2MHz.

Figure 30.4.6 compares this work with state-of-the-art low-power RXs. This work achieves state-of-the-art NF and IIP3 while improving power consumption by a factor of 2 for an IoT RX with NF<6dB. The very strong ACR of >63dB at >2 channels offset without external filtering makes the RX ready for future IoT standards.

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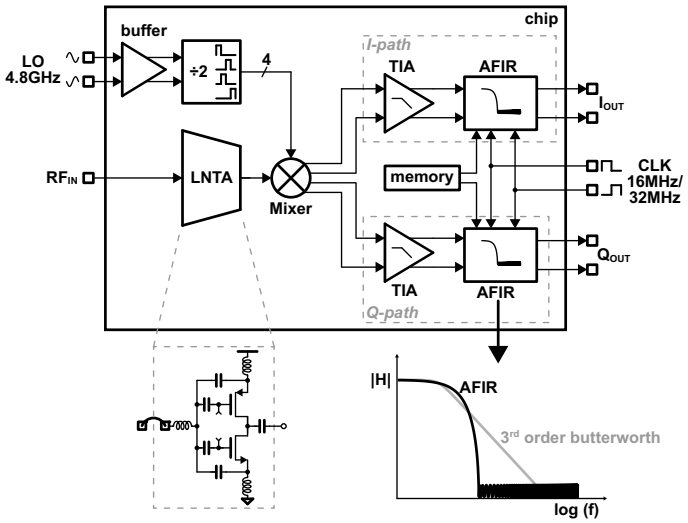

Figure 30.4.1: The 2.4GHz Internet-of-Things receiver architecture.

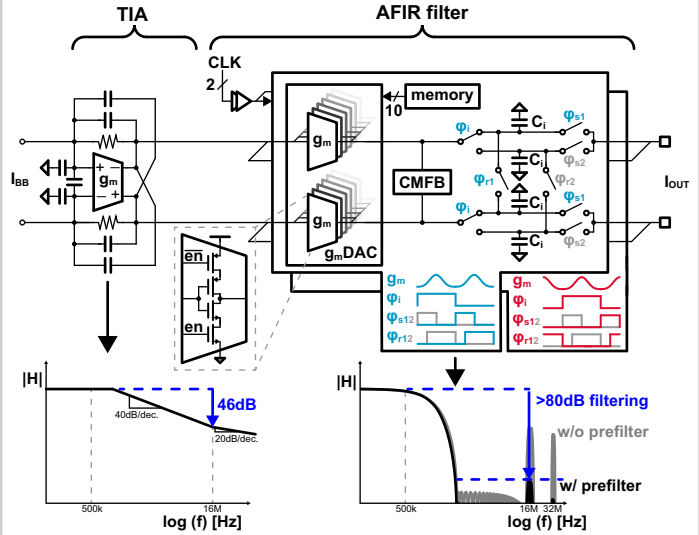

Figure 30.4.2: I-path RX base-band. Transimpedance Amplifier (TIA) and Analog FIR (AFIR) filter. The TIA provides prefiltering of the AFIR filter aliases.

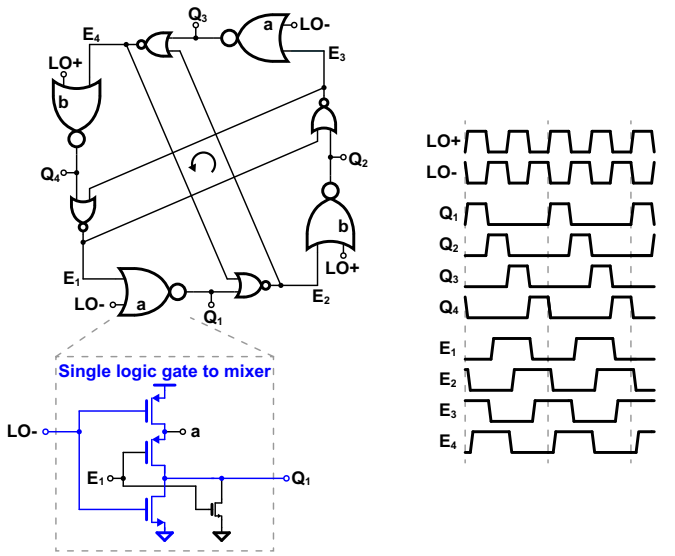

Figure 30.4.3: "Windmill" frequency divider including waveforms.

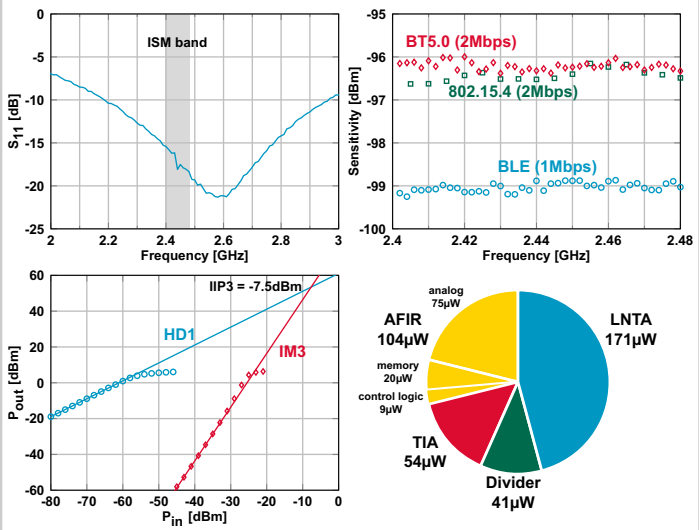

Figure 30.4.4: Measured S_{11}, Sensitivity, IIP3 (for Δf = 4.01MHz and $2\Delta f$ = 7.98MHz input tones) and power consumption breakdown for BLE (1Mb/s).

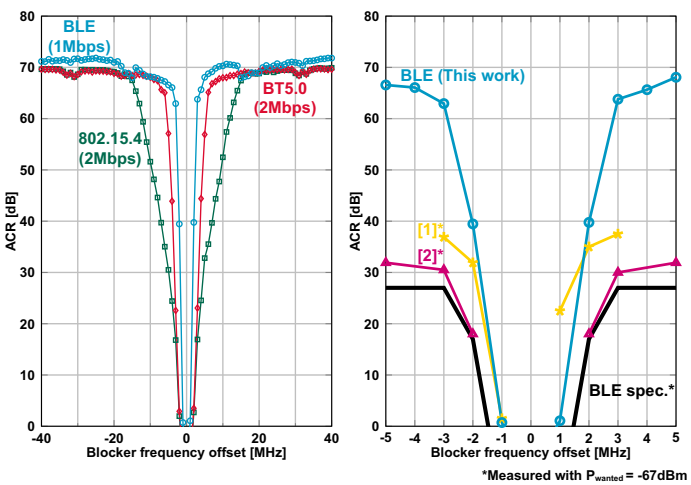

Figure 30.4.5: Measured adjacent-channel rejection (ACR) with modulated interferer and wanted signal at sensitivity +3dB. Across ISM band and close-in compared to prior art for BLE (1Mb/s).

	This Work			[1]	[2]		[3][h]	[6]	[4]
Standard	BLE	BT5.0	802.15.4[d]	BLE	BLE	BT5.0	802.15.4[d]	BLE	BLE
Data rate [Mbps]	1	2	2	1	1	2	2	1	1
On-chip Matching	Yes			Yes	Yes		No	Yes	Yes
P_{DC} [mW]	0.37	0.40	0.40	1.2[e]	1.1[e]	-	1.95[e]	1.7	0.7[e]
NF [dB]	5.5			6	5.9		6.1	8.5	5.2
Sensitivity [dBm]	-99[b]	-96[b]	-96.5[b]	-94	-95	-92	-91	-	-95.8
ACR 2nd/3rd channel[a]	39/63[b,c]	44/65[b,c]	52/67[b,c]	31/36[f]	18/30[f]	18/29.5[f]	24/35[f]	-	-
IIP3 [dBm]	-7.5			-	-	-	-	-6	-19.7[i]
Gain [dB]	61	57	57	68	-	-	-	57	47-72
Supply Voltage [V]	0.7			1	0.8		1	0.6&1.2	1
Active Area [mm²]	0.5			1.64[g]	0.8[g]		1.3[g]	0.22	0.7[g]
Technology	22nm FDSOI			65nm CMOS	40nm CMOS		40nm CMOS	65nm CMOS	40nm CMOS

[a]Channel spacing: BLE 1MHz; BT5.0 2MHz; 802.15.4 5MHz. [b]Demodulated using Matlab CPM demodulator (BLE, BT5.0) and MSK demodulator (802.15.4). [c]Measured with wanted signal at sensitivity +3dB. [d]Verified with 2Mbps raw data rate HS-OQPSK without de-spreading as in [3,5]. [e]Power consumption is estimated from power breakdown, e.g. w/o VCO/PLL. [f]Measured with wanted signal at -67dBm. [g]Area includes more than RX path. [h]Some specifications of this work are found in [5], this work is also compliant with BLE. [i]At minimal gain of 47dB.

Figure 30.4.6: Performance comparison with recently published IoT receivers.

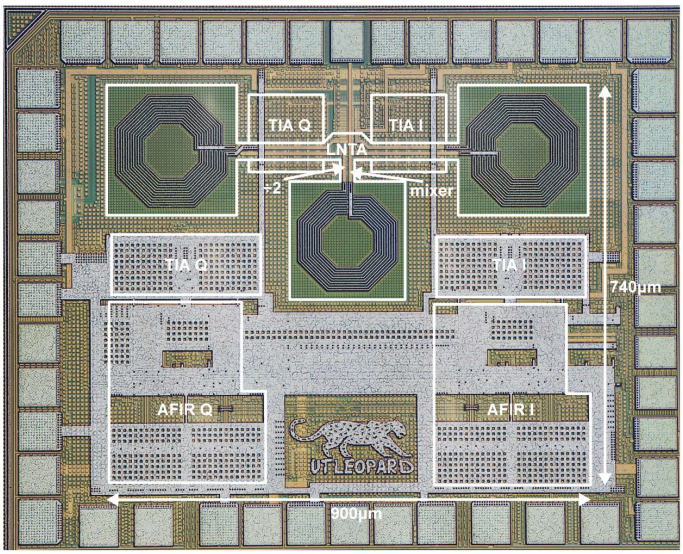

Figure 30.4.7: Die micrograph indicating major receiver blocks.

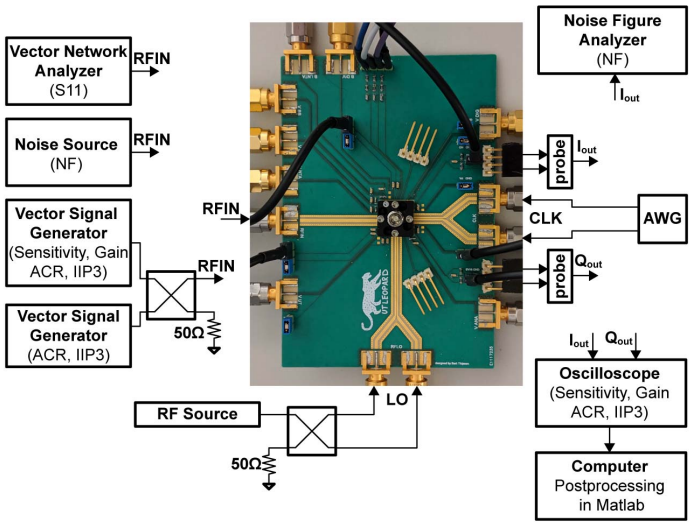

Figure 30.4.S1: Measurement setup.

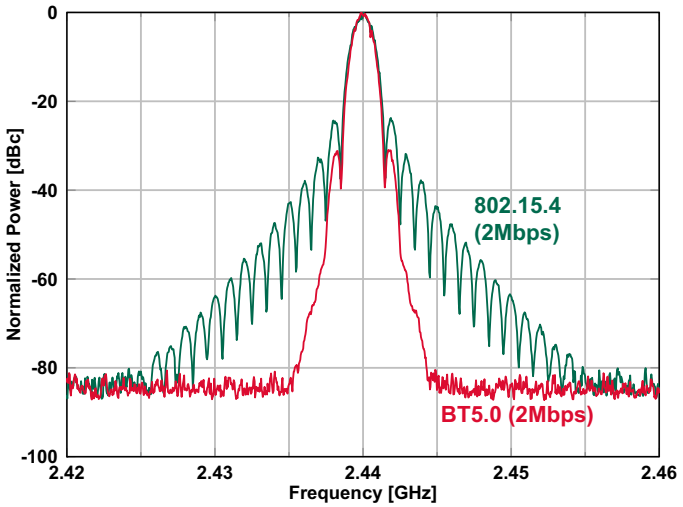

Figure 30.4.S2: Measured modulated blocker spectrum of BT5.0 (2Mb/s GFSK) and 802.15.4 (2Mb/s raw data rate HS-OQPSK). The wideband nature of the 802.15.4 blocker limits the ACR performance in Fig. 30.4.5.

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