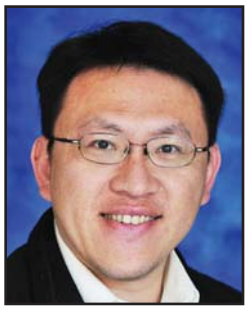
Session 16 Overview: *Computation in Memory*

MEMORY SUBCOMMITTEE



Session Chair:
Meng-Fan Chang
National Tsing Hua University
Hsinchu, Taiwan

Session Co-Chair:
Ru Huang
Peking University, Beijing, China

Session Moderator:
Seung-Jun Bae
Samsung, Hwaseong, Korea

Computation in memory (CIM) continues to diversify to cover various memory technologies using computations performed in different signal domains. This session covers CIM designs using ReRAM, eDRAM, and SRAM with computations in both analog and digital domains.

Paper 16.1 describes a high-performance 22nm ReRAM design using a hybrid-precision technique that supports up to an 8b-input and an 8b-weight MAC operations, while achieving 11.91TOPS/W for an 8b-input, 8b-weight and 14b-output, and 195.7TOPS/W for a 1b-input, 2b-weight and 4b-output. 16.2 describes the first 1T1C eDRAM design supporting analog 8b-input, 8b-weight and 8b-output computations at 4.76 TOPS/W in a 65nm technology. In 16.3 a 28nm SRAM CIM macro with up to 22.75TOPS/W for a 4b-input, 4b-weight and 12b-output and 94.31TOPS/W for a 8b-input, 8b-weight and 20b-output. 16.4 takes a different approach and focuses on an all-digital SRAM area-efficient CIM macro design achieving up to 89TOPS/W with 4b-input, 4b-weight and 16b-output.

2021 IEEE International Solid- State Circuits Conference (ISSCC) | 978-1-7281-9549-0/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISSCC42613.2021.9365967

9:15 AM

16.1 A 22nm 4Mb 8b-Precision ReRAM Computing-in-Memory Macro with 11.91 to 195.7TOPS/W for Tiny AI Edge Devices

Je-Min Hung, National Tsing Hua University, Hsinchu, Taiwan

In Paper 16.1, National Tsing Hua University presents a 22nm 4Mb 8b-Precision ReRAM CIM macro with 11.91 to 195.7TOPS/W for tiny AI edge devices.

9:23 AM

16.2 eDRAM-CIM: Compute-In-Memory Design with Reconfigurable Embedded-Dynamic-Memory Array Realizing Adaptive Data Converters and Charge-Domain Computing

Shanshan Xie, University of Texas, Austin, TX

In Paper 16.2, University of Texas at Austin shows an eDRAM-CIM design with reconfigurable embedded dynamic memory array realizing adaptive data converters and charge-domain computing.

9:31 AM

16.3 A 28nm 384kb 6T-SRAM Computation-in-Memory Macro with 8b Precision for AI Edge Chips

Jian-Wei Su, National Tsing Hua University, Hsinchu, Taiwan and Industrial Technology Research Institute, Hsinchu, Taiwan

In Paper 16.3, National Tsing Hua University presents a 28nm 384Kb 6T SRAM CIM macro with 8b precision for AI edge chips.

9:39 AM

16.4 An 89TOPS/W and 16.3TOPS/mm^2 All-Digital SRAM-Based Full-Precision Compute-In Memory Macro in 22nm for Machine-Learning Edge Applications

Yu-Der Chih, TSMC, Hsinchu, Taiwan

In Paper 16.4, TSMC introduces an 89 TOPS/W and 16.3 TOPS/mm^2 all-digital SRAM-based full-precision CIM macro in 22nm for edge machine-learning applications.