14.6 A 27W D2D Wireless Power Transfer System with Compact Single-Stage Regulated Class-E Architecture and Adaptive ZVS Control

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Compact and high-power bidirectional wireless power transfer (WPT) systems are desirable for mobile device-to-device (D2D) wireless fast charging. Prior WPT solutions [1-3] with integrated Class-D power amplifier (PA) provide relatively low output power (<10W). A Class-E PA has higher output power capability than a Class-D PA with the same input voltage. The 70W single-ended Class-E PA in [4] uses one additional bulky discrete MOSFET working as a tunable capacitor for impedance matching, achieving zero-voltage-switching (ZVS) and zero-voltage-derivative-switching (ZVDS) with 50% switching duty cycle across wide load and distance ranges. The 100W differential Class-E PA in [5] provides higher output power but requires a discrete impedance tuning network with 2 C_{BLOCK}'s, 3 R_{DC}'s, and 2 MOSFETs. These two solutions are well suited for pad-to-device wireless charging, but are hard to be embedded in a mobile phone. In addition, to regulate the PA output power, the supply voltage of the PA is tuned by a DC-DC converter in a conventional two-stage solution. In this work, we design a compact single-stage regulated Class-E architecture with adaptive ZVS control for D2D wireless fast charging.

Fig. 14.6.1 shows the highly-integrated single-stage regulated WPT transmitter (TX) structure that merges a DC-DC buck converter with a Class-E PA, saving one power inductor and one filtering capacitor. The off-chip Gallium-Nitride (GaN) switch M_G works at the LC tank resonant frequency f_o of 6.78MHz, while the integrated NMOS switches M_H and M_L work at 847.5kHz (1/8 of f_o) for improving the efficiency. To remove the bulky resonant tuning components, we set the ZVS point of M_G adaptively off the 50% duty cycle (D_E) point of the Class-E PA, to accommodate load and distance variations. Although off the D_E=50% operation point will result in higher voltage stress on M_G, it is designed to be lower than the drain-source breakdown voltage. Besides, M_G will be turned on right after the ZVS point, to reduce the reverse conduction time, thus improving the efficiency.

There are four working states for output regulation, as shown in Fig. 14.6.1(Bottom). The switches M_H and M_L together with the inductor L form the core of a buck converter. In the steady-state, volt-second balance of L mandates the average value of V_{SW2} to be equal to $D{\cdot}V_{IN2}$, with D being the duty ratio. The inductor also serves as the choke of the Class-E PA and has large value. The inductor current has small ripple and is approximated as a constant. In State-1, L is energized through the path of M_H-L-M_G. In State-2, the inductor current is in the freewheeling mode. In State-3 and State-4, the resonant tank is charged by the inductor current. Taking duty ratio D=0.8 as an example, the one-step regulated Class-E PA works in states 1→3→1→3→4 periodically.

Fig. 14.6.2(top) shows the overall design. The high-side driver of M_H is powered by a traditional bootstrap circuit, using one external diode and one external capacitor. The deadtime controller is a low-power digital circuit with good noise immunity and issues a firm initial deadtime after power-up reset. The bidirectional D2D wireless charging mode with the regulated Class-E architecture is configured in Fig. 14.6.2(bottom). In the rectifier mode, the multiplexer directly connects the comparator output to the GaN driver forming an active diode. When V_{SW3} is high, the GaN FET M_G is turned off, and the choke inductor L is energized. M_G will be turned on when V_{SW3} is lower than the ground.

Fig. 14.6.3 presents the adaptive ZVS controller and the GaN driver. The adaptive ZVS controller tracks the ZVS point, which changes with coil distance and load impedance. This ZVS tracking feature can reconfigure the Class-E PA into a Class-E rectifier. A push-pull comparator with HV-NMOS shielding is designed to detect the ZVS point of the V_{SW} node. As V_{SW} can reach as high as 70V, two 100V NMOS FETs are used to protect the 5V FETs in the comparator. Therefore, this HV comparator can directly sense the V_{SW} point without area-consuming resistor divider.

The M_G turn-off point is triggered by the rising edge of the external input 6.78MHz CLK signal. Also, a short positive pulse P_R is applied to M_{NR} to prevent the comparator from toggling incorrectly due to the induced ringing caused by the high di/dt of the parasitic inductance at the source of M_G. At the rising edge of the comparator output, which is the detected ZVS point of V_{SW2}, M_G is turned on. At the falling edge of the CLK signal, M_G will be turned on firmly to prevent it from being damaged when the resonant tuning circuit loses its ZVS state.

Driving the off-chip GaN FET must address the ringing issue caused by the bonding wire and PCB trace parasitic inductors. A conventional solution either uses gate resistance to damp the ringing, which will increase the rising and falling edge time and causes more power loss, or uses active gate driving, which needs complex circuits to generate the driving patterns. [6] uses an NMOS as the high-side switch in the GaN driver, as only NMOS is available in an enhancement-mode GaN process. Fig. 14.6.3(bottom) shows our GaN driver using a CMOS process, to reduce the parasitic inductance-induced ringing of the off-chip GaN FET. In this GaN driver, the NMOS high-side switch works as a current chock when the driver output voltage exceeds the NMOS threshold voltage, and a smaller size PMOS is used to pull up the voltage when the high-side NMOS is turned off. The current chock allows the driver to turn the GaN FET on fast within 2.8ns, while no overshoot or ringing occurs at the V_G rising edge. The parasitic inductance is different for different packages and PCB layouts. Therefore, the high-side NMOS has three tuning bits, which connects the body of the high-side NMOS to the source or to ground, to control the threshold of the high-side choke NMOS. For larger parasitic inductance, we can increase the threshold voltage of the high-side choke NMOS and vice versa.

Fig. 14.6.4 shows the digital deadtime controller for the switching regulation part. The digital control loop controls two complementary 6-bit capacitor delay lines for the V_X leading and trailing edges. The unit capacitance is 13fF. The total capacitance of one capacitor array is 0.8pF. It occupies a small chip area and consumes very low power. The initial delay at the system power-up is set to half of the full delay range. The sample and hold circuits (SH) sample the V_X and V_{PGND} signals. Here, V_X and V_{PGND} can assume negative values. However, a conventional SH has difficulty in storing a negative voltage. Thus, the SH uses a local charge pump that generates a negative voltage to turn off the sampling switch. Subsequently, the differential dynamic comparator compares V_{DSL}=V_X–V_{PGND} with the reference voltage to detect the body diode working condition of the low-side NMOS M_L. If the comparator output is '00', M_L is working in body diode conduction mode, and the control loop will reduce the delay. If the comparator output is '11', shoot-through current occurs between the high- and low-side switches, and the control loop will increase the delay. The optimal deadtime is obtained if the comparator output is '10', and the digital control loop will hold the counter.

A prototype of our design was fabricated in a 0.18μm BCD-on-SOI process. M_G is an eGaN FET EPC2007C and the choke inductor is 5.6μH. The regulated PA delivers a maximum 27W output power at V_{IN}=10V and V_{OUT}=48V, with 63.3% end-to-end (E2E) efficiency over a coil distance of 19mm. The maximum E2E efficiency of 80% is achieved at 15mm coil distance with V_{OUT}=17V. Fig. 14.6.5 shows the measured current waveform acquired by a de-skewed current probe. Fig. 14.6.5(bottom) shows the measured V_X of which the leading and trailing edge dead time is controlled adaptively. As shown in Fig. 14.6.4(bottom), the regulated differential PA by using two chips can deliver 45W output power over a coil distance of 19mm. Fig. 14.6.6 is a table that compares the output power and system E2E efficiency of our design with state-of-the-art designs under different conditions. Our one-step regulated PA has the highest efficiency and output power among all single-stage regulated PAs. Fig. 14.6.7 shows the chip micrograph and the die area is 2.77mm^2.

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[4] C. Yeh *et al.*, "A 70W and 90% GaN-Based Class-E Wireless-Power-Transfer System with Automatic-Matching-Point-Search Control for Zero-Voltage Switching and Zero-Voltage-Derivative Switching," in *IEEE International Solid - State Circuits Conference (ISSCC)*, Feb. 2018, pp. 138–140.
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[6] M. Kaufmann and B. Wicht, "A Monolithic GaN-IC With Integrated Control Loop for 400-V Offline Buck Operation Achieving 95.6% Peak Efficiency," in *IEEE* Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3169-3178, Dec. 2020.

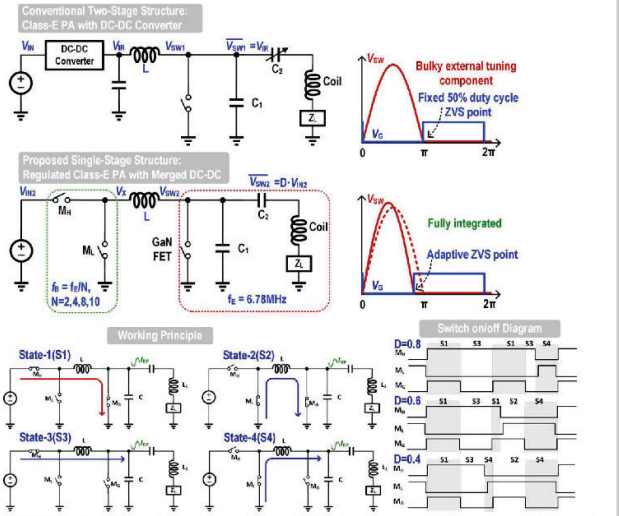


Figure 14.6.1: Traditional two-stage Class-E PA structure, and the proposed one-step regulated Class-E PA structure and its working principle.

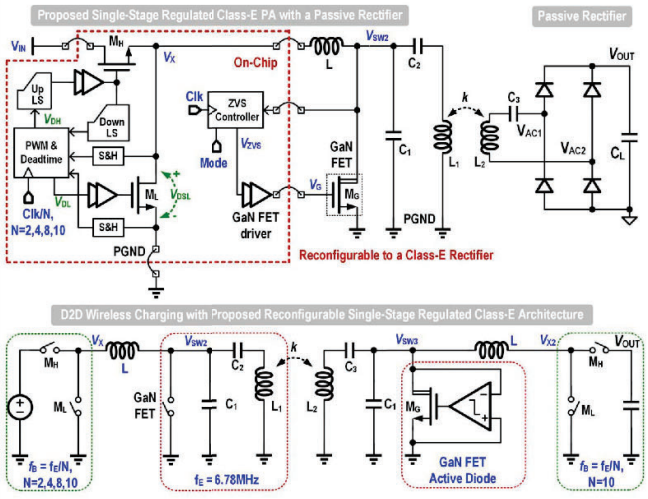


Figure 14.6.2: Block diagram and the diagram of D2D working mode.

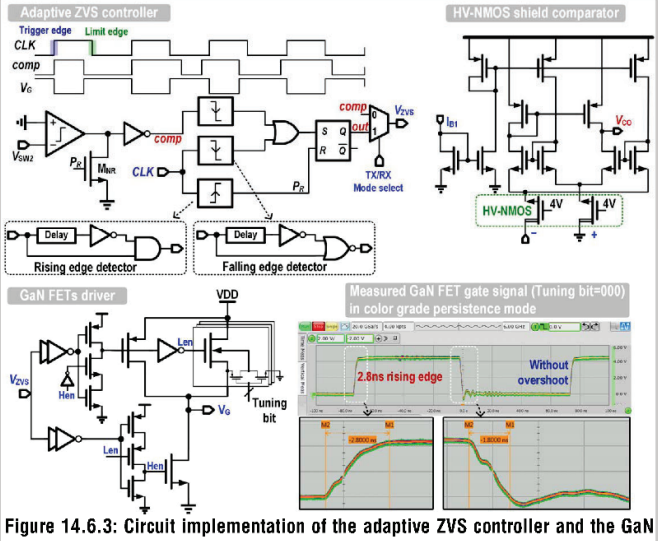


Figure 14.6.3: Circuit implementation of the adaptive ZVS controller and the GaN driver; and the measured GaN FET gate signal under 15W output power.

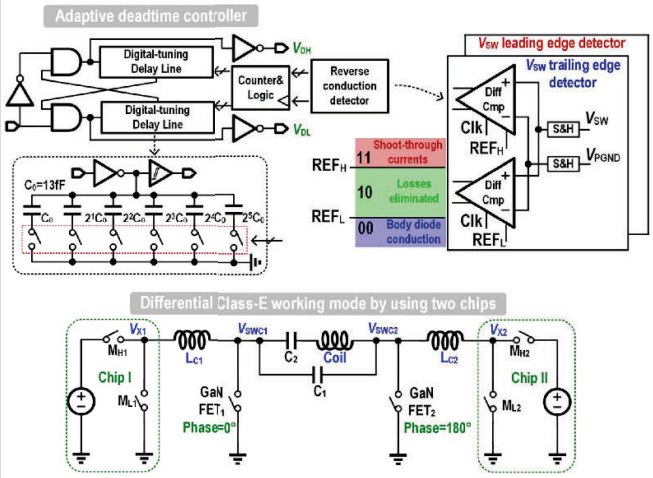


Figure 14.6.4: Circuit implementation of the adaptive deadtime controller which uses four differential comparators and four sample and hold circuits (top), and the diagram of differential Class-E working mode by using two chips (bottom).

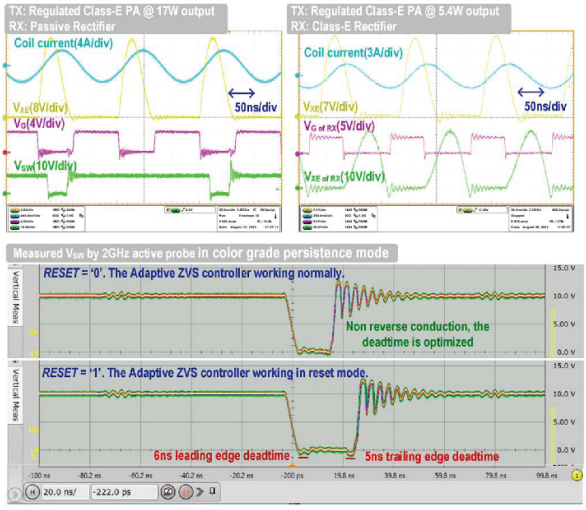
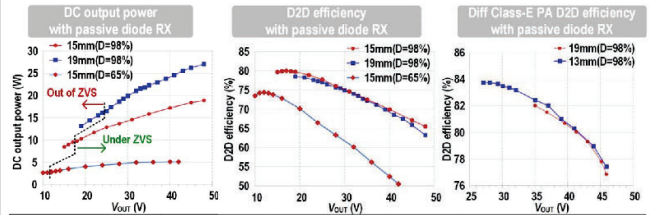


Figure 14.6.5: Measured waveforms of PA with passive diode rectifier and PA with Class-E rectifier; and measured V_{SW} waveform under 0.9A input current.



	JSSC'21 [2]	ISSCC'19 [5]	JSSC'19 [1]	ISSCC'18 [4]	TCAS-I'21 [3]	This work		
Process	0.25μm	0.5μm	0.35μm	0.5μm	0.35μm	0.18μm		
Type	Regualted Class-D	Diff Class-E	Bi-Dir Class-D	Class-E	Regulated Class-D	Regulated Class-E	Reg. PA & Class-E RX	Reg. Diff Class-E
Chip Area [mm^2]	1.61	3.15	3.92	3.78	3.53	2.77		
V_{IN} [V]	4.2	40*	2.5-4.5	40*	15	10		
V_{OUT} [V]	5	N.A.	2.5-4.5	N.A.	12	10-48	5-10	25-46
Operation frequency [MHz]	6.78	13.56	6.78	6.78	6.78	6.78		
Peak DC output power [W]	0.4	100	2.74	70	7.3	27	6.5	45
Peak E2E Efficiency [%]	71.5	91	77.2	90	57.3	80	74.6	83.7
Regulated output	YES	NO	NO	NO	YES	YES	YES	YES
External compnent of PA	1C	5C 4L 2GaN 2MOSFET	1C	3C 2L 1GaN 1MOSFET	3C 2L	2C 1L 1GaN	2C 1L 1GaN	4C 2L 2GaN

* Estimated from testing results

Figure 14.6.6: Comparison with the state-of-the-art; measured D2D efficiency and DC output power under different output voltages and coil distances.

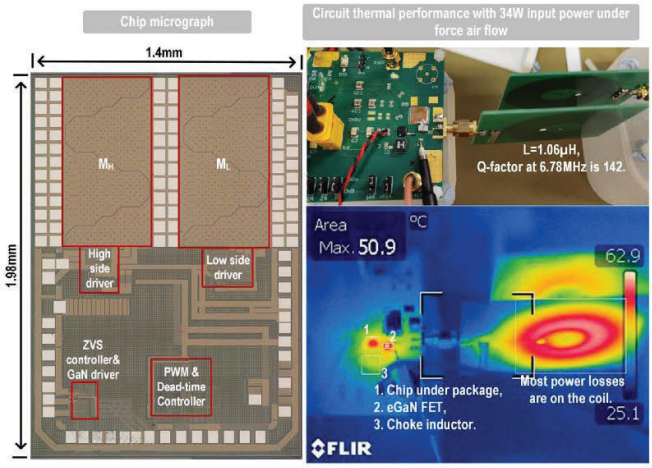


Figure 14.6.7: Chip micrograph (left), circuit thermal performance (right).