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31.2 A 121.4dB DR, -109.8dB THD+N Capacitively-Coupled Chopper Class-D Audio Amplifier

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Class-D amplifiers (CDAs) are often used in audio applications due to their superior power efficiency. Due to the sensitivity of the human ear, a large dynamic range (DR) is desired, and audio DACs with up to 130dB DR are commercially available [1]. However, the DR of the CDAs they drive is typically much lower [2-4], mainly due to the thermal noise introduced by the input resistors of their resistive feedback networks. Reducing this resistance is difficult, as it reduces the CDA's input impedance and increases the required loop-filter capacitance. Alternatively, the CDA could be configured as a capacitively coupled chopper amplifier (CCCA), whose capacitive feedback network could then achieve low noise without reducing input impedance. However, the large PWM component present at its output would then saturate its input stage. By exploiting the inherent PWM filtering present in a feedback-after-LC architecture, this paper presents a capacitively coupled chopper CDA, resulting in significantly improved DR and THD+N. The prototype achieves 8μV_{RMS} of integrated output noise (A-weighted), a 121.4dB DR, and −109.8dB THD+N while delivering a maximum of 15/26W into an 8/4Ω load with 93%/88% efficiency.

A simplified single-ended block diagram of the CDA is shown in Fig. 31.2.1 (top). It employs a feedback-after-LC architecture, in which LC-filter nonlinearity is suppressed by the loop gain. An inner feedback path consisting of a 1st-order LPF placed around the output stage compensates for LC filter phase-shift and ensures stability even in the presence of LC filter spread [3]. In this work, a capacitive feedback network (C_{IN} and C_{FB}) is used to establish CDA gain (8×). The amplifier's input stage can then be configured as a CCCA, whose gain (C_{IN}/C_{GAIN}=16×) attenuates the noise of the loop filter by 24dB. Since the LC filter (L=3.3μH, C=1μF, f_{LC}=88kHz) suppresses most of the PWM content produced by the output stage around multiples of f_{PWM}=4.2MHz, the CCCA can handle the error signal (V_{IN}-V_{FB}/8) in a linear fashion, as shown in Fig. 31.2.1 (bottom).

Chopping mitigates the mismatch in the capacitive feedback network that would otherwise limit the PSRR of the CDA. The LC filter suppresses intermodulation between the chopping (f_{CHOP}) and PWM (f_{PWM}) frequencies and their harmonics. Nevertheless, since chopping demodulates frequency content from even multiples of f_{CHOP} to baseband, f_{CHOP} (=200kHz) is set to an odd (21) sub-harmonic of f_{PWM} so that residual intermodulation products will occur around f_{CHOP} and its harmonics, thus far above the audio band [5]. Due to the non-linearity of the chopper switches and the CCCA's finite slew rate, chopping transitions will also cause nonlinear glitches, and thus distortion, at the CCCA's output. To maintain linearity, these glitches are blocked by a dead-band (DB) switch [5]. Its periodic time-varying action, however, will fold wideband noise from the CCCA, V_{IN}, and V_{FB} to the baseband. Therefore, the DB duration (25ns) is made only slightly longer than the CCCA's settling time. To ensure good tracking over PVT, the DB is generated by an RC delay, and the same type of resistor is used in the CCCA's constant-g_m biasing circuit. All other timing signals, including f_{CHOP} and f_{PWM}, are derived from an on-chip RC oscillator (trimmed for 4.2MHz f_{PWM}).

Figure 31.2.2 shows a schematic of the CCCA. It consists of a 2-stage Miller-compensated opamp in a capacitive feedback network. To mitigate 1/*f* noise, the 1st stage of the CCCA is chopped. The CDA's input (V_{IN}) and feedback (V_{FB}) signals drive C_{IN} and C_{FB} via choppers CH_{IN} and CH_{FB}, respectively. C_{IN} (3pF) is chosen such that the parasitic capacitance at the virtual ground (V_X) of the opamp does not significantly boost its input-referred noise. The DC level at V_X is set by a duty-cycled resistor R_{DC} (250MΩ) to be equal to the CCCA's output CM voltage (0.9V).

In contrast to most CCCA prior arts, which were intended for amplifying millivolt-level signals, the CCCA in this work must handle much larger (14.4V peak) signals from the CDA output via CH_{FB} and still ensure good linearity. As shown in Fig. 31.2.3, CH_{FB} is realized with back-to-back LDMOS devices. Level-shifters translate the chopping clock Φ_{CH} from the low-voltage (LV, 1.8V) domain to the 14.4V domain, and their outputs are applied to switch drivers, which are powered by locally regulated bootstrap supplies (V_{REG1-4}) derived from the output (V_{CP}) of a shared on-chip charge pump to create an on-V_{GS} of ~4V [4]. The use of deadbanding blocks the signal-dependent delay of the level shifters (~3ns), which would otherwise lead to distortion.

Since both V_{IN} and V_{FB} can swing rail-to-rail, the timing skew (Δt) between CH_{FB} and CH_{IN} clocks caused by the level shifters would cause voltage pulses of up to ~2V_{DD} at the virtual ground (V_X) of the CCCA (Fig. 31.2.2), which would overstress its input devices. Moreover, larger glitches (up to several volts) could occur when CH_{FB} flips, in case R_{ON} of CH_{IN} ($R_{ON,IN}$) is much higher than that of CH_{FB} ($R_{ON,FB}$). Ideally, $R_{ON,IN}$ should be ~8× (=C_{IN}/C_{FB}) lower than $R_{ON,FB}$ to avoid these glitches. However, this is difficult because, in the chosen process, the LDMOS devices in CH_{FB} have a fixed length and can contribute significant 1/*f* noise compared to their LV counterparts. Therefore, they are sized much wider for low 1/*f* noise, resulting in a low $R_{ON,FB}$ (11Ω). Although $R_{ON,IN}$ could be sized accordingly to 11Ω/8, this would greatly increase the required area of the switches and their gate bootstrap capacitors (needed to make R_{ON} signal-independent for high linearity). Clamps could be used at V_X to restrict the pulses and glitches, but when activated, they inject charge into V_X, offsetting it by up to ~V_{DD}, which would saturate the CCCA. To address the timing skew, as shown in Fig. 31.2.2, a level-shifter replica timing-skew-correction circuit is added to align the high-voltage (HV) and LV chopper clocks. To resolve large glitches due to the imbalance between $R_{ON,IN}$ and $R_{ON,HV}$, a resistor R_{HV} is added in series with C_{FB}, which is set to 2.4kΩ (~8×$R_{ON,IN}$) and has a negligible thermal and 1/*f* noise contribution. The remaining glitches (due to the residual timing and impedance mismatch between the LV input and HV feedback paths) are kept well below V_{DD} (<900mV peak-to-peak differential) over PVT and are blocked by the DB switches.

Due to the large voltage excursions experienced by the CH_{FB} switches during chopping transitions, the switch drivers must be carefully designed to avoid cross-conduction. An example of such a transition is highlighted in Fig. 31.2.3, where some terminals of the CH_{FB} switches M_{1-3} experience large voltage excursions, whose dV/dt is set by the R_{ON} of the pull-up PMOS device (M_P) used to drive M_1 [6]. Parasitic coupling through the C_{GD} of M_3 could then turn it on due to the IR drop across its pull-down NMOS (M_N), thus creating a low impedance path between V_{FB+} and V_{FB-}. Due to parasitic inductance of the bond wires connecting CH_{FB} to the load, the resulting current pulses can cause significant ringing at nodes $V_{FB+,INT}$ and $V_{FB-,INT}$ (up to several volts, depending on driver design and L_{BOND}), stressing the connected switches and their drivers, and exacerbating glitches at the virtual ground. To minimize such events, the R_{ON} of the NMOS pull-down transistors (e.g., M_N) must be made lower than that of their PMOS pull-up counterparts (e.g., M_P) by at least a factor of V_{REG}/V_{TH} [6]. In this work, R_{ON} of M_N is chosen to be 7× lower than that of M_P to ensure robustness across PVT.

Prototyped in a 180nm BCD process, the CDA occupies 7mm², Fig. 31.2.7. Its audio performance is measured using an APx555 analyzer. Figure 31.2.4 (top) shows the measured FFT spectrum while the CDA delivers 1W into an 8Ω load, achieving a THD+N of -109.6dB. With a -80dBFS output, an SNR of 41.4dB is achieved, which corresponds to a DR of 121.4dB, Fig. 31.2.4 (bottom). The measured integrated output noise is 8μV_{RMS} after A-weighting. Figure 31.2.5 (top) shows the measured THD+N across output power for 8Ω and 4Ω loads, resulting in a peak THD+N of −109.6dB and −109.8dB, respectively. As shown, the noise floor is 10dB lower than that obtained with a pair of 20kΩ input resistors, as are often used in resistive CDAs [2]. Figure 31.2.5 (bottom) shows the measured THD+N vs. input frequency. The CDA consumes a quiescent current of 9mA and can deliver a maximum of 15/26 W into an 8/4Ω load (measured at 10% THD) with a peak efficiency of 93%/88%. Figure 31.2.6 summarizes the performance of this work and compares it with state-of-the-art HV CDAs. Among the CDAs in Fig. 31.2.6, this is the only one to employ a capacitively-coupled chopper topology, with 2.4× lower integrated output noise, 5.9dB higher DR, 2.5dB better THD+N, and a competitive PSRR.

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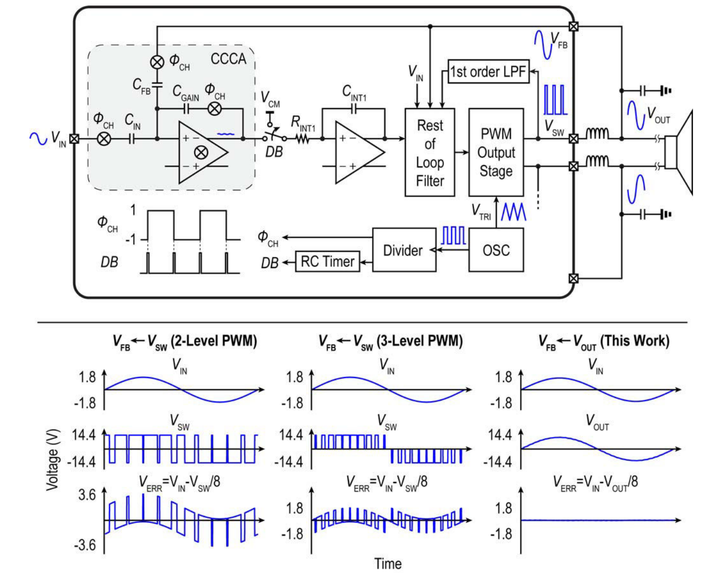

Figure 31.2.1: (Top) Architecture of the proposed capacitively-coupled chopper CDA, (bottom) error-signal waveform with V_{FB} taken from V_{SW} or V_{OUT}.

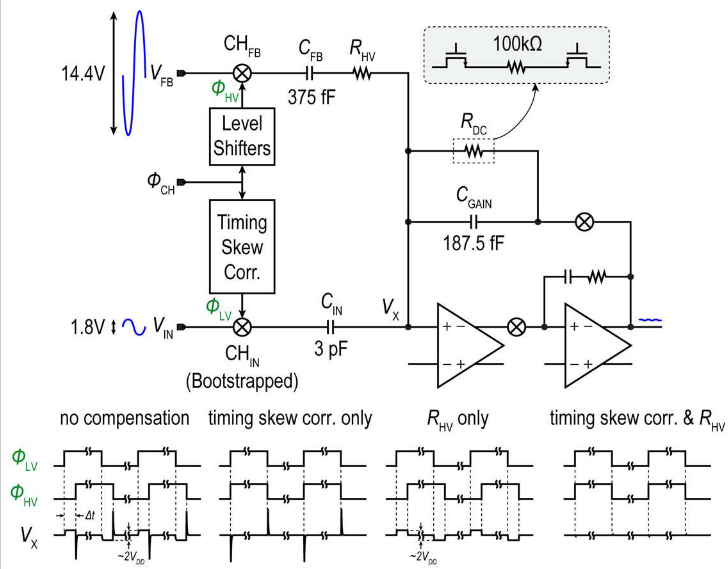

Figure 31.2.2: Schematic of the CCCA and the virtual-ground waveform with/without timing skew correction and/or impedance balancing (R_{HV}).

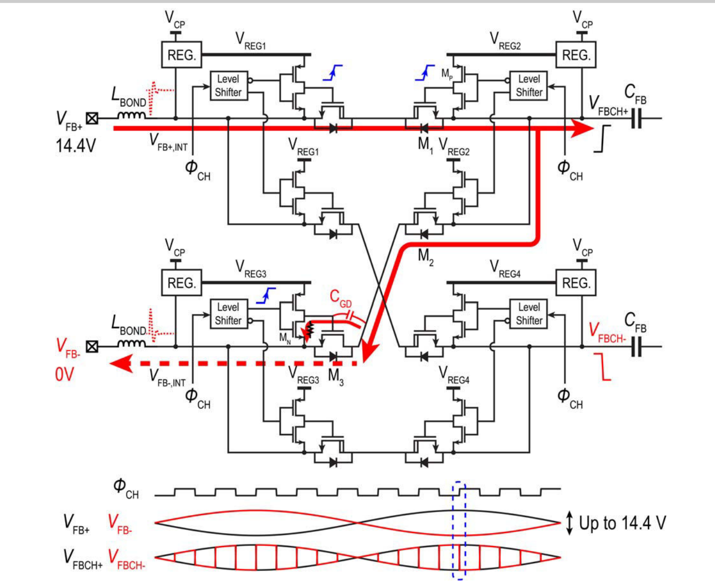

Figure 31.2.3: High-voltage chopper (CH_{FB}) schematic and relevant transients during the highlighted chopping event.

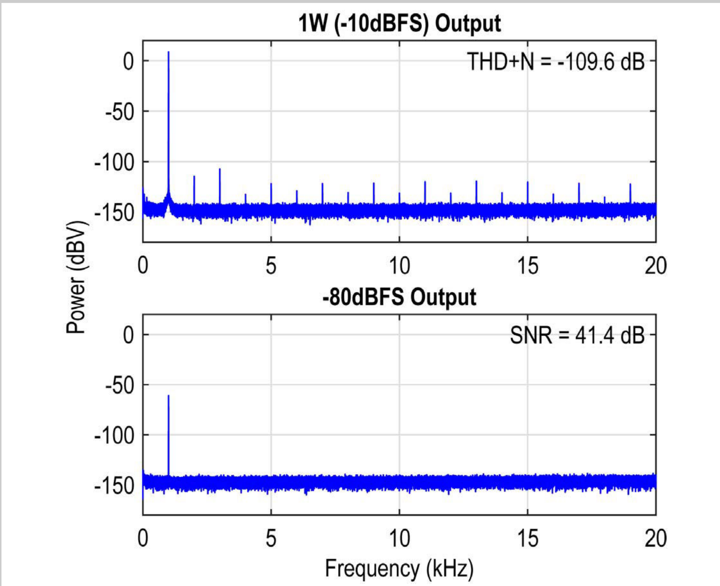

Figure 31.2.4: Measured output spectra when the CDA delivers (top) 1W (i.e., −10dBFS) and (bottom) −80dBFS to an 8Ω load.

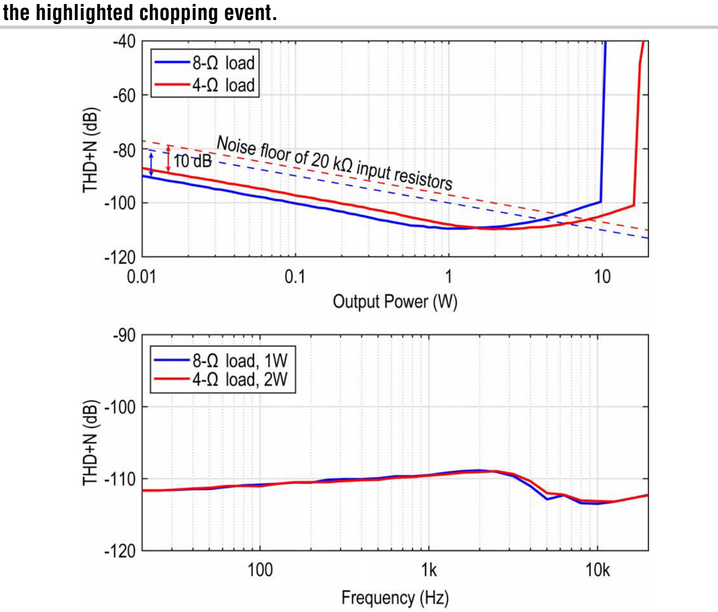

Figure 31.2.5: Measured THD+N (top) across output power for a 1kHz input and (bottom) across input frequency.

	This Work	TPA3255 [2]	Zhang VLSI'21	Karmakar ISSCC'20	Cope ISSCC'18	Schinkel JSSC'17
Process	**180 nm BCD**	-	180 nm BCD	180 nm BCD	180 nm BCD	130 nm BCD
Architecture	**Analog-In**	Analog-In	Analog-In	Analog-In	Digital-In	Digital-In
Feedback Network	**Capacitive**	Resistive	Resistive	Resistive	Resistive	Resistive
Supply (V)	**14.4**	51	14.4	14.4	8~20	14/25
Area (mm^2)	**7**	-	6	4.8	4.3	-
R_{LOAD} (Ω)	**8/4**	4	8/4	4	8	4
$P_{OUT,MAX}$ (W)	**15/26**	315	12/21	28	20	80
Efficiency	**93%/88%**	~90%**	91%/87%	91%	90%	>90%
I_Q / Channel (mA)	**9**	24	8	17	21	12
THD+N (dB)	**-109.6/-109.8**	-84	-107.1/-105.6	-102.2	-97.7	-88.6
DR	**121.4**	113	110*	109	115.5	115
A-wt. Output Noise (μV_{RMS})	**8**	85	-	31	20	19/34
PSRR (dB) (Frequency/Hz)	**89~71 (20~20k)**	>65 dB -	-	70~62 (20~20k)	80~50 (20~20k)	90~60** (20~20k)

*SNR number used
**Estimated from graph

Figure 31.2.6: Performance summary and comparison to prior art.

31

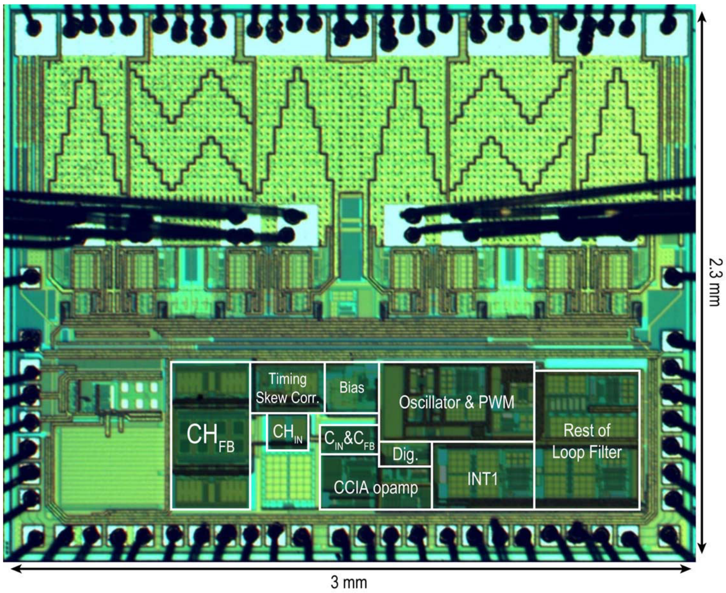

Figure 31.2.7: Die micrograph.