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A Receiver Architecture for Devices in Wireless Body Area Networks

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***Abstract*—A receiver architecture suitable for devices in wireless body area networks is presented. Such devices require minimum physical size and power consumption. To achieve this the receiver should therefore be fully integrated in state-of-the-art CMOS technology, and size and power consumption must be carefully considered at all levels of design. The chosen modulation is frequency shift keying, for which transmitters can be realized with high efficiency and low spurious emissions. A direct-conversion receiver architecture is used to achieve minimum power consumption and a modulation index equal to two is chosen, creating a mid-channel notch in the modulated signal. A tailored demodulation structure has been designed to make the digital baseband compact and low power. To increase sensitivity it has been designed to interface with an analog decoder. Implementation in the analog domain minimizes the decoder power consumption. Antenna design and wave propagation are taken into account via simulations with phantoms. The 2.45 GHz ISM band was chosen as a good compromise between antenna size and link loss. An ultra-low power medium access scheme has been designed, which is used both for system evaluation and for assisting system design choices. Receiver blocks have been fabricated in 65-nm CMOS, and an RF front-end and an analog-to-digital converter have been measured. Simulations of the complete baseband have been performed, investigating impairments due to 1/f noise, frequency and time offsets.**

***Index Terms*—Body sensor networks, CMOS integrated circuits, Low power electronics, Receivers, System-on-a-chip**

I. Introduction

There are numerous applications for ultra-low power wireless communication. For instance, it can benefit such different areas as health care [1] and smart buildings [2], [3]. To achieve ultra-low power consumption it is important to combine low-power transceiver circuits with optimized communication protocols. In medical implants this is critical since the battery cannot be replaced and must last the product lifetime, and the smaller the size of the implant the more comfortable for the patient. In some cases it is even possible to have a battery-less system using energy scavenging or remote powering [4]. In other applications like entertainment and smart buildings not only the small size, but also the reduced cost that comes with smaller batteries may be a key enabler.

The ultra-low power consumption limits the average data rate and the distance between receiver and transmitter. This is mainly due to the minimum transmitted energy per information bit needed to obtain reliable communication over a certain distance, but also due to the difficulty of realizing a low power receiver with good performance.

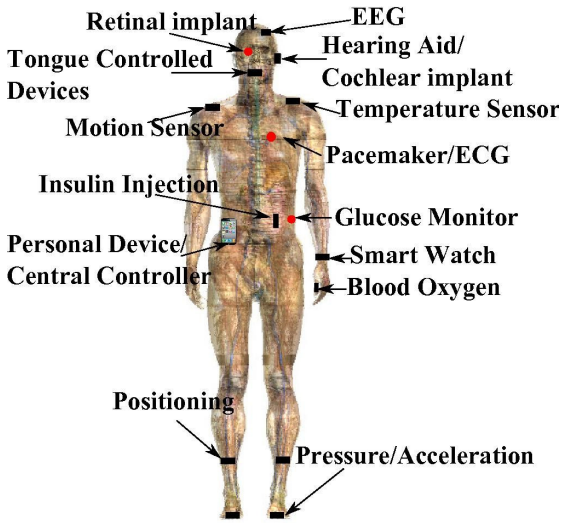


Fig. 1. WBAN with devices and sensors on a human phantom [20]. On-body devices/sensors are shown as black rectangles, and implantable as red circles.

An important application for ultra-low power radios is wireless body area networks (WBANs). Devices carried by a person then communicate wirelessly between different parts of the body, see Fig. 1. The devices could be medical implants like pacemakers or hearing aids, sensors for monitoring heart, glucose level, acceleration or temperature, as well as more generic devices for presentation, storage and communication of

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data [5], [6]. The distance of communication is in this case short, and the required data-rates are limited. However, although the distance is limited to a couple of meters, substantial attenuation of the signal may still occur when the receiver and transmitter are located on opposite sides of the body. It is therefore important to investigate the wave propagation carefully when choosing the frequency band and deciding the radio link parameters. It is also important to take interference in the frequency band into account, so that a receiver with adequate selectivity and linearity can be employed.

To minimize the size of the radio transceiver it should be realized as a single chip in nanometer CMOS technology. This will also minimize the cost when fabricated in large volumes, which is important if each person will carry several WBAN devices. The main benefits of nanometer CMOS are the low cost for implementing digital functions, and the high speed of devices that allows RF circuits to operate in weak inversion with extremely low power consumption. In addition, reaching very low total power consumption means designing a medium access (MAC) protocol tailored not only to the application requirements, but also to the particular node architecture used and to the energy characteristics of the circuits.

WBAN is a topic of high interest to both academia and companies. State-of-the art is quickly advancing, and new standards are being drafted in IEEE 802.15.6 and IEEE 802.15.4. While delivering robust performance, generally power consumption of the standardized radios is too high, typically 50 to 100 nJ/bit [1]. On the other hand, there are systems developed by universities, which use very simple and low power modulation techniques like on-off keying (OOK), achieving very low energies near 1 nJ/bit [7]. There are, of course, several other parameters that must be considered to make a fair comparison, such as communication distance (link loss) and robustness to interference. For instance the system in [4] reaches 0.33 nJ/bit, but it is tailored for neural sensors, which only need to communicate through the skull bone and fat. There are also companies developing proprietary solutions for different applications. In [8] a system operating in the 400-MHz MICS band is described, intended for medical implants like pacemakers and camera pills. The MICS transceiver ZL70102 uses 2FSK or 4FSK modulation and is implemented in 0.18-µm CMOS. To save power it features an ultra-low power duty-cycled wake-up receiver operating in the 2.45 GHz ISM band, which periodically sniffs for a wakeup signal. By using the 2.45 GHz band the wake-up signal can be transmitted with high power without violating the regulatory requirements. The sensitivity requirements of the wakeup receiver can then be relaxed, reducing its power consumption. By using the main radio only for a very small part of the time the system can then achieve ultra-low power consumption. The power consumption of the main radio is less than 5mA from a supply voltage between 2.1 and 3.5 V, for a maximum raw data rate of 800 kbit/s. Another duty-cycled 2.4 GHz wake-up receiver is described in [9]. To further reduce power consumption we suggest using a wake-up receiver that can detect different addresses, so that it will only wake up the main receiver if it is addressed.

In this paper we present a receiver architecture for WBAN applications, suitable for integration in nanometer CMOS. The different parts have been simulated and/or measured in 65-nm technology. By choosing FSK modulation a simple transmitter with high efficiency and low spurious emissions can be realized. For the receiver a direct-conversion architecture is employed, which has benefits in power consumption but problems with DC-offsets and 1/f noise. By tailoring the frequency deviation of the FSK modulation, matched filters with DC-notches can be used for demodulation, eliminating DC-offsets and suppressing 1/f noise. The 2.45 GHz ISM band is targeted, and since this is a popular band for wireless communication systems, immunity to interfering signals is critical. To address this continuous-time delta-sigma analog-to-digital converters (ADCs) are used, providing an attractive dynamic-range power trade-off and inherent anti-alias filtering. To further improve linearity, the ADCs are preceded by mixers with passive output filtering. High selectivity is obtained by sharp filtering in the digital domain, and by using a low phase noise LC-oscillator for the local oscillator. A decoder is used to increase the receiver sensitivity, and to reduce the power consumption overhead an analog implementation is proposed. The targeted power consumption is less than 1 mW in active mode for both receiver and transmitter, for a raw data rate of 250 kbit/s. The targeted receiver sensitivity is -92 dBm at 250 kbit/s and -97 dBm at 125 kbit/s at bit error rate (BER) .001. According to our wave propagation simulations this will allow communication in the difficult case where devices are located in opposite ears. The transmitted power required is -7 dBm, which can be obtained from a transmitter with a 1 mW total power consumption budget.

This paper is organized as follows. Section II presents the receiver architecture in more detail, section III describes the circuit design for the different parts of the receiver, and section IV shows the results of simulations and measurements.

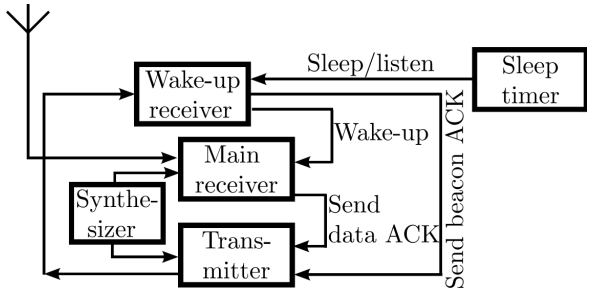


Fig. 2. Device architecture block diagram.

II. Receiver Architecture

The wireless communication part of a body area network device is shown in Fig. 2. It is important to consider the implications to the overall system when choosing receiver architecture. For instance, the choice of modulation will have a

dramatic impact on transmitter complexity and efficiency, and the sensitivity of the receiver will impact the required transmit output power. Phase noise and spectral purity of the frequency synthesizer will limit receiver selectivity. In low-traffic scenarios the power consumption and sensitivity of the wake-up receiver may be even more important to the system performance than that of the main transceiver.

The targeted total power consumption is 1 mW in active mode, when either receiver or transmitter is operated. To avoid interference they will not operate simultaneously. The transmitter will generate a frequency modulated signal directly in the frequency synthesizer, a signal with continuous low-pass filtered phase resulting in relatively low spurious emissions. Since the signal is constant envelope the PA does not have to be linear and can thereby be very efficient. For instance a class-D PA based on CMOS inverters can be used. The targeted power consumption of the frequency synthesizer is 500 µW, leaving 500 µW for the PA. Assuming a 40% efficient class-D PA, the output power will be 200 µW, i.e. -7 dBm. The total transmitter efficiency will then be 20%, which is in line with highest numbers reported for BFSK transmitters [10]. It should be noted, however, that the output power level in this work is 10 dB higher than in [10], which allows a PLL frequency synthesizer in the power budget, while still achieving state-of-the-art transmitter efficiency.

To complete the design of the ultra-low power communication system a medium access scheme is tailored to the device configuration, shown in Fig. 2. The developed scheme, called DCW-MAC, is based on duty-cycled medium access and low-power wake-up receivers [11]. The wake-up receiver is switched on periodically by the sleep/listen timer to listen to the channel for potential communication. The main receiver is on only when there is data to receive, and the transmitter is switched on whenever the device has a packet to transmit. Since the devices communicate asynchronously, the transmitter has to send out periodic wake-up beacons ahead of data to the target wake-up receiver. The wake-up beacon carries the source node and the target node addresses. The target node sends back an acknowledgment message if its wake-up receiver detects the beacon addressed to it. We take into consideration that beacons are detected by a low power wake-up receiver, which has lower performance than the main receiver. Therefore, for equal detection performance we consider a beacon transmission with a longer duration (lower data rate) without changing the transmit power.

The block diagram of the receiver is shown in Fig. 3. In receive mode, not having to generate the modulation, the synthesizer will consume slightly less power, about 450 µW. The radio frequency front-end has a power budget of 200 µW, the analog to digital converters (ADCs) 200 µW, the digital baseband 100 µW, and the analog decoder 50 µW. Together this adds up to 1 mW.

We evaluate the energy performance of the DCW-MAC based on the above numbers. Fig. 4 shows the device mean power consumption as a function of average packet arrival interval, using optimal sleep interval. For reference, the DCW-MAC energy performance is compared to two other MAC protocols; always-on WRx-MAC [12], where a wakeup receiver always monitors the channel, and X-MAC [13], where devices only have the main radio. For long packet-arrival intervals the optimal sleep time increases, and the DCW-MAC outperforms the always-on WRx-MAC. For shorter arrival times, DCW-MAC primarily competes with X-MAC, and it has the largest advantages in the mid-range of the packet-arrival interval. The analysis shows that the selected node architecture and the estimated properties of the circuits can lead to significant advantages in terms of power consumption using an optimized MAC scheme. A more detailed analysis can be found in [11], where we also evaluate performance with maximum delay requirements imposed on the system.

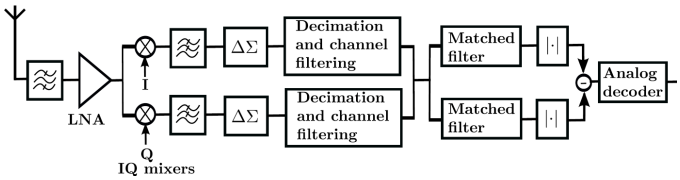


Fig. 3. Receiver block diagram.

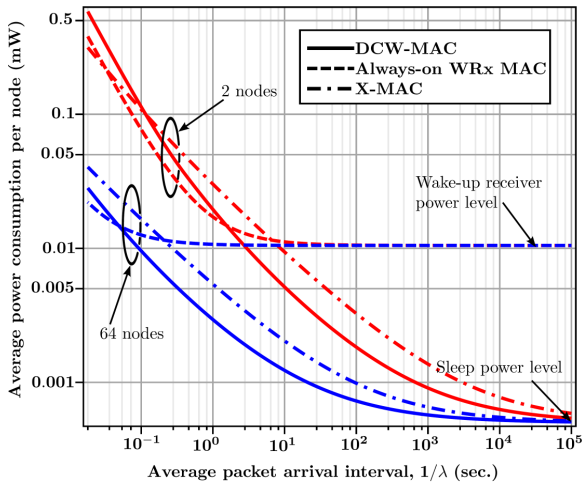


Fig. 4. Power consumption of 2 and 64 node networks, when sleep and listen intervals are optimized for minimal power consumption.

A. Signal Chain

As can be seen in Fig. 3, we use a direct-conversion receiver architecture. The main advantages are the absence of the image frequency, and the fact that after down-conversion the signal is at the lowest possible frequency, centered at DC. This simplifies both filtering and AD-conversion, very important when targeting ultra-low power. Unfortunately the direct-conversion architecture also has a severe problem; DC-offsets and flicker noise are located at the center of the channel after frequency down-conversion. To handle this we use a modulation that carries no information at the center of the channel, and then employ a demodulator that is insensitive to DC signals.

Directly following the antenna, the signal is filtered by an off-chip band select filter. This is typically implemented as a

surface acoustic wave (SAW) filter. The purpose is to attenuate strong out-of-band signals to reduce intermodulation or desensitization of the receiver. Unfortunately the filter introduces some in-band losses and increases both size and cost of the receiver. It would therefore be beneficial to remove it, but the high linearity required to obtain robust operation without the filter, and the resulting stringent phase noise requirements of the frequency synthesizer, are incompatible with the low power budget.

The signal is then fed to the low noise amplifier (LNA). In addition to providing sufficient gain and adding limited noise it should provide proper input impedance to terminate the band select filter. Since this filter does not suppress in-band signals the LNA must have sufficient linearity to handle in-band un-attenuated interfering signals. The LNA is followed by two frequency down-conversion mixers driven by quadrature local oscillator (LO) signals. Quadrature signals are needed to preserve the phase information when down-converting the signal to baseband. The synthesizer thus has to generate quadrature LO signals, but since this is a direct conversion receiver and a rather simple modulation is used, the accuracy needed for these signals is limited, making it feasible to obtain within the power budget. After the mixers the desired signal is at low frequencies, between DC and half the RF-signal bandwidth. By introducing passive low-pass filtering at the output of the mixers, the level of in-band interfering signals can be reduced prior to the ADCs. The output pole inherent to most mixers can be used as a first order filter, which also improves the mixer performance in presence of interferers. To further improve the situation for the ADC we suggest introducing a passive RC-link, implementing a second pole. As this filter is passive it is completely linear.

The signals from the mixer output filters are then fed to the ADCs. Two ADCs are used, each converting the signal from one mixer, together forming the I- and Q-channel. Since the passive filter preceding the ADCs has an order of two, with real valued poles, the attenuation of neighboring channels is rather limited. The ADCs must therefore be able to handle significant interference without being saturated, requiring high dynamic range. It is also of critical importance to handle aliasing, otherwise interfering signals at multiples of the sampling frequency may fold to the same frequency as the desired output signal and prevent reception. The aliasing problem can be handled by either sharp analog filtering, suppressing the high frequency signals before sampling, or by a high sample rate combined with relaxed filters. Here we have chosen the latter alternative, using a continuous-time delta-sigma ADC architecture. In this architecture the signal is first fed to a continuous time filter, before being sampled and quantized at high rate. The ADC thereby has inherent anti-aliasing properties. The quantized signal is then fed back to the input through a digital-to-analog converter (DAC). The feedback increases the linearity of the ADC, and closes a delta-sigma loop allowing the system resolution to be significantly higher than that of the quantizer. The high dynamic range of the ADC minimizes the need for automatic gain control (AGC) to adapt the level of signal to the range of the ADC. To address situations with very strong interference, such as next to a WLAN router, a low gain mode in the LNA and mixers could be implemented. However, reduced sensitivity must be accepted in such extreme situations. Another way to eliminate the need for AGC when having constant envelope signals would to be to apply sharp analog filtering making all interfering signals weaker than the desired one, and then employ limiting amplifiers followed by a single bit quantizer. However, there is a trade-off between filter selectivity, dynamic range, and power consumption that works against this solution. Furthermore, by keeping amplitude information after quantization a better demodulation can be performed at the digital baseband. Sharp analog filters would also need tuning to compensate for process, voltage, and temperature (PVT) variations.

By using the delta-sigma based ADC, the task of filtering for selectivity is moved to the digital domain. A complication is that the digital filters must operate at high clock frequencies to decimate the delta-sigma bit-stream. However, with nanometer CMOS technologies, performing the filtering in the digital domain requires much less power and chip area compared to an analog implementation. The decimation and channel filtering is proposed to be performed by a cascade of half-band filters and decimate by two. The half-band filters suppress signals above half the Nyquist frequency, so after filtering it is possible to reduce the sample rate by a factor of two without folding problems. Both interferers and delta-sigma noise must be suppressed by the filter. As the signal moves through the chain the sampling frequency is reduced, easing the design of latter stages. This is particularly beneficial, since the width of the digital word increases through the chain. Although the clock frequency is several MHz in the beginning of the filter chain, it is still low compared to the capabilities of the technology, and the circuits can operate in weak inversion (sub-threshold) consuming very little power. After filtering the signal is demodulated using matched filters, one filter for identifying the reception of a “0” and one for a “1”, discussed further in the next subsection. The magnitudes of the two matched filter outputs are then compared and the largest determines the received bit. Since only the difference in magnitude of the filter outputs influences the result, not the absolute level, amplitude control (AGC) is not needed. By using the magnitude of the filter outputs the absolute phase is disregarded, making this a non-coherent receiver. The sacrifice in sensitivity of 3 dB compared to a coherent receiver is well motivated by the relative simplicity of the architecture. If higher sensitivity is needed a decoder can be used, as indicated in Fig. 3. The sensitivity will then be increased by both the coding gain and the reduction in effective data rate.

B. Modulation, Demodulation and Decoding

The choice of modulation is a key decision with a dramatic impact on the architecture of both receiver and transmitter, thereby also on the achievable power consumption [14]. To

obtain a transmitter that has both low spurious emissions and high power efficiency, constant envelope modulation schemes are good choices, that is, phase or frequency modulation. An alternative would be to use on-off keying (OOK). However, this causes substantial modulation side-bands, which can disturb other communication. To suppress the sidebands the OOK pulses must be filtered, requiring a linear transmitter which is more complex and less efficient, whereas the phase/frequency modulated signals can be filtered without changing the constant envelope property. This makes phase/frequency modulation an attractive choice for the transmitter, but also the receiver must be considered.

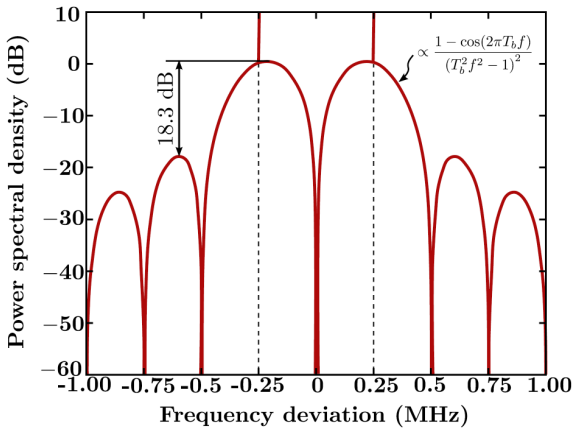


Fig. 5. Power spectrum of 250 kbit/s BFSK modulation with +/- 250kHz frequency deviation.

We use a direct-conversion receiver architecture. This has important benefits for receiver power consumption, but also problems with DC offset and flicker noise at the center of the channel. By choosing binary frequency shift keying (BFSK) with a +/- 250 kHz frequency deviation for the 250 kbit/s signal, a notch occurs at the center of the channel, see Fig. 5. Since there is no information at the center frequency, the demodulation filters can be made insensitive to DC. By using an FSK modulation, it is possible to receive the signal without keeping track of the absolute phase, i.e. non-coherent demodulation can be used. The spectrum shown in Fig. 5 is without filtering applied. As an effect there are peaks at +/-250 kHz, containing half the transmitted energy. When applying phase filtering those peaks will be slightly widened in frequency, but they still contain about half the energy. It is worth noting that the level of the first sideband is about 18 dB below the main signal, 21 dB if also the energy of the peaks is included in the main signal. Applying filtering will further suppress the side-bands, minimizing interference to nearby channels. Another advantage of the chosen modulation is that the relatively high frequency deviation makes it less vulnerable to frequency offsets, reducing the requirements on reference frequency accuracy.

After down-conversion to baseband, the frequencies corresponding to “1” and “0” become +250 kHz and -250 kHz, respectively. With the bit rate of 250 kbit/s this corresponds to a rotation by one turn clockwise for a transmitted “1”, and one turn anti-clockwise for a transmitted “0”. The sample rate is set to 1MS/s, resulting in four samples per transmitted bit. Using delta-sigma ADCs this oversampling factor of two comes for free, as it is achieved by simply skipping the decimation by two stage after the last half-band filter. With these choices the matched filters become very simple: In the filter for “1” the coefficients become 1, j, -1, -j, and in the filter for “0” the coefficients become 1, -j, -1, j. These coefficients are easy to realize by additions of the digital I- and Q- signals. With all coefficients having unity magnitude no scaling is needed, eliminating multipliers. Only sign inversions and interchanges of I and Q before addition are needed to generate all four coefficients. Also note that the sum of coefficients in both cases is equal to zero, resulting in a zero response to DC signals. This eliminates effects of DC offsets and suppresses 1/f noise, relaxing the design of analog parts of the homodyne receiver. A second notch of the matched filters occurs at 500 kHz, at the edges of the 1 MHz wide channel, relaxing the requirements on the channel filter. More notches occur at multiples of 500 kHz, but they are not as important to the system performance as the first two.

The oversampling factor of two that results in attractive properties of the matched filters is also beneficial for time synchronization. It increases the resolution, and accurate timing can be achieved by selecting the proper clock phase for the matched filters. In the beginning of the transmitted packet there will be a preamble that can be used for synchronization. By operating several matched filters simultaneously using different clock phases during the preamble, the clock phase resulting in the strongest output can be identified. Synchronization is then obtained by operating the matched filters on that clock phase for the rest of the packet.

There are two modes of operation, one for 250 kbit/s uncoded transmission, and one for 125 kbit/s with a half rate code. In uncoded mode the digital output is found by comparing the magnitude of the outputs of the two matched filters. If the magnitude of the “1” filter is higher than that of the “0” filter, a “1” was transmitted, and vice versa. In coded mode, the difference in magnitude of the two filters is fed to a decoder, providing soft information. The coded bits are generated by the well-known 4-state (7,5) convolutional encoder, which allows reasonable coding gain while keeping the decoding circuitry small and low power. The half rate transmission together with the coding gain improve the receiver sensitivity by 5dB in the coded mode, at BER = .001. The power consumption of the decoding circuitry is minimized by implementing it in the analog domain biased in sub-threshold. The decoder implements the BCJR decoding algorithm [15].

C. Wave Propagation and Link Budget

The choice of radio frequency band is a key decision. A low frequency band has low link loss, but the antenna is relatively large, and the bandwidth is less than at higher frequency bands. On the other hand, choosing a band at higher frequency results

in a small antenna and large bandwidth, but the link loss is high and it is harder to achieve high RF circuit performance at low power. In medical applications the antenna size is limited, so at low frequencies the antenna becomes an inefficient radiator, and at high frequencies tissue absorption losses dominate [16]. We have chosen the 2.45 GHz ISM band, which offers a good trade-off between these aspects. The main reason for choosing this frequency band, however, is that it offers 80 MHz of license-free bandwidth available world-wide [17]. This makes it popular also for WLAN and other short range wireless systems, and it is therefore important that our radio architecture is designed to handle substantial interference. Receiver sensitivity is of course important, but even more so is the ability to handle interference. The front-end noise figure is therefore relaxed, and to take full benefit of the ADC dynamic range, the ADC is allowed to contribute a significant amount in the noise budget. It is worth mentioning that there are plans for a new frequency band for medical applications adjacent to the ISM band. According to [8], in Europe a group in ETSI is planning for a 2483.5-2500 MHz band, and in the US there are plans for 2360-2400 MHz. If these plans are realized it should be possible to cover both these bands and the ISM band using the same integrated circuit. The new medical bands would have far less interference, and thereby higher reliability.

To create a link budget for the system, the link loss must be estimated. When it comes to WBANs the worst case is when receiver and transmitter are located on opposite sides of the body. A particularly difficult case is when the two antennas are placed inside the ears, not only being on opposite sides of the head, but also obscured by the outer ears. Ear-to-ear communication has important applications in binaural hearing aid systems, with one hearing aid in each ear communicating wirelessly to synchronize noise suppression parameters. To estimate the ear-to-ear link loss, preliminary investigations were performed using a modified SAM head [18], where a simple model of the ear canal was included. The antennas were miniaturized by loading them with a disc and embedding them inside a high permittivity material. Two antenna positions were investigated; in-the-ear (ITE) and in-the-canal (ITC). SEMCAD [19] was used for the simulations, employing the FDTD method. The ear-to-ear link loss at 2.45 GHz was 48 dB for the ITE case, and 92 dB for ITC. Since the link loss for the ITE case was low enough to support low power communication, this antenna placement was chosen for further investigation, using realistic heterogeneous heads of different age and gender, as illustrated in Fig. 6 [20]. The realistic heads have more link loss when compared to the SAM head because of the protruding part of the outer ear called pinna and the lossy skin which are absent in the SAM head [21]. The worst case simulated using realistic heterogeneous heads is a link loss of 79 dB for the largest head.

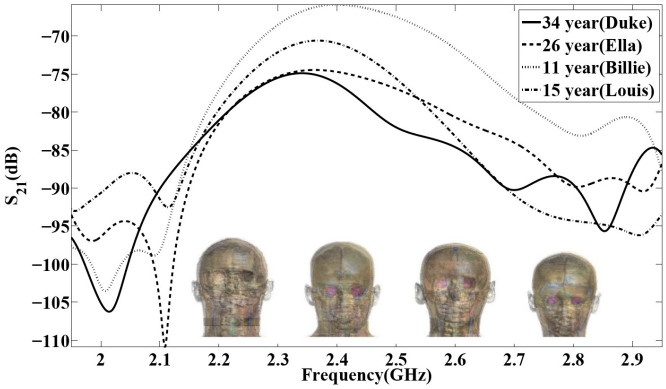


Fig. 6. Ear-to-Ear Link Loss for different head phantoms. Heads from left to right: Duke, Ella, Louis, and Billie.

We can now make a link budget, with the SNR required for demodulation taken from the baseband simulations in the last section. For BER=.001 we get Eb/No=12 dB uncoded and 10 dB coded. Both received and transmitted signals must pass the SAW band-select filter, and a 3 dB worst case insertion loss for a small SAW filter is assumed. Assuming that the on-chip analog part can be realized with 13dB noise figure, the 250 kbit/s mode results in a receiver sensitivity of -174+3+13+12+10·log(250k)=-92 dBm, and the 125 kbit/s mode -174+3+13+10+10·log(125k)=-97 dBm. The transmitter has -7 dBm output power, -10 dBm after SAW losses, which results in a maximum link loss of 82 dB at BER .001 in the 250 kbit/s mode, and 87 dB in the 125 kbit/s mode. With the simulated ear to ear link loss of 79 dB for an adult male, this gives 8 dB fading margin for the 125 kbit/s operation. If more margin is required a lower rate code can be chosen, at the expense of data rate.

D.Handling of Interference

When it comes to receiver robustness to interference, as well as transmitter out of channel emissions, the local oscillator phase noise is a key parameter. With the sharp digital channel filter used, the receiver selectivity will be completely determined by reciprocal mixing. In [22] a low power and compact quadrature LO generation circuit is implemented in 90-nm CMOS technology. Consuming 335 µW from a 1 V supply it achieves -110 dBc/Hz phase noise at 1 MHz offset. In our still unpublished work we have measured similar performance at 250 µW using 65-nm CMOS technology. An interferer about 30 dB stronger than the desired signal can then be tolerated in the adjacent channel, 40 dB in the second adjacent, 50 dB at 5 MHz offset, and more than 60 dB at 20 MHz. Selectivity together with linearity determines the ability to handle interference. Having a 50 dB dynamic range in the ADC, combined with the 2nd order passive filter preceding it, will limit the maximum signal in-channel and in the adjacent channels to -49 dBm. For channels further away the filter will attenuate the signal, and with 2 MHz poles a signal of -33 dBm can be tolerated at 10 MHz offset. This is a very high level, which will force the LNA and mixer into compression. At such high offset frequencies the maximum signal level will thus be

determined by the RF front-end compression point.

Apart from compression, 2nd order intermodulation is also a key concern in the RF part of a direct conversion receiver. Choosing a differential mixer enables high even-order linearity, mainly limited by mixer transistor mismatch. With a 0 dBm circuit IIP2, a -38 dBm 20 MHz wide WLAN signal desensitizes the receiver by less than 3 dB. The low bandwidth of our system compared to WLAN is very beneficial here, as most intermodulation distortion falls out of channel.

Assuming a WiFi interferer with a power of Pint [dBm], we can estimate the input referred energy of the resulting IM2 products as $2*(P_{int} - IL_{band\text{-}select}) - IIP2$. This energy will be distributed as follows; DC (50%), twice the carrier frequency (25%), and baseband (25%) [23]. The energy at baseband will be distributed from DC to the RF bandwidth of the signal, which is equal to 16 MHz for the WiFi signal. Since the energy at DC is rejected by the matched filters and the baseband has a bandwidth of 0.5 MHz, compared to the interfering signal bandwidth of 16 MHz, we can estimate the total energy entering the receiver as $P_{int_BB} = 2*(P_{int} - IL_{band\text{-}select}) - IIP2 - 6dB - 15dB$, where - 6dB corresponds to the 25% energy at baseband, and - 15dB to the ratio between 0.5 MHz and 16 MHz. With coding we require an Eb/No of 10 dB for a data rate of 125 kbit/s. With an No of $P_{int_BB} - 10*\log(500k)$ we can estimate the largest interferer with a 3 dB loss of sensitivity as $P_{int}=IL_{band\text{-}select} + (P_{sens} + IIP2 + 14dB + 10*\log(500k) - 10*\log(125k))/2$. Included is a 3 dB increase of Eb as the baseband signal power comes from both sidebands. With a base sensitivity of -97 dBm and an IIP2 of 0 dBm we estimate that we can tolerate an interferer of -35.5 dBm. However, it should be noted that the power spectral density of the intermodulation is not flat, and the intermodulation is strongest at low baseband frequencies. The calculation above is thus a bit optimistic, and to find a more accurate estimate we performed simulations in MATLAB™. As the absolute carrier frequency is not important the 64QAM OFDM WiFi signal was generated at a reduced carrier frequency to reduce simulation time. The signal was sent through a 2nd order non-linearity, and the resulting spectrum can be seen in Fig. 7. The result was that we can tolerate an interferer of -37.5 dBm, a 2 dB degradation compared to the calculation.

Transmitters using constant envelope modulation, such as in Bluetooth or the system of this paper, cause limited problems with even order intermodulation. They simply cause a DC-offset when they are on, to which the matched filters are not sensitive. In situations with very strong interference, such as near a WLAN router, the low noise amplifier could be by-passed or put in a low gain mode. This reduces the signal level in the analog part, allowing it to handle larger input signals, at the expense of sensitivity. To avoid ADC saturation, reduced gain is also beneficial when the receiver is located very close to the transmitter, with a link loss less than 40 dB.

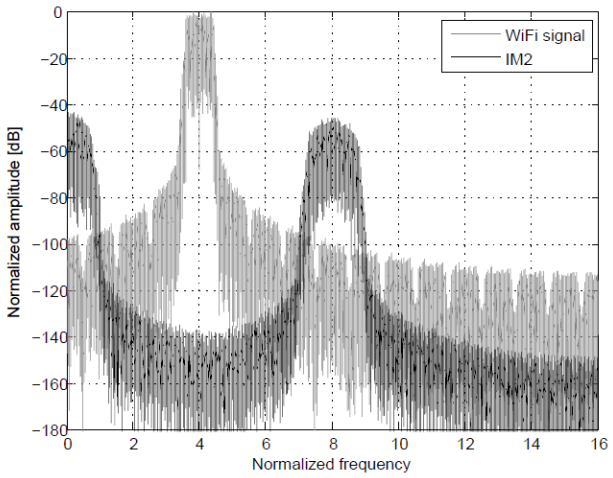


Fig. 7. Simulated interfering WiFi signal and its IM2.

III. Circuit Design

To demonstrate the feasibility of a receiver with the performance and power budget indicated, the design of key building blocks is described in this section. The next step will be to co-design the different parts into a system-on-chip featuring a complete receiver chain. We then target the use of no more than two supply voltages, one for analog and one for digital.

A. RF Front End

As inductors require substantial chip area and scale poorly with technology, we aim for an inductor-less LNA and mixer design. However, as low phase noise is critical to the selectivity of the receiver, we need to use an LC oscillator with an on-chip inductor. To minimize chip area the quadrature LO signal needed by the direct conversion architecture is generated by a frequency divider. In this way only a single LC oscillator operating at twice the frequency is needed, and at twice the frequency the inductor size is reduced. Given that the 5 GHz frequency divider can be realized with low enough power consumption this is an attractive solution.

A prototype of the front-end was presented in [24], operating at 915 MHz. The frequency of operation was limited by the included frequency divider, but we are confident that one with a 2.45 GHz output frequency with only slightly increased power can be designed [22]. The other blocks are capable of operating at full frequency. The LNA and mixers are shown in Fig. 8.

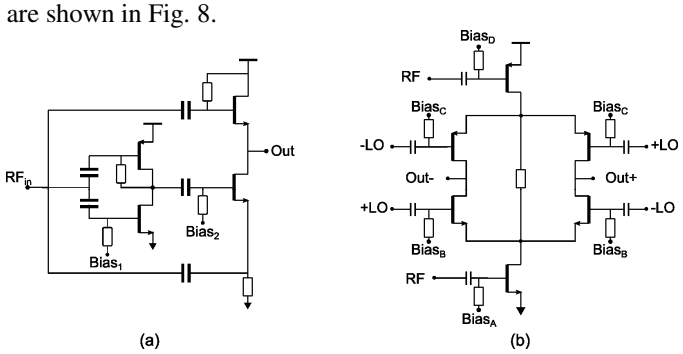


Fig. 8. Circuit schematic (a) LNA (b) One of the I- and Q-mixers.

The usual method of generating a resistive LNA input impedance is to use inductive degeneration. Although high performance can be achieved, it depends on two inductors, one of which tends to be rather large. The alternatives are to terminate the input with a resistor, or to actively generate a feedback current. Though the first is a cheap and simple method, we have chosen the active solution, as it can achieve superior noise performance [25]. An additional advantage of the chosen feedback solution is that it provides some inductance, which can reduce the effects of parasitic capacitance at the input. To reduce power consumption 200 Ω input impedance is used. As typical SAW filters are designed for 50 Ω, either a custom designed filter is needed, or an impedance matching circuit transforming the 200 Ω impedance of the chip to 50 Ω. If a standard 50 Ω filter is to be used directly without impedance transformation its performance must first be verified in a 200 Ω environment.

By using complementary devices the mixer can operate in a manner similar to a double balanced mixer, despite having a single ended input. The two sides, formed by NMOS and PMOS devices, respectively, reuse the same bias current, minimizing power consumption. High output impedance can be achieved, and thus also high voltage conversion gain. Additionally, a complementary solution can provide some IM2 cancellation [26]. A resistor is used to bypass some bias current past the switch devices, slightly reducing flicker noise.

B. Delta-Sigma ADC

Continuous and discrete time delta-sigma modulators have recently been used in sensor networks and biomedical applications, providing high resolution at low power consumption [27], [28], [29]. Continuous time delta sigma modulators have several advantages over their discrete time counterparts. The most important one, and the primary reason for choosing a continuous modulator in our case, is the inherent anti-alias filtering.

The current system specification is an SNR of 50 dB over a 500 kHz bandwidth, using 8 MHz sampling frequency, which is the target for our on-going designs. However, the modulator design started before the receiver specification was finalized, targeting a high SNR of 73 dB over a 125 kHz bandwidth, with a sampling frequency of 4 MHz. This modulator has been fabricated and verified by measurements [30], showing the feasibility of implementing a continuous-time delta-sigma modulator for ultra-low power receivers.

A signal to quantization noise ratio (SQNR) of 81 dB was targeted to provide sufficient margin for thermal noise. In order to achieve this SQNR, a 3rd order loop filter with a 3-bit quantizer was used. The so-called CIFB architecture was chosen for the loop filter. It was implemented with active-RC integrators and additional feedback paths were used to create zeros in the noise transfer function. The block schematic of the modulator is shown in Fig. 9. All RC integrators were implemented using single stage folded-cascode amplifiers.

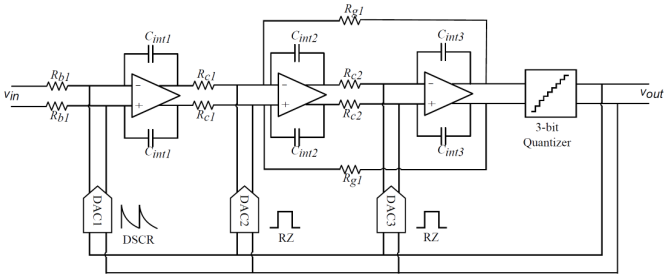


Fig. 9. Block schematic of the delta sigma ADC.

The first DAC employs dual exponential feedback pulses which reduce the jitter sensitivity and relax the slew rate requirement on the amplifier in the first integrator. This DAC is implemented with switched-capacitor-resistor circuits [31]. Return-to-zero (RZ) DACs were used in the two remaining feedback paths, resulting in simpler implementation compared to the first DAC. The RZ pulses were delayed a quarter of the clock period to ensure that the quantizer has fully processed the samples before they are converted by the DACs. RZ feedback is advantageous over non-return-to-zero (NRZ) feedback, since a delayed NRZ pulse would enter into the next clock period. To compensate for that an extra feedback DAC would be required as well as an adjustment of the loop filter coefficients.

Switched-resistor cells were used to realize the two RZ DACs. Since the RZ pulses are delayed by one quarter of clock period, both RZ DACs use a quadrature clock. All DACs are updated well after the beginning of the clock period. The 3-bit flash quantizer was realized with a resistor ladder and regenerative latch comparators without preamplifiers. The overall design also includes a non-overlapping clock generator and a data weighted averaging algorithm for dynamic element matching of the DAC components to improve linearity.

C. Decimation and Channel Filtering

The first task of the digital baseband circuit is to re-sample the data received from the ADC at a rate of 8 MS/s to 1 MS/s. A down sampling of the signal must be preceded by anti-alias filtering. Wave-digital IIR filters are chosen as they can be implemented with fewer coefficients for the required cut-off frequencies, saving both power and chip area. Another property of these filters is that they operate with high stability when the order of the filter is low [32]. Therefore, instead of implementing a high order filter, a cascade of low order filters is applied to achieve sufficient suppression of high frequency interference and delta-sigma modulator noise before decimation. The low order filter is a third-order bi-reciprocal lattice wave-digital filter [33].

Half-band digital (HBD) filters are highly suitable as a decimator or interpolator, for sample rate conversions by a factor of two. The proposed filter has the benefit of low arithmetic complexity, reducing both power consumption and chip area. The transfer function of the proposed filter is

$$H_z = \frac{1 + 2z^{-1} + 2z^{-2} + z^{-3}}{2 + z^{-2}}, \qquad (1)$$

and the magnitude response is shown in Fig. 10. As can be

seen the -3 dB point is at half the Nyquist frequency, hence the name half-band filter. The suppression in the cut-off region is about -22dB. In [34] the structure of this particular filter implementation is described as shown in Fig. 11, where x_n is an input and y_n an output of the filter. The multiplications by coefficients 2 and 0.5 are easily implemented by shifts.

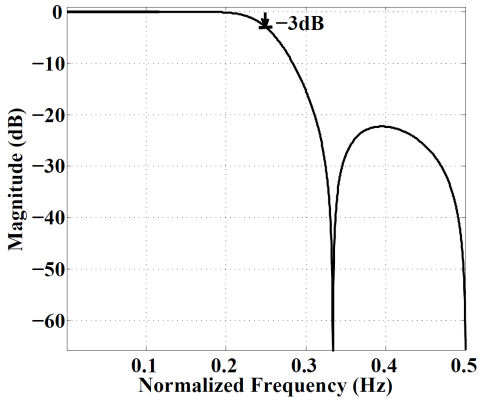


Fig. 10. Magnitude response of the HBD filter.

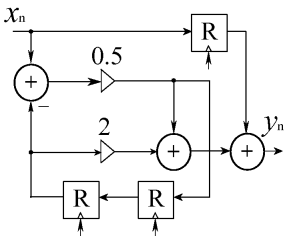


Fig. 11. HBD filter structure.

Initial analysis of a decimation filter chain was performed with relaxed requirements, decimating from of 4 MS/s to 250 kS/s. The filter was designed for sub-threshold operation, where the energy minima can be achieved, using the sub-threshold energy model presented in [35]. However, the drawback of such aggressive voltage scaling is massive reduction of the maximum speed. Analysis indicated that the required throughput was not achievable using the original architecture as shown in Fig. 11. Therefore, unfolding was applied to the original architecture, by which k parallel samples are calculated per clock cycle, k being the unfolding factor. The original filter architecture was unfolded by factors 2, 4, and 8, and characterized for sub-threshold operation, using low-power high-threshold-voltage (HVT), low-power standard-threshold-voltage (SVT), and low-power low-threshold-voltage (LVT) cells. The energy and throughput analysis was carried out for filters with all three library implementations [36], [37]. With stringent low energy dissipation requirements combined with moderate throughput requirements, unfolded architectures synthesized with SVT cells were found to be the best option. The lowest power decimation filter chain dissipates 205 fJ per output sample, corresponding to a power consumption of just 25 nW at 125 kS/s output.

According to the presented receiver architecture, the ADC provides the data at the rate of 8 MS/s. At least 60 dB suppression in the cut-off region is needed to achieve sufficient rejection of delta-sigma quantization noise. This is achieved by using a cascade of three HBD filters to form one 9th order down-sampling filter stage. An identical filter is used for the 1 MS/s decimated data, to perform the last stage of channel filtering. However, the last filter stage is not followed by decimation, resulting in the desired oversampling rate of a factor 2. Using three cascaded half-band filters results in a 9 dB signal drop at 500 kHz, but at 400 kHz the drop is negligible. Therefore this does not represent a problem, as the matched filters have a notch at 500 kHz. The resulting adjacent channel filtering is very steep, and as discussed before, the selectivity is set by local oscillator phase noise. The power consumption of the decimation and channel filter will increase compared to the first filter, since an 8 MHz input frequency is used instead of 4, and due to the increased filter order. However, as the first filter consumed just 25 nW, we are confident that the two filters for I and Q can be realized with a power consumption of less than 2 μW in total, also including design margin for process variations. This shows the effectiveness of digital filtering implemented in nanometer CMOS technology, and motivates the choice of architecture.

D. Analog Decoder

Analog decoding was introduced in 1998 [38], [39]. Since then the idea of implementing soft iterative decoding algorithms in analog circuitry has been pursued by other researchers, aiming for improvements over digital implementations in terms of power consumption, speed and silicon area. In [40], [41], [42] power reduction of analog decoders compared to digital counterparts by factors ranging from 8 to more than 200 are reported.

The main building block for analog channel decoders based on the BCJR decoding algorithm is the Gilbert vector multiplier. To perform proper multiplication, the Gilbert multiplier requires transistors with an exponential current to voltage characteristic. MOS transistors in strong inversion have a quadratic characteristic, but in weak inversion, which is the region for ultra-low power, the characteristic has the desired exponential form. Despite the low speed of transistors operating in weak inversion, high throughput can still be achieved in analog decoders by parallel processing in a network of transistors operating in continuous time.

The decoding process of a coded block starts by loading soft values from the matched filters to parallel inputs of the network. Each soft bit is translated to a differential input current to the decoder, representing the probability of the received bit being “1” over the probability being “0”. Since the probabilities are represented by currents, there is a need for a unique reference current in the circuit corresponding to the probability of 1, referred to as I_{ref}.

In this design there is no need for temporary storage of data during processing; when a new block of received data is introduced to the circuit, all currents and voltages change in continuous time until they settle to a new level. The decoded bits can then be read from the stable output of the circuit.

To be able to incorporate an analog processing stage after

digital demodulation and filtering, a digital interface has been designed for the analog decoding core. The information after matched filtering is buffered in the digital domain (digital memory) and then converted to differential currents by an array of low resolution current steering DACs. Three bits is sufficient in the DACs, allowing very low power and area implementation. This eliminates the need of implementing memory in the analog domain, which would require area-consuming storage capacitors. The memory can instead be implemented efficiently in the digital part. A digital buffering stage with the size equal to the block length is required to apply the received stream of soft information to the analog decoding core for parallel processing. An array of current comparators performs hard decision on the output of the circuit. A digital controller provides the required timing signals and serially streams out the decoded bits. The architecture of the decoder is shown in Fig. 12, whereas the detailed structure is presented in [43].

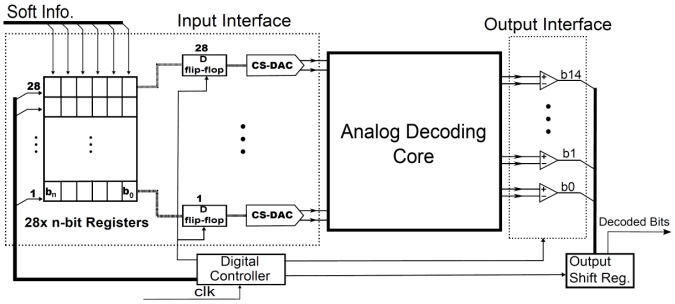


Fig. 12. Architecture of the (7,5) analog decoder with digital I/O.

IV. Results

A. RF Front-End

Measurements were performed with the chip wire bonded directly to a PCB. When operated at 915 MHz the front-end has a voltage gain of 30 dB from a 200 Ω source, or 36 dB with an external match to a 50 Ω source. The total measured noise figure is below 9 dB, the ICP_{1dB} is -37 dBm, and the IIP_3 is -28 dBm. IIP_2 is better than -5 dBm. S_{11} (related to 200 Ω) is better than -10 dB from 500 MHz to 2.6 GHz. The mixers provide 18 dB voltage conversion gain and their flicker noise results in a front-end noise corner of 100 kHz. The total power consumption of the LNA and mixers is 180 µW, and the divider consumes 100 µW [24]. These numbers are well in line with the target.

The LNA was also measured stand-alone, using an impedance tuner to set the source impedance to 200 Ω at each frequency point. At 2.45 GHz it achieved 8.2 dB voltage gain from a 200 Ω source, and a noise figure of 6.8 dB, see Fig. 13. This should be compared to the gain of 12 dB achieved at 915 MHz. The same LNA bias current of 120 µA was used at both frequencies. The reduced LNA gain results in a front-end noise figure of 11.5 dB in the 2.45 GHz band. This is 1.5 dB higher than targeted, but if the ADCs still contribute as much noise as a front-end with 10 dB noise figure, the total receiver sensitivity will degrade by just 0.8 dB. Still a re-design of the front-end optimizing it for 2.45 GHz would be worthwhile.

Still within the power budget of the system, we have recently designed a front-end with 50 Ω input impedance to be directly compatible with standard SAW filters. With the present front-end, however, either a 50 Ω off-chip match has to be used, or a 200 Ω filter.

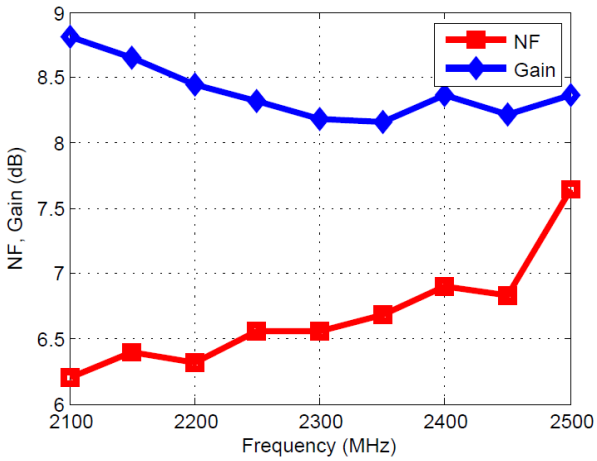


Fig. 13. Measured LNA gain and noise figure.

B. Delta-Sigma ADC

The delta sigma modulator has been fabricated in 65-nm CMOS and tested. Using a 900 mV supply the circuit consumes a total power of 380 µW. The full scale differential input signal is 200 mV. The modulator achieves a maximum measured SNR of 74 dB for an input signal of -1.7 dBFS, and a maximum SNDR of 70 dB for an input signal of -2.5 dBFS [30].

Since according to the most recent receiver specifications about 50 dB of SNDR is sufficient in the ADC, additional measurements were performed to estimate the power consumption at this SNDR value. The result is shown in Fig. 14. The modulator consumes 57 µW at 53 dB SNDR. Two things should be pointed out. First, the modulator is optimized for a higher SNDR, and re-optimization would reduce both power consumption and chip area; Second, the bandwidth should be increased by a factor of four to fit the receiver specification. With this in mind, we think that the power budget of 100 µW for each ADC can be met.

Anti-aliasing suppression around the sampling frequency is the main reason to the choice of continuous-time delta-sigma ADC architecture. The suppression was therefore measured, and the result is shown in Fig. 15. The suppression is far better than needed by the system, being above 80 dB throughout the channel.

C. Analog Decoder

The analog decoder is implemented and simulated using 65 nm CMOS low-leakage high-VT (LL-HVT) standard transistors. The analog decoding core consumes 19 µW from a 1.2 V supply, independent of throughput, up to a maximum of 1.25 Mbit/s. The total power consumption including the digital

interface and the mixed signal parts is 40 µW at an output data rate of 125 kbit/s, but then it should be noted that the digital interface has not been optimized. For instance it supports 6 bit soft inputs for test purposes, whereas 3 bits would be sufficient for the system, and it operates in strong inversion on a supply voltage of 0.8 V.

Our simulations show that to achieve maximum coding gain from the (7,5) decoder using the BCJR algorithm, a block length of at least 14 should be used, but that further increasing the block length provides negligible extra coding gain. A block length 14 was thus chosen, giving a close to maximum coding gain while minimizing the size of the circuit.

Operating in the sub-threshold region, analog decoders are sensitive to transistor mismatch [44]. Monte-Carlo simulations were therefore performed to determine suitable transistor sizes in the Gilbert multipliers. As presented in [45], when I_{ref} =100 nA, the transistors must be at least W/L = 1µm/0.6 µm to make the BER performance robust to process variations.

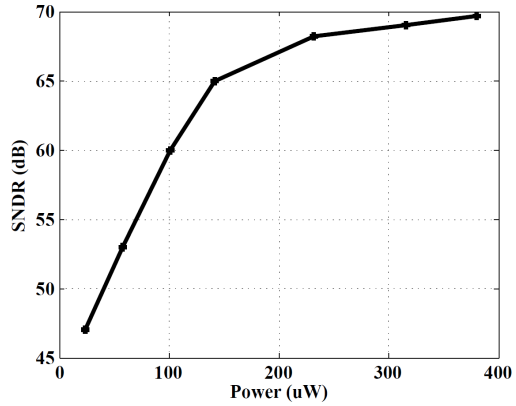


Fig. 14. Measured SNDR vs. power consumption.

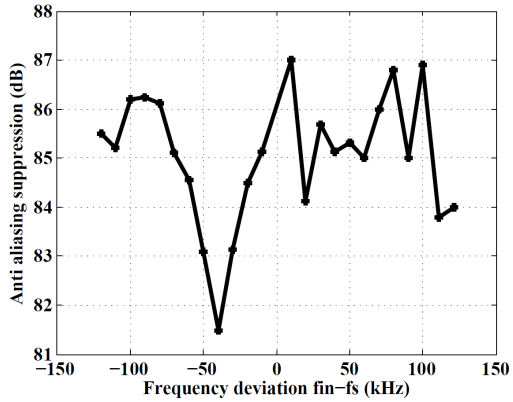


Fig. 15. Measured anti-alias suppression vs. offset from sampling frequency.

D. Complete Baseband

To investigate the behavior of the chosen baseband architecture, a signal chain consisting of delta-sigma ADCs, digital decimation and channel select filters, digital matched filters, and analog decoder has been simulated in MATLAB™. The RF front-end and antenna were thus not included in the baseband simulations. First the performance in presence of just thermal noise was investigated. In Fig. 16 the BER versus energy per information bit (Eb) divided by thermal noise spectral density (No) is shown. Two simulated curves can be seen, one including the decoder, and one for the uncoded mode. In the figure also the theoretical curve for non-coherent detection is indicated as a reference. Compared to theory about 1dB stronger signal is required for a certain BER in the uncoded mode. Half of this difference is due to the synchronization scheme using the 1MS/s decimalted signal. The timing error can be up to half a sample interval, i.e. 0.5µs, and to include some margin we have used a total error of 0.625µs in Fig. 16. In Fig. 17 the loss due to timing error is shown, and as can be seen the simple synchronization results in about 0.5dB loss. For BER=.001 an Eb/No slightly above 10 dB is required in the coded mode, and 12 dB in the uncoded. This serves as the baseline, to which we compare the performance when investigating impairments due to 1/f noise and frequency errors.

Starting with 1/f noise, the curves in Fig. 18 show the required increase in signal level to maintain a certain BER in 1/f noise. As can be seen, for a noise corner of 100 kHz the signal must be increased by 1 dB. Thus the receiver is rather robust to 1/f noise, thanks to the DC-notch of the matched filters. In Fig. 19 the sensitivity to frequency errors is shown. At 50 kHz the signal level must be increased by 1 dB to obtain the same BER as for zero frequency error. For a 2.45 GHz carrier, this corresponds to a 20 ppm total frequency error, setting the required crystal accuracy. To verify the robustness to interference two adjacent channel tones were injected at the input at the frequencies 800 kHz and 1.23 MHz. The BER was investigated when each tone had an amplitude up to 15 times higher than the desired signal, see Fig. 20. As can be seen no degradation is visible in the figure, thanks to the sharp digital filtering. The complete receiver selectivity is instead limited by local oscillator phase noise.

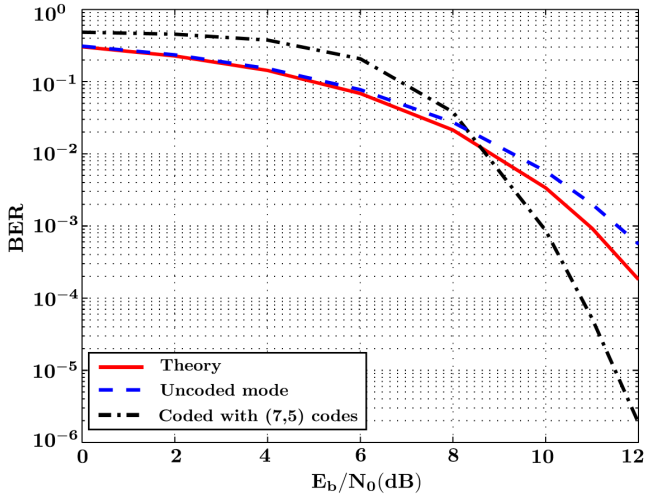


Fig. 16. BER in thermal noise; theoretical non-coherent detection, coded, and uncoded mode.

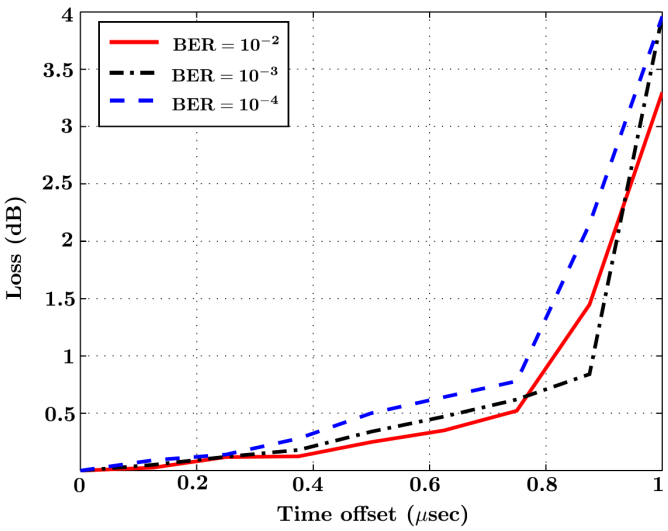


Fig. 17. Impact of time offset on signal level at BERs .01, .001, .0001.

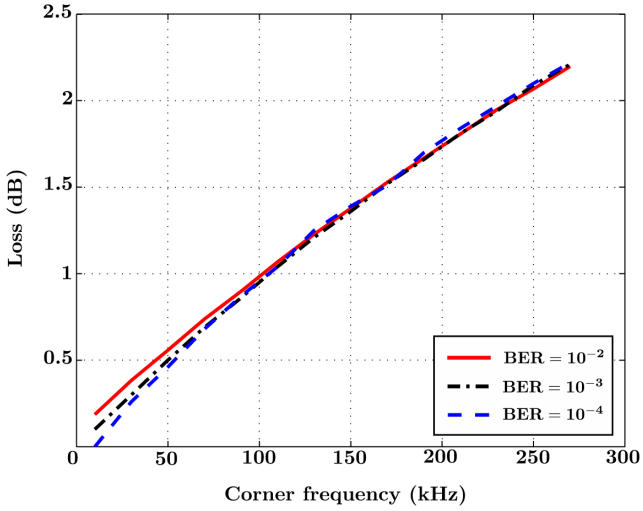


Fig. 18. Impact of 1/f noise corner on signal level at BERs .01, .001, .0001.

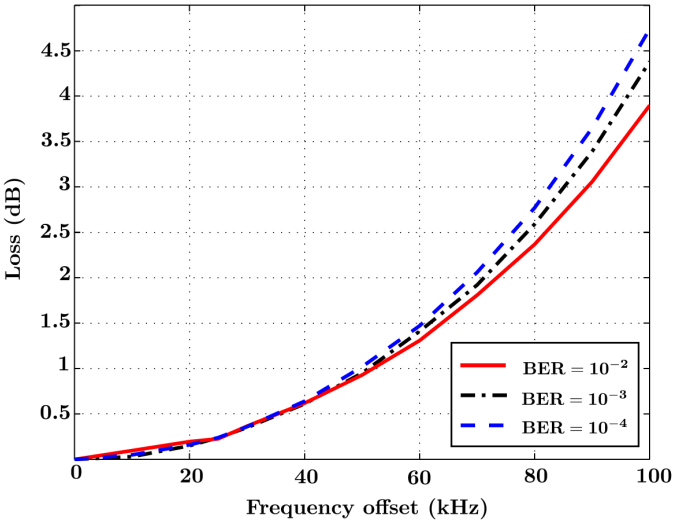


Fig. 19. Impact of frequency errors on signal level at BERs .01, .001, .0001.

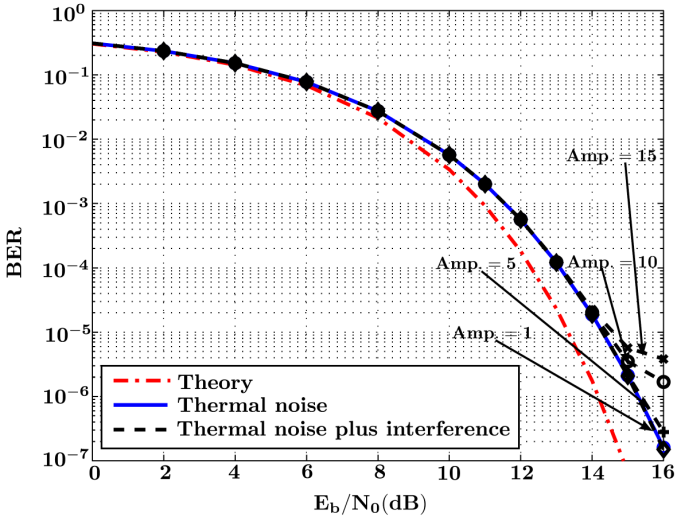


Fig. 20. Performance with interference; two tones at 800 kHz and 1.23 MHz with different amplitudes (Amp). The amplitude of desired signal is 1.

V. Conclusion

An architecture for receivers in wireless devices requiring ultra-low power consumption has been presented. It is intended for the 2.45 GHz ISM band, and hence robustness to interference is essential. The wave propagation in wireless body area networks at 2.45 GHz has been investigated and taken into account in the link budget. FSK modulation has been chosen to facilitate high efficiency transmitters with low spurious emissions, and by using a modulation index of 2, DC-offsets can be suppressed in a homodyne receiver without loss of information. The receiver chain consists of LNA, quadrature mixer, continuous time delta-sigma ADC, digital decimation and channel select filters, digital demodulation via matched filters, and analog decoding. Circuits have been designed and fabricated in 65-nm CMOS technology to investigate the achievable performance, and system level simulations of the complete baseband signal chain have been performed to investigate effects of 1/f noise and frequency errors. Using the proposed receiver architecture it is deemed feasible to achieve robust communication in 2.45 GHz WBAN applications with a power budget of just 1 mW in active mode. To minimize the mean power consumption we propose to use a medium access scheme based on a duty cycled wakeup radio capable of detecting node addresses.

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