Guest Editorial
Next-Generation Delta-Sigma Converters

DELTA-SIGMA ($\Delta\Sigma$) modulation has demonstrated to be one of the most efficient techniques for the implementation of Analog-to-Digital (A/D) and Digital-to-Analog (D/A) converters in many diverse application scenarios. These kinds of converters cover one of the widest conversion regions of the resolution-versus-bandwidth plane, by palliating the effects of low-accuracy analog integrated circuit components with the action of two main signal processing techniques, namely: oversampling and noise shaping. However, in spite of their benefits with respect to other data converters, technology downscaling towards nanoscale, as well as the aggressive specifications required for A/D interfaces in many consumer electronic products, demand more and more efficient circuits and systems strategies in order to push the state of the art on data conversion forward.

In this scenario, this special issue of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems aims to provide readers with an overview of the most recent advances in $\Delta\Sigma$ circuits and systems techniques, which are in the frontiers of data converters, in terms of energy efficiency, frequency range and scalability to advanced nanometer CMOS. To this purpose, a Call for Papers was published in February 2015 and an exhaustive selection process was carried out after the submission deadline in May 2015. The submitted manuscripts were peer reviewed, involving several review rounds in the majority of cases in order to refine and increase as much as possible the high scientific quality of accepted papers. Overall, the review process involved a total of 38 submissions, out of which 12 papers were finally accepted, which cover a great variety of emerging topics dealing with the design of high-performance $\Delta\Sigma$ converters.

The special issue begins with an overview paper contributed by the guest editors, where the emerging circuits and systems techniques which are at the forefront of the state of the art in $\Delta\Sigma$ modulators ($\Delta\Sigma$Ms), are surveyed. The envisioned techniques and trends in the design of $\Delta\Sigma$Ms are presented in a systematic way, giving the authors' visions on the future of $\Delta\Sigma$ ADCs as an introduction to the rest of contributions summarized below.

I. $\Delta\Sigma$Ms for Digital-Intensive Wireless Telecom

One of the hot trends which are giving rise to new families of $\Delta\Sigma$Ms are those intended for Radio-Frequency (RF) digitization in modern wireless communication systems evolving toward Software Defined Radio (SDR). This topic is covered by the next three papers in this special issue, addressing different design considerations. In the first paper, Ritter and Ortmanns, from the University of Ulm, review the state of the art of $\Delta\Sigma$Ms for receiver applications, giving a tutorial overview of $\Delta\Sigma$ techniques used for improved interferer rejection, and presenting a method to analyze and to scale the internal states meeting the requirements of diverse interferer scenarios. In the next paper, Östman *et al.*, from Aalto University, Nordic Semiconductor and HiSilicon, discusse the use of the so-called direct $\Delta\Sigma$ receivers for the implementation of RF-to-digital conversion in digital-intensive wireless receivers. The paper proposes new models and design equations that link RF stage properties to ADC system properties, thus providing a useful circuit design tool for these emerging $\Delta\Sigma$Ms. In the third paper dealing with wireless telecom, Bettini *et al.*, from ETH, AMS and ACP Advanced Circuit Pursuit AG, present the design and measured results of a reconfigurable $\Delta\Sigma$M for multi-standard 2G/3G/4G wireless receivers. The chip reconfigures the oversampling ratio and the quantizer resolution to adapt the effective resolution from 13.2 bit to 9.7 bit, within a programmable signal bandwidth from 100kHz to 25 MHz with adaptive 3.4-to-56.7 mW power consumption.

One of the main challenges associated with the practical implementation of RF-to-digital conversion is achieving a widely tunable frequency band with reasonable low power dissipation. This problem is explored in the next paper by Feng *et al.*, from the University of Macao and the University of Pavia, who propose the use of polyphase despomposition technique to implement widely tunable Band-Pass (BP) $\Delta\Sigma$Ms, with a higher robustness to interleaved mismatch. The method is analyzed and applied to high-order single-loop and cascade topologies, being a very promising strategy to implement ADCs for SDR. Also based on the idea of using Time-Interleaved (TI) $\Delta\Sigma$Ms, Han and Maghari, from the University of Florida, present a TI noise-coupled $\Delta\Sigma$M that uses the inherently available time-domain quantization error of noise-shaped integrating quantizers (NSIQ) to increase the order of the noise transfer function. A modified NSIQ scheme is proposed which can be implemented in any arbitrary number of TI channels and is specially suited for high-resolution wideband applications.

II. $\Delta\Sigma$Ms With Time/Frequency-Based Quantization

Another tendency in the design of state-of-the-art $\Delta\Sigma$Ms consists of using time/frequency-based instead of amplitude-based quantization. This strategy is addressed by the next two papers of this special issue. The first paper, contributed by Lee *et al.*, from the University of Texas at Austin, presents a first-order scaling-friendly VCO-based closed-loop $\Delta\Sigma$ ADC. The circuit uses the VCO as both quantizer and integrator with intrinsic mismatch shaping capability, thus obviating the need for OTAs and precision comparators, and automatically addressing DAC mismatches. A chip prototype integrated in 130nm CMOS demonstrates the benefits of the presented techniques, featuring 65.8-dB SNDR within a 2-MHz signal bandwidth with a power consumption of 1.1 mW. The next paper, written by Chen and Hung, from National Chiao

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Tung University, presents the design and measurements of a third-order CT $\Delta\Sigma$M in 90-nm CMOS. The chip uses 3-bit time-domain flash quantizer and a novel Data-Weighted Averaging (DWA) linearization technique that does not use any adder circuit, featuring 65.3-dB SNDR over a 20-MHz signal bandwidth with a power consumption of 5.8 mW.

III. Calibration/Compensation Techniques

In parallel with the development of new $\Delta\Sigma$ architectures, significant progress is being made in calibration and error compensation techniques. This topic is addressed by the next two papers in this special issue. In the first one, Pol *et al.*, from TU and Philips Research Eindhoven, propose a new background calibration technique based on the limit cycle model of $\Delta\Sigma$Ms, showing how a simple counting and categorization of output bit-patterns can be used for the correction and adjustment of errors in the modulator loop filter. This method, verified by experimental measurements of a test chip, is especially suitable to make reconfigurable $\Delta\Sigma$Ms more robust to the effect of circuit error mechanisms in a wide range of applications. In the next paper, Sanyal and Sun, from the University of Texas at Austin, present a novel Dynamic Element Matching (DEM) technique that can simultaneously high-pass shape static and dynamic errors of each individual feedback DAC element, while ensuring a good decorrelation of the instantaneous transition density from the input signal. The method is compared with existing art on DEM techniques, showing its effectiveness for high-performance multi-bit Continuous-Time $\Delta\Sigma$Ms.

IV. Energy-Efficiency $\Delta\Sigma$ Techniques

The special issue is closed with two trending strategies to increase the energy efficiency of $\Delta\Sigma$Ms in low-frequency applications. Thus, Chen *et al.*, from Oregon State University, present a tutorial on the design and operation of incremental $\Delta\Sigma$ ADCs for high-resolution energy-efficient sensor interfaces. Several single-loop and cascade topologies are introduced and the use of multi-step extended counting scheme is discussed as an effective method to improve resolution and energy efficiency.

The last paper of this special issue, contributed by Qazi and Dabrowski from Linköping University, presents a tutorial study of passive SC $\Delta\Sigma$Ms using a comparator as the only active building block. The paper includes a detailed description of behavioral models and analysis of main circuit errors affecting the performance of passive $\Delta\Sigma$Ms. A chip prototype integrated in 65-nm CMOS is used as a demonstration vehicle of the presented models and theoretical analyses, featuring 71-dB SNDR within 500-Hz signal bandwidth with 0.47 μW power consumption.

To conclude this guest editorial, we would like to express our deepest gratitude to all authors contributing to this special issue, for their excellent research, hard work and great efforts to write their papers and to address their revisions on time. We are also grateful to the legion of reviewers that helped to review the submitted and re-submitted manuscripts, giving always a prompt, detailed and constructive feedback. Finally we wish to thank the Senior Editorial Board of JETCAS, and specially the Editor-in-Chief, Dr. Manuel Delgado-Restituto, and the Deputy Editor-in-Chief, Dr. Yen-Kuang Chen, for giving us the opportunity to organize this special issue.

We are in debt with all of them, because they allowed us to present readers a special issue with the highest quality (resolution) within the required time to publication (speed). This is indeed a well-known compromise for us as $\Delta\Sigma$ designers.

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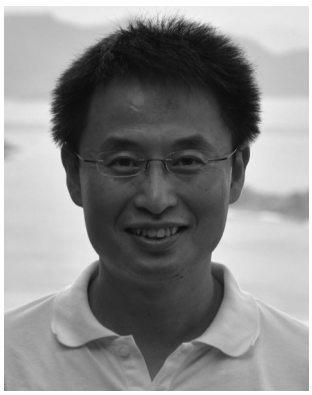
Dr. Schreier was a recipient of the 2002 ISSCC Lewis Winner Best Paper Award as well as the 2006 ISSCC Beatrice Winner Award.



Kong-Pang Pun received the B.Eng. and M.Phil. degrees in electronic engineering from the Chinese University of Hong Kong, in 1995 and 1997, respectively, and the Ph.D. degree in Electrical and Computer Engineering from the Instituto Superior Técnico, Technical University of Lisbon, Lisbon, Portugal, in 2001.

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