

# Guest Editorial

## Low-Power, Adaptive Neuromorphic Systems: Devices, Circuit, Architectures and Algorithms

**T**HIS special issue of the IEEE JOURNAL ON EMERGING TOPICS IN CIRCUITS AND SYSTEMS (JETCAS) aims to demonstrate the latest research progress in the design of adaptive neuromorphic systems and cuts across all the areas from devices and circuits to architectures and algorithms.

The recent success of “Deep neural networks” (DNN) has renewed interest in bio-inspired machine learning algorithms. DNN refers to neural networks with multiple layers (typically two or more) where the neurons are interconnected using tunable weights. Though these architectures are not new, availability of lots of data, huge computing power and new training techniques (such as unsupervised initialization, use of rectified linear units as the neuronal nonlinearity, regularization using dropout or sparsity, etc.) to prevent the networks from overfitting have led to its great success in recent times. DNN has been applied to a variety of fields such as object or face recognition in images, word recognition in speech or even natural language processing and the success stories of DNN keep on increasing every day.

However, the common training method in deep learning, such as back propagation, tunes the weights of neural networks based on the gradient of the error function, which requires a known output value for every input. It would be difficult to use such supervised learning methods to train and adapt to real-time sensory input data that are mostly unlabeled. In addition, training and classification phases of deep neural networks are typically separated, such that training occurs in the cloud or high-end graphics processing units, while their weights or synapses are fixed during deployment for classification. However, this makes it difficult for the neural network to continuously adapt to input or environment changes in real-world applications. By adopting unsupervised and semi-supervised learning rules found in biological nervous systems, we anticipate to enable *adaptive* neuromorphic systems for many real-time applications with a large amount of unlabeled data, similar to how humans analyze and associate sensory input data. Energy-efficient hardware implementation of these adaptive neuromorphic systems is particularly challenging due to intensive computation, memory, and communication that are necessary for online, real-time learning and classification. Cross-layer innovations on algorithms, architectures, circuits, and devices are required to enable adaptive intelligence especially on embedded systems with severe power and area constraints.

With the huge push towards embedded intelligence coming from many different industries, it is the right time for the CAS society to assimilate research progress in all areas of adaptive neuromorphic systems. This special issue aims to provide the readers with a good summary of the field as well as some exciting recent work. In response to this special issue call, we received many excellent submissions which went through a rigorous peer review process involving at least 3 reviewers. The final issue has 12 submissions remaining including one overview paper. Review was carried out with emphasis placed on quality of the work, fitness to the scope of this special issue as well as balance of topics.

This issue contains a survey paper and 11 papers divided into four broad topics: (A) Analog Circuits blocks for online learning systems (B) Novel Algorithms (C) Cross layer optimization and (D) Novel Applications of Neuromorphic Circuits.

The special issue starts with a survey paper by Arindam Basu *et al.* titled “Low-Power, Adaptive Neuromorphic Systems: Recent Progress and Future Directions” that describes recent progress in this field as well as future directions and applications. It starts off by describing novel algorithms and gives a historical perspective of the evolution of adaptive systems. Next, different non-volatile memory devices used in neuromorphic systems are presented and compared. Following this, the authors describe innovative circuits in CMOS that support adaptive synapse design. Next, different architectures for large scale neuromorphic systems are compared and recently fabricated integrated circuits are surveyed. Finally, different emerging applications requiring adaptive neuromorphic systems such as brain-machine interfaces and robotics are described.

Following this survey, we have two papers focusing on Analog Circuits blocks for online learning systems. Analog circuits are a promising candidate for achieving low-power, low-area implementations of neuromorphic circuits. Also, some of the common problems with analog circuits, such as noise and mismatch can be elegantly solved through learning and adaptation in neuromorphic systems.

The first paper entitled “SoC FPAA Hardware Implementation of a VMM+WTA Embedded Learning Classifier” by S. Shah *et al.* presents circuit details of vector-matrix-multiply (VMM) and k-Winner-Take-all (WTA) classifier structure. The field programmable analog array (FPAA) implementation includes the feedforward computation, spectral decomposition and classification, as well as the basic training approach. The classifier used a 12x3 VMM classifier followed by a 3 input,

3 output WTA. This paper has a corresponding paper describing algorithmic details in this same issue.

The second paper entitled “Analog Spike-Timing-Dependent Resistive Crossbar Design for Brain Inspired Computing” by C. Zhao, *et al.* describes an inter-spike interval (ISI) based resistive crossbar neuromorphic design, built with the standard CMOS technology, is proposed. A test bench of video frames consisting one person rotating head from 0 to 75 degrees with an increment of 15 degrees has been employed. The results showed that the ISI code has better performance in both recognition rate and converging speed.

The next three papers present novel algorithms for adaptive neuromorphic systems. They cover different aspects such as memory in spiking neural networks, stochastic learning for RRAM synapses and algorithms for learning on field programmable analog arrays.

The first paper in this group by P. Panda *et al.* with the title “ASP: Learning to Forget with Adaptive Synaptic Plasticity in Spiking Neural Networks” describes a novel unsupervised learning rule Adaptive Synaptic Plasticity (ASP) that addresses “catastrophic forgetting” in spiking neural networks (SNNs). ASP integrates an adaptive weight decay mechanism, which balances gradual forgetting and immediate learning, to construct a stable-plastic self-adaptive SNN. Compared to traditional spike timing dependent plasticity (STDP), ASP demonstrated superior accuracy especially for noisy handwritten digit recognition.

The second paper in this group entitled “VMM + WTA Embedded Classifiers Learning Algorithm Implementable on SoC FPAA Devices” by J. Hasler, *et al.* presents training of classifiers of a single layer of a vector-matrix-multiply (VMM) and a single layer of a k-Winner-Take-all (WTA) on a large scale field programmable analog array (FPAA). A mathematical framework is utilized to allow for transformations and simplifications that reduce system complexity. It was measured in FPAA hardware. Assuming a minimum time for any symbol of 40ms, the classifier correctly recognized the results every time.

The last paper in this section titled “Stochastic Learning in Neuromorphic Hardware via Spike Timing Dependent Plasticity With RRAM Synapses” by G. Pedretti *et al.* proposes to use resistive switching memory (RRAM) to overcome the lack of bio-realistic and scalable devices in current neuromorphic technology. It includes perceptron-like neuromorphic hardware capable of spike timing dependent plasticity (STDP), and its operation under stochastic learning conditions. The system is capable of on-line learning for both static and dynamic patterns. Noise is shown to improve learning time and decrease false fire, although exceeding a certain noise density causes unstable learning.

After this, we have set of five papers on cross-layer optimization for neuromorphic systems. All of these papers deal with issues pertaining to multiple layers of the design including device, algorithm, circuit and architecture.

The first paper in this set entitled “Multiscale Co-Design Analysis of Energy, Latency, Area, and Accuracy of a ReRAM Analog Neural Training Accelerator” by M. Marinella *et al.* presents an analog crossbar circuit block designed to process

three key kernels required in training and inference of neural networks. It is shown that the analog accelerator has a 270x energy and 540x latency advantage over a similar block utilizing only digital ReRAM. It takes only 11 fJ per multiply and accumulate (MAC). Compared to an SRAM based accelerator, the energy is 430X better and latency is 34X better.

The next paper entitled “Stuck-at Fault Tolerance in RRAM Computing Systems” by L. Xie, *et al.* presents a fault-tolerant framework for RRAM-based Computing System (RCS). A Mapping Algorithm with inner fault tolerance (MAO) is proposed to convert matrix parameters into RRAM conductances in RCS and tolerate Stuck-At-Faults (SAFs) by fully exploring the available mapping space. This paper also presents two baseline redundancy schemes to ensure that RCS is effective when the percentage of faulty RRAM cells is high.

The third paper entitled “Mitigating Asymmetric Nonlinear Weight Update Effects in Hardware Neural Network Based on Analog Resistive Synapse” by Chang *et al.* proposes new techniques to address the asymmetric nonlinear weight update issue in analog RRAM based neural network hardware design. By engineering the nonlinear activation function and employing a threshold weight update scheme, a two-layer perceptron network showed weight update noise suppression and self-adaptiveness to RRAM devices with high asymmetric nonlinearity.

The fourth paper entitled “Memristive Mixed-Signal Neuromorphic Systems: Energy-Efficient Learning at the Circuit-Level” by G. Chakma *et al.* proposes a memristive neuromorphic system for high power and area efficiency. The mixed-signal spiking based system design also includes synchronous digital long term plasticity (DLTP), an online learning methodology to train the neural networks during the operation phase and improve the efficiency in learning considering the power consumption and area overhead.

The last paper in this group entitled “Memristor Crossbar Tiles in a Flexible General Purpose Neural Processor” by D. Mountain *et al.* presents the use of smaller crossbar tiles that can be flexibly combined to create a variety of crossbar sizes and aspect ratios to more closely fit the ideal sizes required. A general purpose neural processor using a single tile size is demonstrated and compared to highly specialized neural processor designs using multiple, optimally sized custom crossbars.

The last section of this special issue deals with novel applications of neuromorphic circuits. It has one paper describing the design of a neuromorphic digital to analog converter using memristors. The paper written by L. Danial with the title “DIDACTIC: A Data-Intelligent Digital-to-Analog Converter with a Trainable Integrated Circuit Using Memristors” describes a new technique to train the memristors that are used in the weighted resistance in a digital-to-analog converter (DAC). The authors developed a supervised learning algorithm termed “binary-weighted time-varying gradient descent” train the on-chip neural network in real time to configure an adaptive four-bit DAC.

For this special issue, the Guest Editors first would like to extend their gratitude to the authors who committed time and energy to contribute their technical excellence and insights

for this issue. We also would like to thank volunteer reviewers for providing valuable comments and suggestions to comply with the high-quality standards of JETCAS. We are grateful to the Editor-in-Chief, Yen-Kuang Chen, the Deputy Editor-in-Chief, Eduard Alarcon, as well as the Senior Editorial Board for their consistent support and advices. Last but not least, we are grateful to IEEE Publishing Operations personnel for their great efforts and patience in finalizing this special issue. We hope this special issue will interest a large portion of related researchers and facilitate further progresses in this important and emerging research area.

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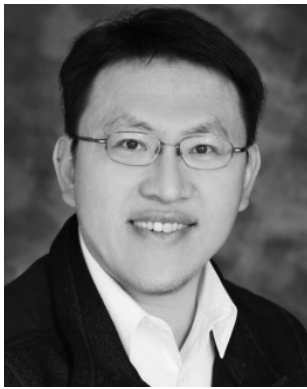
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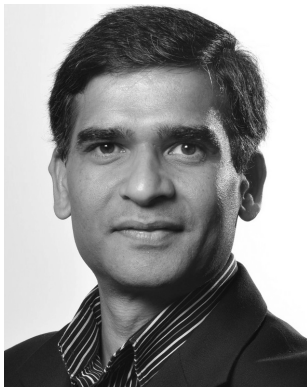


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