Multi-State Memristors and Their Applications: An Overview

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***Abstract*—Memristors show great potential for being integrated into CMOS technology and provide new approaches for designing computing-in-memory (CIM) systems, brain-inspired applications, trimming circuits and other topologies for the beyond-CMOS era. A crucial characteristic of the memristor is multi-state[1] switching. Memristors are capable of representing information in an ultra-compact fashion, by storing multiple bits per device. However, certain challenges remain in multi-state memristive circuits and systems design such as device stability and peripheral circuit complexity. In this paper, we review the state of the art of multi-state memristor technologies and their associated CMOS/Memristor circuit design, and discuss the challenges regarding device imperfection factors, modelling, peripheral circuit design and layout. We present measurement results of our in-house fabricated multi-state memristor as an example to further illustrate the feasibility of applying multi-state memristors in CMOS design, and demonstrate their related future applications such as multi-state memristive memories in machine learning, memristive neuromorphic applications, trimming and tuning circuits, etc. In the end, we summarize past and present efforts done in this field and envisage the direction of multi-state memristor related research.**

***Index Terms*—Memristor, RRAM, memristive circuits and systems, multi-state memristors, multi-bit RRAM, AI hardware.**

I. Introduction

In the past decades, the semiconductor industry has steadily followed Moore's law by advancing to deeper technology nodes. In view of the possibility that CMOS technology may eventually approach its physical limit, new devices have been proposed to be integrated with the existing technology. At the same time, the pursuit of novel computing architectures such as neuromorphic computing has been driven by the need for addressing the data scalability limits in the traditional von-Neumann architectures. The rapid technological advances of memristors promise to resolve both issues, improving the capability of electronics beyond what the CMOS cannot achieve alone and rendering unconventional computing architectures that are becoming viable [1].

Since Leon Chua postulated the concept of the memristor in 1971 [2], several devices with similar characteristics to the conceptual memristor had been reported in the literature [3–7], but the conceptual memristor was not linked to any physical devices in the following three decades. In the early 2000s, an increasing number of Metal-Oxide-Metal (MOM) devices with non-volatile resistive switching behaviour started to emerge, such as the ones in [8–11]. One typical example is a solid-state non-volatile device based on the Copper-Tungsten oxide whose resistance can be switched by the applied write current [12]. In 2008, HP lab first linked a non-volatile resistive switching device based on Pt-TiO_2-Pt layered structure [13] to the theoretical concept of a memristor. Since then, memristors have attracted increasing attention from the research community, and memristors based on different types of materials have been reported. More importantly, memristors' unique features such as non-volatility, small feature size (down to 2nm [14]), low power consumption, and compatibility with CMOS technology for monolithic integration render them good candidates for using in various applications [15–21].

Among all of the promising advantages of the memristor, the multi-state switching capability is a unique feature. Since 2008, using the multi-state characteristic of memristors in next-generation electronics has become a popular research direction because a single memristor can potentially replace multiple transistors, while performing the same logic function [22]. Nevertheless, multi-state memristors still face various challenges including retention degradation, vulnerability, device-to-device variations, cycle-to-cycle variations, process voltage temperature (PVT) variations, inaccurate modelling, complex control logic and excitation circuits, etc [23–26].

In this paper, we review multi-state memristors with different bi-layer oxide combinations and the state-of-the-art

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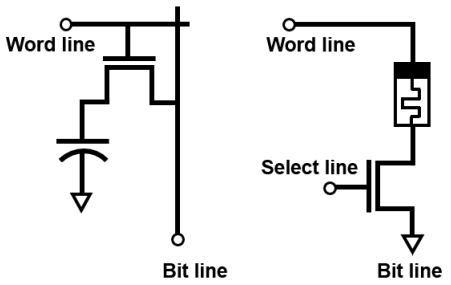
[1]also often referred as multibit, multi-state, and multi-level



(a) (b)

Fig. 1: (a) A conventional DRAM consists of 1T1C cells. Each capacitor stores 1-bit information. (b) A multi-state 1T1R memristor cell can in principle store up to 5.5-bit of information [28].

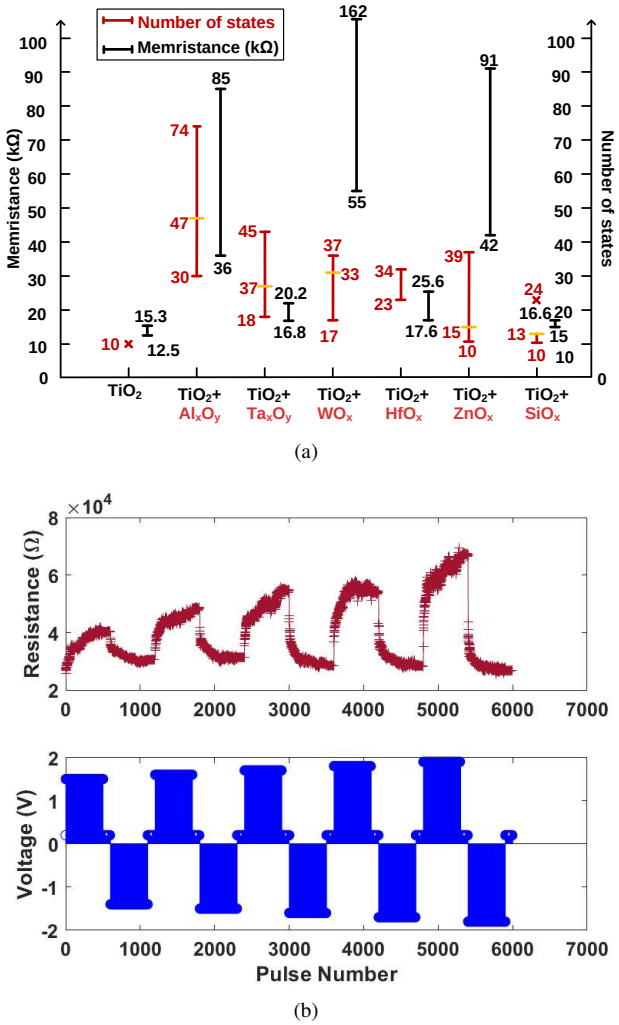
memristive systems. We mainly analyse the difficulties and challenges that lie in the memristive circuits and systems design, and provide an overview of the multi-state memristors related applications. The rest of the paper is organized as follows: Section II reviews multi-state memristors and the state-of-the-art CMOS/Memristor systems. Section III illustrates the design challenges of multi-state memristive systems including device defects, device modelling, peripheral circuits design, and layout and post-processing in CMOS. Section IV introduces three major categories of applications where multi-state memristors can enhance overall performance. Section V discusses high-level insights and research directions for multi-state memristive systems, and Section VI concludes the paper.

II. Multi-state Memristor Devices and Systems

Shortly after the memristor was realised as a solid-state device in [13], the concepts of exploiting a multi-state memristor to realise logic functions [22] and memory [27] were proposed. Taking a random-access-memory (RAM) as an example, as shown in Fig.1, traditional DRAM employs 1 transistor and 1 capacitor (1T1C) to store 1-bit information in one cell, whereas in a multi-state 1 transistor and 1 memristor (1T1R) cell, a single memristor can store up to 5.5-bit information in principle [28]. In addition, the capacitor in the DRAM cell needs to be refreshed periodically to deal with charge leakage. The memristor's non-volatility not only prevents the information loss due to the leakage, but also enables fast and safe power-cycling. Compared with other RAMs such as SRAM, memristive RAM can achieve higher density while maintaining the same speed [29]. In this section, we review the multi-state memristor devices based on different bi-layer oxides and the performance of the state-of-the-art multi-state memristors in integrated 1T1R crossbar arrays.

A. Multi-State Memristor Device

Metal-oxide-metal (MOM) memristors have been reported with many electrode material and active material combinations, which lead to different specifications and performance. For example, a TiO_x memristor with gold electrodes is almost completely volatile, while the one with platinum electrodes is



(a)

(b)

Fig. 2: (a) Memristors based on different oxide combinations exhibit different resistive state ranges and multi-state switching capabilities. The monolayer device (only TiO_2) has lower resistance range and number of states compared with the bi-layer devices. (b) The Pt-TiO_2+Al_2O_3-Pt memristor exhibits multi-state switching behaviour. The stimulus consists of sets of programming voltage pulses with increasing amplitude at 500 pulses per voltage level and pulse width of 10μs. Between each programming process, there are 100 reading pulses with the same amplitude of 0.2V and the same pulse width of 10μs.

almost completely non-volatile. Besides the electrode materials which determine the volatility of a memristor, active materials determine the multi-state switching behaviour. Among different bi-layer oxide combinations, the most popular ones use Ta_2O_5, HfO_2 and TiO_2 as their main active oxides and a variety of metals as electrodes [30–34]. Every combination behaves differently as a multi-state device. These differences include the values of the high and low resistive states (HRS, LRS) and the number of distinguishable states indicated by different resistive switching ranges. The resistive switching range is important because it affects the trade-off among power consumption, linearity, and resolution of the peripheral circuit design, whereas independent and distinguishable states affect the stability, reliability, and reconfigurability of the multi-state memristor. Here, a comparison is made based on the work in [28] analysing 7x types of memristors, of which

TABLE I: SUMMARY OF BEHAVIOUR OF MULTI-STATE MEMRISTORS BASED ON DIFFERENT BI-LAYER STRUCTURES [28]

Bi-layer Oxide	TiO_2	TiO_2 +Al_xO_y	TiO_2 +Ta_xO_y	TiO_2 +WO_x	TiO_2 +HfO_x	TiO_2 +ZnO_x	TiO_2 +SiO_x
Number of States	10	47	37	33	23	15	13
LRS (kΩ)	12.5	36	16.8	55	17.6	42	15
HRS (kΩ)	15.3	85	20.2	162	25.6	91	16.6
Range (kΩ)	2.8	49	3.4	107	8	49	1.6
HRS/LRS Ratio	1.2	2.4	1.2	2.9	1.5	2.1	1.1
Equivalent Number of Bits	3.3	5.5	5.2	5	4.5	3.9	3.7

6x feature different bilayer oxide combinations (TiO_x is the "base layer" in all cases) and 1x is a simple monolayer device (only TiO_x "base layer" oxide). As shown in Fig.2 (a) and Table I. The monolayer memristor exhibits the lowest number of states, smallest resistive switching range, and low HRS/LRS ratio. On the other hand, memristors based on TiO_2 with Al_xO_y[2], WO_x, and ZnO_x exhibit promising multi-state capability. In particular, the TiO_2+Al_2O_3 bi-layer shows the highest number of states and has been leveraged in different integrated applications such as a one-time-programming memristive memory (RRAM) in [35]. Fig.2 (b) shows an example of the measurement result of a Pt-TiO_2+Al_2O_3-Pt memristor. After applying voltage pulses with an increasing amplitude, the memristor can be written to different resistance states.

The retention measurement is another important process for characterizing a memristor. Memristors experience retention degradation after a certain time or in different temperatures, which leads to undesired volatile behaviours. For example, in the study reported in [28], at room temperature, the Pt-TiO_2+Al_2O_3-Pt memristor in Table I only achieves 10 states after 8 hours of electroforming[3]. When baking the memristor with 85°C, the memristor can only retain 4 states. Similarly, the SiN-$TiNO_x$+WO_x+$TiNO_x$-SiN memristor with 8 states in [36], the W-Ta+TaO_x-Pt memristor with 8 states in [37], and the Au-Al_2O_3+HfO_2-TiN memristor with 16 states in [38] only retain their states up to 85°C. Since retention is an inevitable problem when employing memristor's multi-state characteristic, it has to be carefully considered and handled.

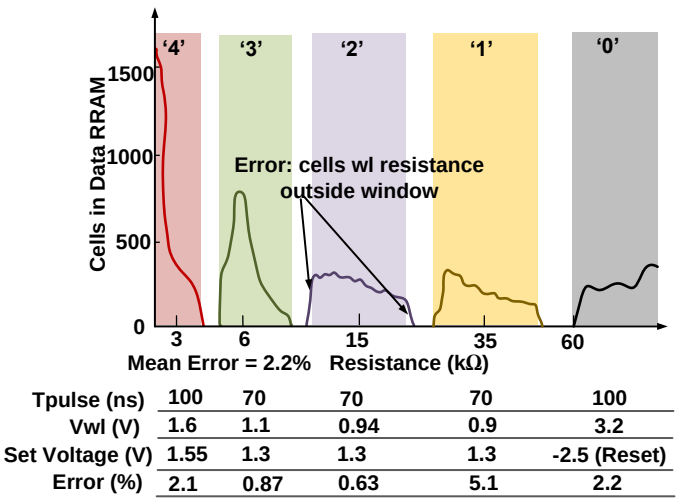
B. Multi-State Memristive System State of the Art

Although stand-alone memristors range from supporting 10 to 47 states (Table I), an essential problem is assessing this capability within a CMOS/Memristor system. The highest reported number of independent states in a memristive neural network is 32 [24], which is equivalent to 5x bits. Yet, when employing these states, multi-state memristors in an array are unreliable and experience high device-to-device and cycle-to-cycle variations, low yield rate, and limited precision [24], which limit applicability in multi-state memristive systems.

The past five years have seen the emergence of fully integrated memristive systems, especially RRAM in neuromorphic computing [35, 39–48]. Among these works, the multi-state

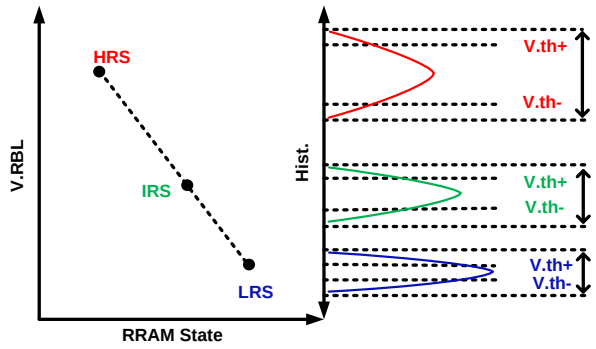
[2] Al_xO_y stands for Aluminum Oxide such as Al_2O_3

[3] An electrical biasing routine undertaken to electrochemically activate a device after manufacturing and before it is used for the first time. This can frequently involve voltages many times larger than normal operating conditions.



Tpulse (ns)	100	70	70	70	100
Vwl (V)	1.6	1.1	0.94	0.9	3.2
Set Voltage (V)	1.55	1.3	1.3	1.3	-2.5 (Reset)
Error (%)	2.1	0.87	0.63	5.1	2.2

(a)



(b)

Fig. 3: (a) The RRAM design in [40] presents 5 independent states in a single cell. Each state is defined within a resistance range, and error windows are defined between each resistance range. (b) The fully integrated RRAM in [46] exhibits three resistance states (i.e HRS, IRS and LRS) and can store 1.58 bit/cell.

RRAM exhibits its advantage of storing more information in a single cell [35, 40, 45, 46]. Table II shows the state-of-the-art RRAM systems, and few observations are acquired. Although weight resolution in an RRAM system can reach up to 20-bit in [47], the highest reported number of states in a single RRAM cell is 5, which is equivalent to 2.3-bit information storage per cell [40]. As shown in Fig.3 (a), in this work, error windows are defined between resistance ranges to avoid the collision. When writing to a desired state, write voltages are precisely controlled. This method is also adopted in other multi-state RRAM designs such as the one proposed in [29]. In 2021, a fully integrated RRAM exhibiting 3 independent states that can be employed to store 1.58 bit/cell of information was reported [46]. As shown in Fig.3 (b), by using this approach, an intermediate resistance state (IRS) is used to achieve 3 states. Another RRAM employing 3 states is also adopted in [35], a fuse state is employed beyond the HRS. Nevertheless, the multi-bit weight does not correspond to a true multi-state memristor cell, among all the state-of-the-art memristive systems, most of them still only employ two states, HRS and LRS, to achieve reliable switching.

TABLE II: COMPARISON OF THE STATE-OF-THE-ART RRAM DESIGNS

	ISSCC 18 [39]	VLSI 18 [35]	ISSCC 19 [40]	ISSCC 19 [41]	ISSCC 20 [42]	ISSCC 20 [43]	ISSCC 20 [44]	SSCL 20 [45]	CICC 21 [46]	ISSCC 21 [47]	ISSCC 21 [48]
Technology	65nm	14nm	130nm	55nm	130nm	130nm	22nm	90nm	40nm	40nm	22nm
Supply (Volt)	1.0 V	5.5 V	0.71-1.2 V	1.0 V	4.2 V	1.8 V	0.7-0.9 V	1.2 V	0.9 V	0.9 V	0.8 V
Multi-bit Weight Memristor Cell	No	**Yes**	**Yes**	No	No	No	No	**Yes**	**Yes**	No	No
RRAM Type	Digital	Digital	Digital	Digital	Analog	Analog	Digital	Digital	Digital	Digital	Digital
Array Size	512 x 256	n/a	256 x 16	256 x 512	784 x 784	256 x 256	512 x 512	128 x 64	256 x 256	256 x 256	1024 x 512
Array Type	1T1R	1S1R	1T1R	1T1R	2T2R	1T1R	1T1R	1T1R	1T1R	1T1R	1T1R
Max Input Resolution	1 bit	n/a	1 bit	2 bit	1 bit	1 bit	4 bit	1 bit	1 bit	8 bit	8 bit
Max Weight Resolution	Ternary	**1.58 bit/cell**	**5.6 bit 2.3 bit/cell**	3 bit	Ternary	Analog	4 bit	**2 bit/cell**	**1.58 bit/cell**	8 bit	8 bit
Max Output Resolution	3 bit	n/a	1 bit	3 bit	8 bit	1 bit	11 bit	1 bit	4 bit	20 bit	14 bit
Write Verification	No	No	**Yes**	No	No	No	No	**Yes**	**Yes**	**Yes**	No
Sensing mode	Current	Current	n/a	Current	Current	Voltage	Current	Voltage	Voltage	Voltage	Voltage

III. Multi-State CMOS/Memristor System Design Challenges

Multi-state memristors provide different methodologies for designing future electronics and applications. In the previous section, a few integrated multi-state RRAM systems have shown their promising potential. However, not all technical details about the technologies are publicly available. In this section, we analyse the feasibility and challenges of the multi-state memristor technologies and we combine the analysis with the measurement results from our in-house fabricated memristor devices.

A. Multi-State Memristor Device-Level Imperfection Factors

Multi-state memristors of different structures have been reviewed in Section II-A, however, memristors still suffer from device and process variations, inaccurate writing process, retention degradation, low yield rate, etc. Combining with the observations and measurement results of our in-house fabricated Pt-TiO_2-Pt memristor, we analyse the challenges of using multi-state memristors in a large CMOS array.

1) Case Study: Measurement Result of an in-house Fabricated Memristor: Fig.4 (a) shows the micrograph of the multi-state Pt-TiO_2-Pt memristor. To fully characterize the memristor, a complete testing platform is set up as shown in Fig.4 (c). A customised memristor testing platform and a software interface developed in [49] are adopted to write and read the memristor-under-test (MUT) with adjustable voltage pulses of different amplitude, number, and frequency. In Fig.4 (b), two probes are connected to the positive and negative terminals of a single memristor to minimize the factors that can potentially affect its characteristics. Fig.4 (d) shows the IV characteristics of the MUT. A pinched hysteresis loop is formed successfully. By applying different amplitudes of voltage pulses while fixing equal pulse number and pulse width and vice versa, the memristor can be written to different states. An example of the measurement results is shown in Fig.4 (e).

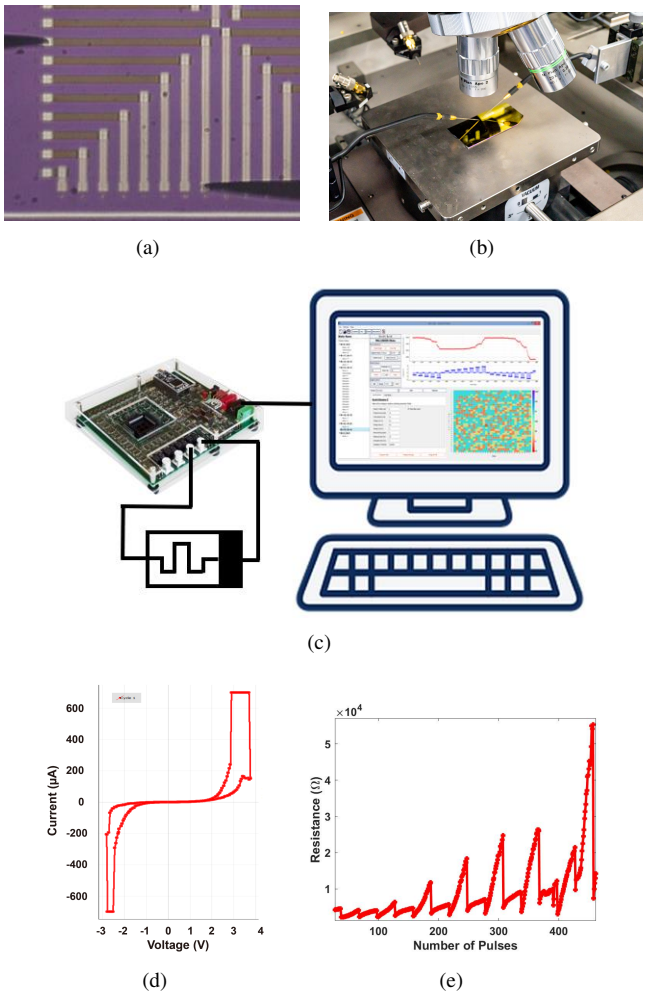


Fig. 4: (a) The micrograph of an in-house fabricated Pt-TiO_2-Pt memristor. (b) Two probes are connected to the terminals of the memristor to minimize the undesired effects. (c) The complete testing setup. (d) The pinched hysteresis loop of the memristor after electroforming. (e) An example of the measured results indicates the Pt-TiO_2-Pt memristor reaches different resistive states.

While these measurements were performed and results were obtained, we identified a few difficulties of using the multi-state memristors in integrated circuits design. First of all, multi-state switching specification in integrated circuits design is stricter. A properly defined state has to be accurately rewritten by the same pulse train which is often measured within 2-3σ. This needs a "program and verify" approach to guarantee the switching behaviour, but it adds circuit complexity. Under the same testing condition and voltage pulses, we observed that the MUT did not always reach the desired state, the successful forming and writing process are not always perfectly repeatable. This leads to some states becoming incompatible and cannot be considered as a stable state. Moreover, memristors are sensitive to the voltage above their threshold, and they can be damaged with high voltage

when performing electroforming. Yet, there is not a constant threshold voltage observed that can be applied to all the MUTs. Thus, when designing a crossbar array, this variation has to be considered to avoid broken memristors. Furthermore, based on our measurements, "designed non-volatile" memristors are not non-volatile under all possible configurations: it depends on the forming process, pulse amplitude, and the current resistance state (e.g. larger resistance state is more volatile). This has been discussed in [50], and needs further investigation. In addition, as discussed in Section II-A, retention degradation must be considered in a CMOS/Memristor system. Although there are reported investigations of retention such as in [23], and methods to improve the stability such as the multilevel incremental step pulse with verify algorithm in [51], there is not a commonly adopted method to overcome the volatile behaviour and guarantee data retention.

B. Memristor Modelling

Practically exploiting the existence of multiple states of a memristive device for circuit applications requires a compact device model. The model must accurately simulate the nature of the various states observed in real devices. Measurements have shown that not all aforementioned device states are sufficiently reliable for circuit applications. For instance, certain states are meta-stable, and this means a device in such state cannot persist its state over our interested timescales. Stable states on the other hand are more useful for traditional multi-bit circuit and memory applications. From a circuit applications point of view, we are interested in constructing the relationship between the characteristics of the applied stimulus and the subset of device states that can be accessed by the device from some initial states, upon the application of the stimulus. Furthermore, we are interested in the relationship among different states for a given input (i.e. determining whether a given state can be obtained by using alternative sets of programming pulses).

A large class of models in literature such as [52–54] are deterministic models that are constructed as a set, consisting of a differential equation and an algebraic equation. A typical set is shown in (1) and (2).

$$\frac{ds}{dt} = f_u(u,s) f_w(s) \tag{1}$$

$$i(t) = G(s,u) \cdot u(t) \tag{2}$$

Here, s is the internal modelling state variable, $f_u(u,s)$ is the input sensitivity function, and $f_w(s)$ is a window function. The memristor conductance can be derived from the state variable governed by (1) and the input $u(t)$ using an appropriate function $G(s,u)$. The current through the device $i(t)$ and voltage across it $u(t)$ are therefore related by (2).

In such a model, a given input stimulus and an initial condition specify a unique deterministic trajectory in the state-space, towards a terminal state. Upon reaching the terminal state, no further change in state occurs despite the application of input. In practice, these terminal states are defined by using suitable window functions. In most models the window functions simply bind the state variable into a valid range used for modelling. In more complex models such as [55], the window is a function of the state variable and the input stimulus and can therefore additionally describe input-dependent stable states to which the memristance saturates. Whilst this is useful in cases where the device can be allowed to reach a steady state, the models are not yet upgraded to account for the transient volatility that describes the state of the device shortly after the stimulus is removed. In practice, all valid values of the memristance are not stable and the memristance typically decays to another more stable value. The basic state evolution differential equation (1) can be extended to model such behaviour by dividing the state space into stable regions and unstable regions. Furthermore, relaxation dynamics can also be introduced to describe volatile behaviour from the unstable states towards the stable states. The modelling approach of [56] introduces a single stable state into the dynamics via the following addition to (1):

$$\frac{ds}{dt} = \left(f_u(u,s) - \frac{s-\epsilon}{\tau} \right) f_w(s) \tag{3}$$

In (3) the only stable state is the value of s for which $\frac{ds}{dt} = 0$. Typically $f_u(u=0,s) = 0$, thus the parameter ϵ is equal to the value of this single stable state in this model. The models presented in [57] and [58] extend this further by allowing the parameter ϵ to be a dynamic variable, governed by its own differential equation, driven by the input stimulus. Therefore, in these models, the stable state of (3) is variable and depends on the history of the input stimulus. Another approach to introduce a series of stable and unstable states in the governing dynamics is to impose a potential-energy-like function on the dynamics, whose minima correspond to stable states and maxima correspond to unstable states. For example, [59] introduces a combination of exponential functions and a sinusoid function to model the interfacial energy and periodicity of the transport dynamics respectively. While the model accuracy issue caused by numerical integration of model equations have been addressed [60, 61] and there are ongoing efforts to develop accurate models for specific applications [62–64], the multi-state switching behaviour has not been modelled to the comprehensiveness required for robust circuit design. With more and more characterization data becoming available, it is expected that the memristor model will be extended to cover switching metastability, temperature dependencies, and also the electroforming process [65].

C. Circuits Design and Implementation

Peripheral circuit design in multi-state memristor arrays is more challenging than in bi-state memristor arrays. Fig. 5 shows a common 1T1R architecture of the memristor crossbar array. When writing a memristor to the desired state, row and column selectors are used to select a device from the array. One terminal of the memristor is connected to a pulse generator and other terminals are connected to the ground or a virtual ground. The pulse generator then sends programming signals to the selected memristor. The read operation faces more difficulties than the write operation. When reading the

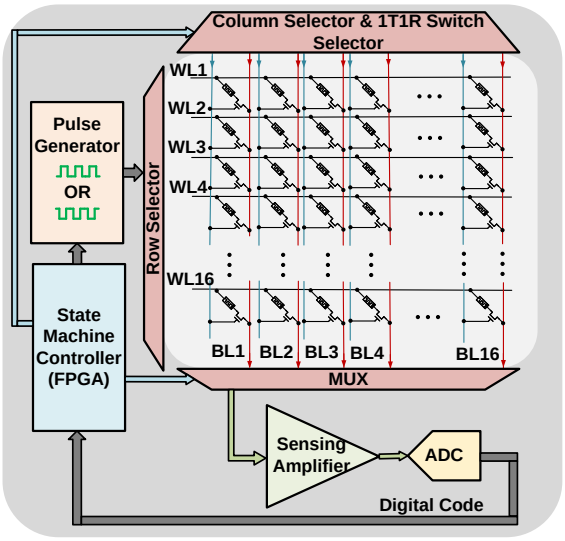


Fig. 5: A common architecture of a 1T1R RRAM architecture. The pulse generator generates either writing or reading pulses depending on the instructions from the processor. Either the readout current or voltage is sensed by the peripheral circuitry and converted to digital codes by an ADC. The converted digital codes are sent back to the processor for signal processing.

memristance [4], low voltage pulses are applied to the selected memristor, while the resulting current is measured. The readout voltage has to be sufficiently low to avoid changing the memristance. The resulting current is interfaced with dedicated readout circuitry and gets digitized. Referring to Table II, both voltage mode and current mode sensing are adopted in state-of-the-art designs. Current mode sensing provides higher speed and larger sensing margin [26]. However, current mode sensing is not preferred in a multi-state memristive system due to its higher noise nature than voltage mode sensing, which leads to inaccurate readout result when the memristor has more states. Besides, current mode sensing also leads to large static power dissipation [26]. On the other hand, in voltage mode sensing, a current-to-voltage (I2V) circuitry is required. It has been demonstrated in Table I that multi-state memristor with higher HRS/LRS ratio leads to a larger current range. For instance, if an amplifier is used to sense the current, the trade-off among large dynamic range, low input offset, low input referred noise, high open-loop gain, and high linearity must be optimized. When the I2V conversion is finished, a high resolution analog-to-digital converter (ADC) and a digital quantizer are needed to precisely categorize the I2V output voltage to different digital ranges which correspond to different distinguishable resistance states such as the approach shown in Fig.3 (a) [42]. The more states that a 1T1R cell aims to achieve, the higher resolution of ADC is needed. This leads to another trade-off among multi-state switching, power consumption, chip area, and circuit complexity. In addition, to ensure the memristor is written to a desired state, a write-verify circuit is needed [40, 45–47], which leads to a more sophisticated peripheral circuit design. Thus, there is a wide Pareto surface to optimise over and every bit of resolution requested from the memristive

[4]refers to the resistance or the conductance of the memristor depends on different designs

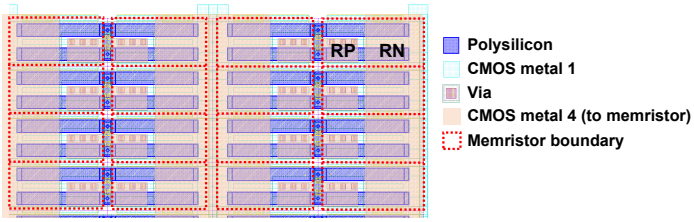


Fig. 6: Layout of a 1T1R array corner with CMOS layers indicating memristor placements. RP links to memristor top electrode and RN connects to its bottom electrode. The insufficient layout data regarding the post-processed memristor hinders the way to perform post-layout analysis for a whole picture.

devices has to be carefully balanced against the costs of the corresponding peripherals.

Hybrid CMOS/Memristor circuits are typically fabricated in two steps: the CMOS parts including the peripheral circuits and the selecting transistors in the 1T1R cells are fabricated using standard CMOS process, and then the memristors are integrated on top of the CMOS through wafer-level post-CMOS processing. Fig. 6 shows an example layout of a 1T1R array chip corner showing the CMOS layers and the boundaries of custom memristor layers. There has been progressed in process design kit development to allow hybrid CMOS/Memristor circuit design using design flows compatible to standard CMOS process [66]. When designing circuit especially for interfacing memristors at a large scale, both layout-dependent and processing-dependent parasitic effects need to be modelled. This will become possible as more data becomes available from post-processed devices on top of CMOS, and a dedicated characterization platform has been constructed to facilitate this development [67].

IV. MULTI-STATE MEMRISTOR APPLICATIONS

A multi-state memristor can be understood as a device that manifests variable resistance values in response to certain input stimulus patterns. This feature means it can be used as a multi-bit memory cell or a resistive trimmer, and also be used to encode or process temporal dynamic signals such as physiological signals. In this section we will discuss about three potential applications corresponding to these characteristics respectively.

A. Next-generation Memory and Computing

The potential to store multiple states in a single memristor cell makes it promising for high-density memory implementation, potentially paving the way for the development of digital and analog memory which will impact the technology landscape of future computing systems. As shown in Fig. 7, a multi-state memristor array is adopted in a conventional von-Neumann computing architecture as an example. The CPU is responsible for constantly adjusting the input data until multi-bit information is stored at a specific memory cell. The high density and low power advantages of the multi-state memristor memory make it a potential candidate to compete with DRAM in the future [1]. However, adopting multi-state RRAM in the von-Neumann architecture leads to the long-distance data

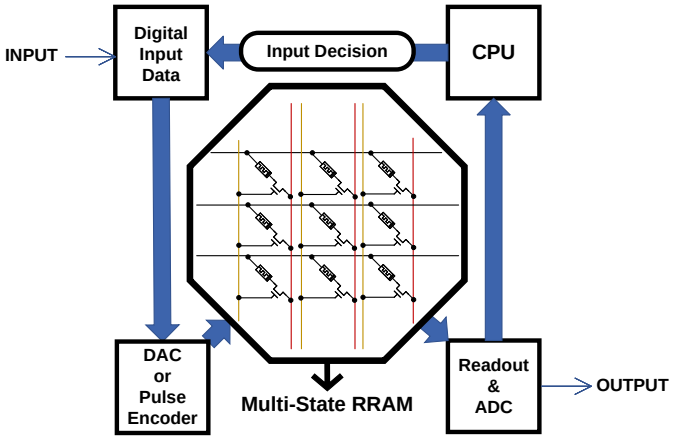


Fig. 7: Multi-state RRAM applied von-Neumann computing architecture. For a typical writing process, the input data is firstly applied to the RRAM as read voltage without changing the memristor's state, the readout data will then be transmitted to the CPU for comparison with an expected value, and a proper write voltage is generated from the CPU to change the state (weight). The closed-loop process continues to work until the information is stored to the multi-state memristor cells.

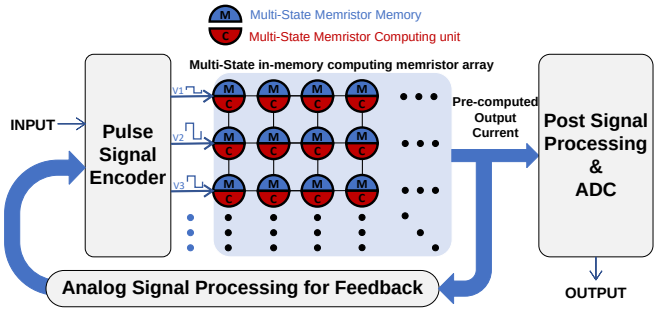


Fig. 8: Analog-based RRAM computing architecture. In a machine learning training process, the input signals are encoded by a pulse signal encoder and then applied to the memristor array. Each memristor cell works as a multi-state memory but also as a computing unit, the computed MAC result is carried by the readout current of every column to realise in-memory processing. The result is transmitted to an analog signal processing circuit and then fed back to the pulse signal encoder to update the write voltage. The final result is post-processed and digitized to the output.

transmission between the CPU and the RRAM, which costs considerable power, area, and more importantly, leads to low processing efficiency [1]. As a multi-bit memory cell, the memristor facilities computing-in-memory (CIM) which addresses this inefficiency, and because it stores the weight and performs Multiple-and-Accumulate (MAC) operation in the analog domain, faster and more power-efficient neuromorphic and artificial neural network hardware were built thanks to this advantage [68–77]. Compared with an SRAM-based CIM, the analog-based RRAM CIM eliminates excess full adders and logic gates, substantially reducing chip area and power consumption. An example of such analog-based in-memory computing array is shown in Fig. 8. Notably, a fully integrated CMOS/Memristor CIM chip which incorporates 3 million analog RRAM cells was presented recently [78]. This chip demonstrates directly the advantages of multi-state memristors for building large-scale artificial intelligence hardware with high energy efficiency, application versatility, and software-comparable accuracy.

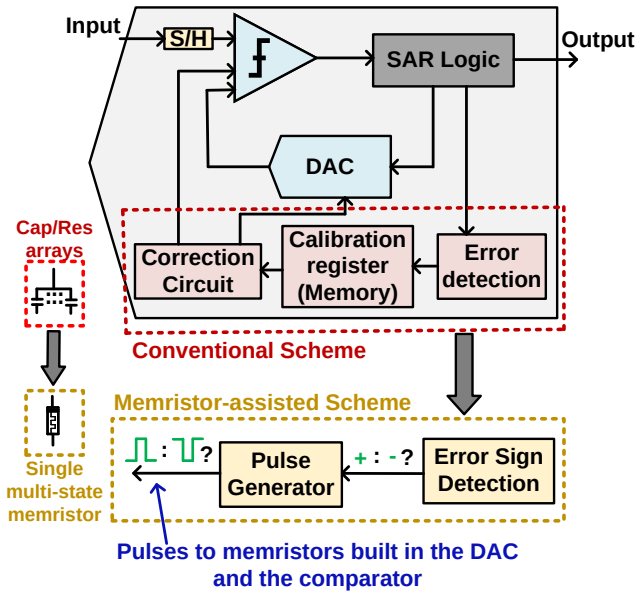


Fig. 9: Conventional SAR ADC calibration scheme assisted by capacitor/resistor arrays and a substitute scheme assisted by multi-state memristors [79]. The MSB of the R-2R DAC is replaced by a memristor and this memristor is considered as a trimming element. The error sign detection logic is similar to the one proposed in [80], and the pulse generator is used to write the memristor to a certain state based on the feedback error sign, the updated memristance leads to a correction on the DAC output level, and thus improve the accuracy of the A/D conversion.

B. Multi-state Memristor for Analog Trimming & Tuning

As early as 1976, laser trimming was used to improve the linearity of an R-2R digital-to-analog converter (DAC) that was constructed by thin-film resistors [81]. The resistance can be adjusted by means of irradiating thin-film resistors with the laser, thus the DAC output level can be trimmed. Compared to the conventional scheme, this laser-trimming approach reduced the complexity of the peripheral calibration circuit but the laser is difficult to be applied to today's integrated circuits. Alternatively, memristors can be used for calibration in the similar way as laser-irradiated thin-film resistors because they both offer variable resistance in principle. In recent years, some studies show that memristors tunability can be employed to trim circuit imperfections (i.e mismatches, offsets) in amplifiers [82] and ADCs [79].

Taking the successive-approximation ADC (SAR ADC) as an example, as shown in Fig.9, in a conventional SAR ADC calibration scheme, the calibration information needs to be stored in calibration registers in advance of trimming the DAC mismatches and comparator offsets. When the resolution of the SAR ADC is increased, more calibration bits are required to maintain good linearity, thus demanding more registers and calibration components (i.e capacitor and resistor arrays) to store the calibration information and correct the errors, which induces larger latency, power consumption, and area. Thanks to the in-memory processing nature of memristor, a smaller, faster and more power-efficient design can be realised by replacing conventional calibration with a memristor-assisted calibration scheme. In Fig.9, calibration registers and correction circuits are no longer required as the memristor itself

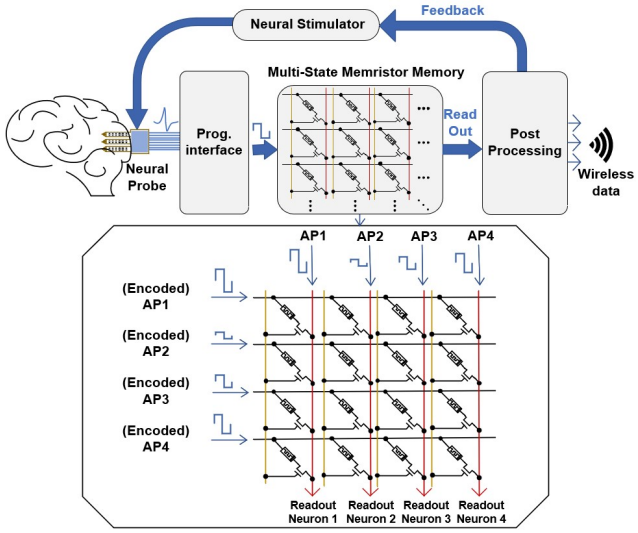


Fig. 10: An envisaged memristor-centric neural interface system. A multi-state memristor array can be used to construct a matching template [83], performing spike sorting algorithms to process the raw data from the high-density neural probe at the front end. After spike sorting, the output data rate is significantly reduced and can thus be transmitted wirelessly to the external hardware. Closed-loop neuromodulation for brain disorder (eg. epilepsy) treatment can be achieved using multi-state memristors to analyse the neural states in real time, providing feedback to the brain through neural stimulation.

can store the calibration information. The calibration can be conducted by applying programming pulses to increase or decrease the memristor resistance according to the error polarity so that the mismatch errors in the DAC and the comparator are minimized. In addition, the multi-state switching property also provides a wider calibration range for the ADC mismatches, which can potentially realise more precise trimming than the conventional approach.

C. Multi-State Memristor for Neural Interfaces

The emerging techniques for using multi-state memristors to perform bio-signal processing have shown promising results in energy efficiency improvement, which is vital for embedding intelligence in future biomedical implants [83–85]. Encoding the neuronal spikes into multi-state memristors results in real-time sub-μV/ch spike detection [84]. In [85], memristors with conductance states programmed to multiple values (1$\sim$20μS) were used to construct coefficients in a low-power finite impulse response (FIR) filter bank, which can process neural local field potentials with two orders of magnitude better energy efficiency than conventional CMOS filters. Significant reductions in circuit area, power consumption, and processing latency in neural spike sorting were achieved using the multi-state memristors to construct template coefficients (4-bit resolution) for template-matching-based classification algorithms [83]. Notably, the retention characteristics reported in [83] ensures a reliable storage of the neuron templates for over 2.7 hours. This satisfies the requirement in typical neural electrophysiological experiments, while periodic refresh operation could be applied for longer experiments or in clinical application scenarios. A multi-state memristor array will prospectively be the core part of a closed-loop neural interface system shown in Fig.10. The state-of-the-art neural probe technologies today support implantation of over 10,000 microelectrodes acquiring a large volume of data from the brain [86, 87]. Multi-state memristor arrays provide a promising solution to process these data in situ, extracting the key information in real time to facilitate closed-loop neuromodulation and wireless data connection to the external hardware.

V. Discussion

Permeating throughout this work are a number of key observations and trends. We begin by noting the gradual move towards analog memristive devices. Central to this has been efforts to increase the resistive state resolution, and yet now we seem to have reached the point where the bottleneck is no longer the device, but our ability to read it precisely. As such, in the future the new "spec battleground" is likely to revolve around obtaining reliability and predictability of behaviour, which disaggregates into high retention, predictable resistive state change given input parameters, good cycling endurance, etc. The ultimate limits of what memristors can achieve in terms of these specs are unclear at the moment. What is certain, however, is that large-scale characterisation studies that are increasingly comprehensive (i.e. attack multiple operating parameters and multiple behavioural tests) will become increasingly important.

Next, we notice that as memristive technologies mature, their interaction with peripherals becomes increasingly important. This manifests itself into two major directions: First, an increasingly pressing need for comprehensive memristor models is likely to drive the need for large-scale characterisation. This includes low-level (electrochemistry-level) modelling, which we expect will be essential for providing reliable models of what is a time-varying component; the very configuration of atoms within a memristor changes during operation, which excluding ageing and other undesirable effects is not the case for any other component. The limits of predictability (and therefore modelability) of memristive devices of various underlying electrochemical mechanisms are still unclear to us and a very big question to answer. Secondly, we already observe a very pressing imperative to engineer devices that do not require electroforming and that can exhibit switching with voltage/current combinations that are sufficiently low to admit provision by typical peripheral circuits in modern CMOS. Specifically, the series resistance of CMOS switches and the $<$2V head-rooms seen starting from CMOS techs going as far back as 180nm realistically demand devices that can switch in sub-V and sub-10μA conditions (and yet still feature a "safe zone" of biases that allow read-out without disturbing the underlying resistive state). Despite the very beneficial, exponential trade-off noted between write voltage and duration [88, 89], it is unclear how much voltage head-rooms can be squeezed before it becomes exceedingly difficult to support both non-invasive read operations and effective write operations.

Finally, we note the large variety of applications in which memristors have found very promising paths of exploitation. A

potentially interesting observation is that in most applications (excluding standard memory storage), memristors seem to have found a very solid niche as parameter-setting elements. This seems to be highly beneficial even for systems where most of the signal processing around them is performed in the digital (or even time) domain. The idea of "using analog to trim digital", as in the cases where analog weights trim the decision surface of an artificial neural network or analog parameters determine the "hit" window for a template-matching function, seems to be very fundamental and powerful. At its limit it may generate a powerful "technological resonance" with standard digital techniques, by enabling futuristic systems where extremely down-scaled digital circuits are held within their operating parameters via aid from analog trimming (imagine a nanoscale resistor near every 2nm transistor, trimmed to ensure an entire array of nano-transistors has exactly the same channel on resistance). Once again, it is unclear exactly how far this concept may go.

VI. Conclusion

Memristor related research has provided a practical solution in the era beyond CMOS. Nevertheless, precisely executing write and read, select and control, and verifying the non-volatility of a multi-state memristor are still a leading-edge research direction in both material science and electrical engineering. In this paper, we introduced and reviewed the state-of-the-art multi-state memristive systems. More importantly, combining the most advanced research results with our previous studies and observations, we analysed the challenges of designing a multi-state CMOS/Memristor system in the aspect of device, memristor modelling, peripheral circuits design, and layout and post-processing. While memristor is an emerging device and as of today there are still areas which require further research and improvement, we have also highlighted a number of promising applications where the multi-state memristor technology could be game changers as the technology advances. We believe the promising results obtained recently in these applications (e.g. the AI accelerator [78] and neural signal processing [83] chips reported very recently) will drive the research community to improve the technology further. Overall, the picture for the field of multi-state memristive technologies seems to consist of two major elements: a) the past and present, where a host of applications and intriguing ideas have been demonstrated and are maturing on the back of what the technology can already deliver or is judged to be very likely to deliver in the not too distant future and b) the future, where the big questions to be uncovered revolve around exactly how much more potential memristors have; this in terms of everything from down-scaling and multi-state precision to retention, richness of internal mechanics and even manufacturing costs, material choice (e.g. what can we achieve using only Silicon and a few relatively abundant dopants?). Thus, in our view, the field promises an exciting future spanning new technologies and science from fundamental electrochemistry and fabrication and all the way up to large-scale memristor-enabled systems.

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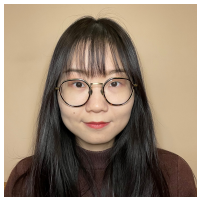

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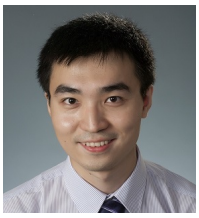

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