INVITED PAPER

Microsensor Integration Into Systems-on-Chip

Micromachining before, during, or after standard CMOS or bipolar processing is being used to produce sensing systems-on-a-chip.

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ABSTRACT | Sensing systems-on-chip (SSoCs), combining micromachined sensing structures and microelectronic building blocks on a single chip, are reviewed. While single-chip pressure and inertial sensing systems have been commercially available for more than a decade, the recent expansion of SSoC into new application areas, ranging from chemical and biochemical sensing to atomic force microscopy, demonstrates the full potential of this microsensor integration approach. Available fabrication processes for integrated sensing systems are summarized, categorizing them into pre-, intra-, and post-CMOS approaches depending on the way the micromachining module is merged with the integrated circuit (IC) technology. Examples of SSoCs are presented to highlight the different integration options, ranging from cointegration of micromachined sensors with purely analog signal chains to microsystems with cointegrated digital signal processors and digital interfaces.

KEYWORDS | CMOS-MEMS; integrated sensor; microsensor; system-on-chip (SoC)

I. INTRODUCTION

Small sensors, translating nonelectrical input signals into electrically processible information, have become ubiquitous in our daily life: microsensors trigger our car's airbag in case of a collision, warn us if the carbon monoxide concentration in our house exceeds certain threshold values, or "quantify" our weather in small weather stations. In order to reduce the fabrication cost, many sensors have been scaled down by the use of fabrication technologies borrowed from the integrated circuit (IC) technology. IC fabrication technologies are used to produce devices with dimensions in the micrometer to millimeter range and the employed batch processing enables the fabrication of thousands of devices in parallel. To be able to scale mechanical structures, such as the membrane of a pressure sensor, dedicated micromachining techniques have been developed, enabling their fabrication using batch fabrication techniques [1]. The related field is called microsystems technology or microelectromechanical systems (MEMS). Micromachining techniques in combination with standard IC processing steps—namely, doping, deposition, photolithography, and etching—form the technological base for many of today's microsensors.

In order to reduce the number of off-chip components required to operate a sensing system, more and more microelectronic building blocks are integrated together with the microsensor on the same chip. Depending on the application, the resulting (sensing) systems-on-chip (SoCs) might feature "only" analog signal processing in addition to the actual transducer or they might incorporate sophisticated digital signal processing enabling on-chip testing, calibration, and off-chip communication via a bus interface. To be able to produce SoCs with integrated sensing functions [in this paper called sensing systems-on-chip (SSoCs)], the technology used to fabricate the microsensor must be merged with standard IC technologies, i.e., CMOS or bipolar process technology. The challenges and prospects of the resulting integrated microsystems, often termed CMOS-MEMS [2], are the topic of this paper.

Certain microsensors can be completely formed within the regular IC process sequence, typically not requiring any additional process steps. Prominent examples include temperature sensors, magnetic field sensors (especially Hall sensors), and CMOS imagers. An additional subset of CMOS-based microsystems only requires either the modification of a CMOS layer or the deposition and patterning of additional films. Examples include various chemical sensors [3], such as amperometric sensors, palladium-gate and ion-selective FET structures, and chemoresistors/capacitors, biosensor arrays for DNA

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analysis [4], [5] and recording/stimulation of neural activity [6], [7], but also a number of physical sensors, such as fluxgate sensors [8]–[10], fingerprint sensors [11], and force sensors [12].

The focus of this overview paper is, however, on integrated microsystems, which require micromachining process steps to be merged with CMOS processing. In the first part of the paper, we will highlight fundamental fabrication approaches for integrated sensing systems. The available processes are categorized by the way the micromachining module is integrated with the IC technology: the additional process steps (or modules) either precede the standard CMOS (or bipolar) process sequence (pre-CMOS), they are performed in between the regular CMOS steps (intra-CMOS) or are added after completion of the CMOS process (post-CMOS). Some fabrication approaches even require several additional process modules, combining, e.g., a pre- and a post-CMOS micromachining module. The first part of the paper provides an overview of these three fundamental CMOS-MEMS integration approaches, highlighting their advantages and disadvantages and providing example process flows. A detailed review of CMOS-MEMS fabrication technologies is beyond the scope of this paper (an extensive treatment of CMOS-MEMS can found in [2]). The second part of the paper discusses examples of CMOS microsystems, showing the various integration levels pursued. Again, we are not aiming for completeness, but rather intend to discuss the advantages of the different integration levels using dedicated examples from both industry and academia.

II. INTEGRATED MICROSYSTEM FABRICATION

Micromachining techniques used to produce (three-dimensional) microstructures, such as cantilevers, bridges, and membranes, are typically categorized into bulk micromachining and surface micromachining (see Fig. 1). In the case of bulk micromachining, significant amounts of the silicon substrate material are removed (etched) to release the microstructure. In the case of surface micromachining, the microstructure is composed of thin film layers, which are deposited on top of the substrate and selectively removed in a defined sequence to define the MEMS structure.

Bulk micromachining techniques [13], i.e., etching techniques to machine the (silicon) substrate, can be classified into isotropic and anisotropic, and into wet and dry etching techniques. *Anisotropic wet etching* of single crystalline silicon is the most common micromachining technique and is characterized by different etch rates along different crystal directions. Using (100) wafers as substrate material, wet anisotropic etching using common solutions, such as potassium hydroxide, KOH, and tetramethyl ammoniumhydroxide (TMAH), results in characteristic truncated pyramid-shaped etch cavities bound by slow-

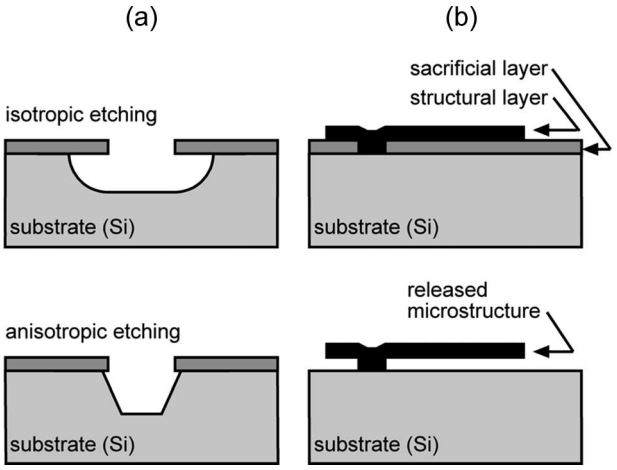

Fig. 1. *Schematic of: (a) bulk and (b) surface micromachining.*

etching (111) planes. The most common *isotropic wet etchant* for silicon is HNA, a mixture of hydrofluoric acid (HF), nitric acid (HNO_3) and acetic acid (CH_3COOH). The etchant exhibits relatively high etch rates for silicon dioxide films, making it difficult to combine with IC processes. *Anisotropic dry etching* of silicon is usually performed by reactive ion etching (RIE) in plasma-assisted etching systems. With the availability of processes and process tools for etching very high aspect ratio microstructures (often termed deep-RIE or DRIE), anisotropic dry etching of silicon has gained importance during recent years. One of the main advantages of dry anisotropic etching is the independence of the anisotropy from the crystal orientation and the resulting increased design freedom. However, DRIE equipment and processes are typically far more expensive than wet etching setups. Finally, *isotropic dry etching* of silicon can be done using xenon difluoride, XeF_2. The vapor-phase etching method exhibits excellent etch selectivity with respect to aluminum, silicon dioxide, silicon nitride and photoresist, making the etch process suitable for combination with IC technologies.

Surface micromachining techniques [14] are most commonly based on sacrificial-layer etching. In this process, a microstructure, such as a cantilever beam or a suspended plate, is released by removing a sacrificial thin film material, which was previously deposited underneath the microstructure. The release of polysilicon microstructures by removing a sacrificial silicon dioxide film is the most popular surface micromachining technique [14]. Sacrificial aluminum etching (SALE) has been developed to release dielectric microstructures with embedded metal layers [15]. Metallic microstructures deposited by low-temperature physical vapor deposition (PVD) processes can use polymer films as sacrificial layers, which are easily removed using, e.g., an oxygen plasma [16], [17].

Depending on the chosen integration path, a number of fabrication constraints are imposed on the micromachining steps in order not to deteriorate the performance of the CMOS (or bipolar) electronics. An important example is the thermal budget allowed for the micromachining process steps. The widely used polysilicon microstructures are deposited at temperatures between 575 °C and 625 °C in a low-pressure chemical vapor deposition (LPCVD) furnace and typically require thermal annealing at temperatures $\geq$ 900 °C to reduce residual stress [18], [19]. However, after deposition of the aluminum metallization of a CMOS process, the maximum process temperature is limited to $\leq$ 450 °C in order not to degrade the aluminum–silicon contacts. Therefore, polysilicon cannot be deposited after the completion of a CMOS process with standard aluminum metallization. In order to enable the deposition of polysilicon microstructures after the completion of the CMOS process sequence, the use of an alternative high-temperature stable metallization, such as tungsten, was proposed earlier [20]. Keeping in mind that IC manufacturers have invested enormous resources into the development of reliable, multilevel aluminum interconnect technologies, and further considering the inferior resistivity of tungsten versus aluminum, the adoption of such a process by industry is unlikely. Alternatively, the standard polysilicon gate material of the CMOS process is used for the microstructures as well or an additional structural polysilicon layer is deposited and structured before the standard CMOS metallization is applied. In this approach, the regular CMOS process sequence is interrupted before the metal deposition, a dedicated micromachining module is inserted, and then the CMOS process sequence resumes with the back-end aluminum interconnect technology. This intra-CMOS approach minimizes performance degradations for both electronic and mechanical components, but requires interruption of the CMOS process sequence and, more critical, the need to return CMOS wafers into a CMOS line after performing nonstandard process steps. As a result, especially companies with in-house CMOS or BiCMOS fabrication facilities (e.g., Analog Devices [21]–[23] and Infineon Technologies [24], [25]) have adopted this fabrication approach for high-volume CMOS-integrated microsensors based on polysilicon microstructures. Finally, one can try to find low-temperature alternatives for the mechanical polysilicon, enabling deposition of structural films after completion of the CMOS process. In this regard, e.g., polycrystalline silicon–germanium films deposited below 450 °C have attracted considerable interest in recent years [26]–[28].

A. Pre-CMOS Micromachining

Pre-CMOS micromachining or "MEMS-first" fabrication approaches avoid thermal budget constraints during the MEMS fabrication. This way, e.g., thick ($\geq$ 10 μm) polysilicon microstructures requiring stress relief anneals at temperatures up to 1100 °C can be cointegrated with CMOS circuitry. Typically, the MEMS structures are buried and sealed during the initial process module. After the wafer surface is planarized, the preprocessed wafers with embedded MEMS structures are used as starting material for the subsequent CMOS process. Of course, the preprocessed starting material requires qualification by the CMOS foundry in order not to compromise their process yield. Challenges also include the surface planarization required for the subsequent CMOS process and the interconnections between MEMS and circuitry areas. Examples of polysilicon microstructures implemented in a pre-CMOS approach include the M^3EMS (modular, monolithic microelectromechanical systems) technology [29] and, more recently, the ModMEMS technology [30].

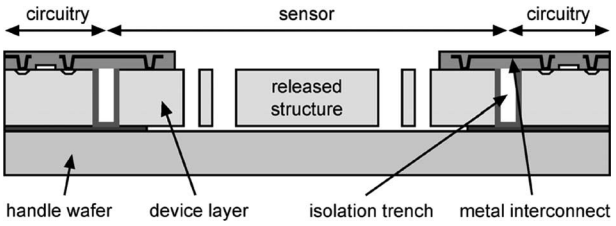

Fig. 2. *Cross section of SOI-based integrated MEMS technology (SOIMEMS) by Analog Devices with 10-μm device layer for fabrication of single-crystalline silicon inertial sensors (adapted from [22]).*

Single-crystalline silicon microstructures can be implemented in a pre-CMOS fabrication approach using either silicon-on-insulator (SOI) wafers as substrate material [22], [31]–[33] or by incorporating sealed cavities using wafer bonding [34], [35]. Originally demonstrated at the University of California (UC) Berkeley [31], the SOIMEMS technology has been further developed and commercialized by Analog Devices as a next-generation process for the monolithic integration of inertial sensors. Compared to Analog Devices' high-volume iMEMS technology [21], SOIMEMS offers thicker structural layers (10 μm instead of 4 μm), yielding more robust sensor structures, and a more advanced BiCMOS technology (0.6 μm instead of 3.0 μm minimal feature sizes), enabling more on-chip functionality. A cross section of the SOIMEMS technology is depicted in Fig. 2 [22]. The fabrication process comprises both a pre-CMOS (trench isolation) and a post-CMOS (microstructure definition and release) fabrication module, but has the advantage that all of the circuit processing is done in single, noninterrupted process sequence [22]. The fabrication process starts with etching trenches in the SOI wafers (having a 10-μm device layer) to establish isolated areas on the wafer. The DRIE trench etching stops at the buried oxide layer of the SOI substrates. After trench-refill and surface planarization, the regular 0.6-μm

BiCMOS process sequence is executed. Interconnects between circuitry and microstructures are established with the standard IC metallization. After completion of the BiCMOS process sequence, the structural regions are cleared from all dielectrics and the microstructures are defined using a DRIE trench-etching step. Finally, the microstructures are released by etching the buried oxide layer underneath them using a hydrofluoric acid (HF) based solution.

B. Intra-CMOS Micromachining

Intermediate micromachining is most commonly used to integrate polysilicon microstructures in CMOS/BiCMOS process technologies [14]. Inserting the micromachining process steps before the backend interconnect metallization ensures process compatibility with the polysilicon deposition and anneal. The polysilicon annealing temperature is typically limited to about 900 °C in order not to affect the doping profiles of the CMOS process. As a result, the polysilicon layer thickness is limited to a few micrometers.

Commercially available examples of microsensors based on polysilicon microstructures, fabricated using CMOS/BiCMOS processes with intermediate micromachining, include Analog Devices' ADXL series accelerometers and ADXRS series gyroscopes [36], Infineon Technologies' KP100 series pressure sensors [37] and Freescale's MPXY8000 series pressure sensors [38]. Not surprisingly, all three companies have in-house IC processing capabilities, facilitating the chosen interleaved process sequences and allowing to fine-tune the overall process sequence to minimize degradation in both electronic and mechanical components.

In the following, we will briefly highlight the process technology developed by Infineon Technologies (formerly Siemens) to fabricate integrated pressure sensors based on polysilicon microstructures. In contrast to Analog Devices, which deposits a dedicated low-stress polysilicon layer for its mechanical structures [21], [22], Infineon Technologies uses the standard capacitor polysilicon layer (second polysilicon layer) of a 0.8-μm BiCMOS process as mechanical layer for their pressure sensors [24], [25]. A schematic cross section of the surface-micromachined pressure sensors is shown in Fig. 3. The standard process sequence of the 16-mask BiCMOS process is stopped before the back-end interconnect metallization to insert a single-mask micromachining module. The basic pressure sensor structure is formed within the course of the BiCMOS process sequence. The lower electrode is made from the n-well, the 600-nm field oxide serves as sacrificial layer and the 400-nm capacitor polysilicon as structural layer and top electrode [24], [25]. Within the micromachining module, membranes are perforated in a dry etching step, the oxide sacrificial layer is etched using vapor HF through the holes in the membrane and, finally, the resulting cavities are sealed [24]. After completion of the micromachining module, the regular BiCMOS back-end process is employed to form the aluminum interconnects and passivate the microsystem. The final pad etch is used to open the contact pads and form the oxide boss structures on the pressure sensors (see Fig. 3).

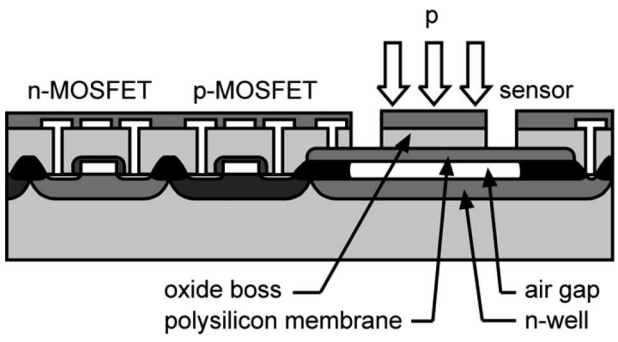

Fig. 3. *Schematic cross section of Infineon Technologies' integrated MEMS technology for the fabrication of pressure sensors (adapted from [24]).*

Sub-0.25-μm CMOS processes typically offer a copper-based multilevel interconnect technology with high planarity. In order to use these metallic interconnects for mechanical devices (e.g., switches and resonators) [39], [40], researchers at IBM's T. J. Watson Research Center have adapted the standard copper (dual)-damascene process sequence used by IBM for interconnect formation. The process additions include: 1) the encapsulation of the copper to prevent its oxidation; 2) the introduction of suitable contact materials for the switches; and 3) the deposition of an organic sacrificial layer for copper microstructure release. All required dielectric films are produced using PECVD at temperatures of 400 °C or less, and all metal films are deposited by sputtering or a combination of sputtering and electroplating [39].

Bulk micromachining using wet anisotropic silicon etchants in combination with p^{++} etch-stop techniques has been extensively used by K. D. Wise and coworkers at the University of Michigan for the fabrication of CMOS-based mass-flow sensors [41], pressure sensors [41], [42], microelectrode recording arrays [43]–[45], thermal converters [46], and infrared sensors [47]. All these microsystems are fabricated using a modified p-well CMOS process. Highly p-doped regions are diffused into the silicon substrate wafer after the CMOS p-well implantation. The p-well implant dose had to be modified from the baseline CMOS process to account for the additional p-well oxidation and boron segregation into the masking oxide in the merged process [41], [43]. The p-well drive-in is accomplished simultaneously with the p^{++} diffusion. If required, an additional shallow p^{++} diffusion is implemented. The p^{++} regions define: 1) the lateral dimensions of dielectric membranes by providing a nonetched p^{++} rim around them and 2) the thickness of silicon

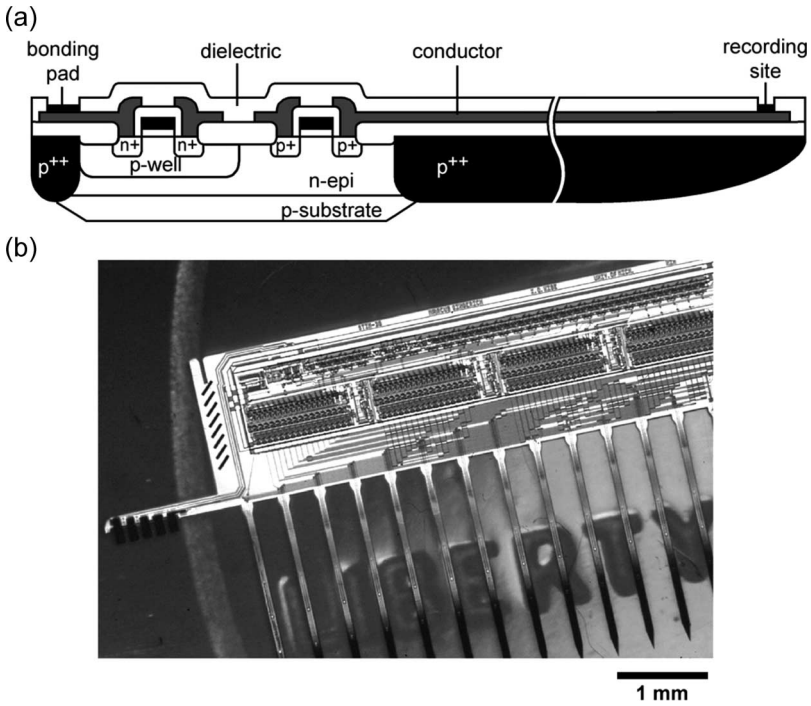

Fig. 4. *(a) Schematic cross section (adapted from [43]) and (b) photograph of needle probe developed at the University of Michigan (image courtesy of Prof. K. D. Wise, University of Michigan, Ann Arbor; see also [45]); diffused p^{++} regions are used as etch-stop layers during the microstructure release by anisotropic wet etching.*

microstructures, e.g., membranes for pressure sensors or shafts for needle probes, by the depth of the diffusion (see Fig. 4). The microstructures are released after completion of the CMOS process sequence with the p^{++} regions providing an intrinsic etch-stop. As an example, Fig. 4 shows a schematic cross section and photograph of an integrated needle probe fabricated with the intra-CMOS approach [43], [45].

C. Post-CMOS Micromachining

A key advantage of post-CMOS micromachining approaches is that the fabrication can be completely outsourced. After completion of the regular CMOS process sequence, which can, in principle, be performed at any CMOS foundry, the post-CMOS micromachining steps can be done at a dedicated MEMS foundry. The price to pay for this fabrication flexibility is the stringent thermal budget for all process steps following standard CMOS technologies with aluminum metallization. A maximum process temperature of approximately 450 °C excludes high-temperature deposition and annealing steps, such as polysilicon deposition in an LPCVD furnace. PECVD processes, sputtering, electroplating, and most wet and dry bulk and surface micromachining processes are, however, well suited for the post-CMOS approach. During the micromachining etching/release step, the CMOS electronics might require a special protection.

Two general post-CMOS micromachining approaches can be distinguished: the microstructures are formed either by machining the CMOS layers themselves or by building the complete microstructures on top of the CMOS substrate. In the first approach, most of the microstructure is already created within the regular process sequence. In this case, the post-CMOS process module typically requires very few process steps, such as an etching step to release the microstructure. Building the complete MEMS on top of the CMOS substrate might require more process steps but can save valuable real estate, because the MEMS part can be build directly on top of the CMOS circuitry. In the following, we will provide examples for both fabrication approaches.

1) Post-CMOS Micromachining of Add-On Layers: Most processes in this category use surface micromachining techniques and in particular sacrificial layer etching to build and release the microstructures on top of the CMOS substrate. Based on the required process temperatures, the post-CMOS add-on micromachining modules can be classified in two basic categories: 1) low-temperature modules with process temperatures up to approximately 100 °C–150 °C, which are typically based on PVD or electroplating of metal layers and use polymers or metals as sacrificial layers and 2) medium-temperature modules requiring process temperatures over 300 °C, which are

often based on chemical vapor deposition (CVD) processes for the structural and the sacrificial layers. Crucial for all add-on surface micromachining modules is a good planarity of the underlying CMOS substrate and both a good electrical and mechanical contact between the microstructures and the CMOS circuit. The on-chip circuitry can either surround the MEMS or be located underneath the microstructures, saving valuable CMOS real estate.

Because of their excellent mechanical properties, the integration of polysilicon microstructures after the completion of a CMOS process has been studied carefully in the early 1990s [14], [20]. The LPCVD deposition and stress-relief anneal of thin polysilicon films requires process temperatures of $\approx 600\ ^\circ$C and $\geq 900\ ^\circ$C, respectively, which are not compatible with the standard aluminum (or copper) metallization used in most of today's CMOS processes. To accommodate the required high-temperature postprocessing module, significant modifications had to be made to a baseline CMOS process at the metallization and passivation level [20], introducing, e.g., a tungsten metallization for circuit interconnection.

To avoid doping redistribution and the need for high-temperature stable interconnect metallization, the postprocessing temperature must be reduced to below $\approx 500\ ^\circ$C [48]. To achieve this, polycrystalline silicon–germanium films have been investigated recently [26]–[28] as an alternative to polysilicon films. Depending on the germanium concentration and the deposition pressure, polycrystalline Si–Ge films can be deposited at temperatures of 450 °C or even lower, making the process compatible with a standard CMOS aluminum metallization. In [26], two post-CMOS micromachining approaches for the cointegration of poly-SiGe microstructures with CMOS circuitry are investigated: the first approach uses n-type poly-Ge deposited at 400 °C as structural layer and SiO_2 as sacrificial layer, the second approach p-type poly-$Si_{0.35}Ge_{0.65}$ as structural and poly-Ge as sacrificial layer (see schematic in Fig. 5). While the first approach requires a special CMOS passivation to protect the circuitry during the microstructure release, the second approach uses hydrogen peroxide for sacrificial layer etching and no special layers are needed to protect CMOS metallization and dielectric layers.

The use of PVD techniques for film deposition can further reduce the processing temperatures of post-CMOS micromachining modules. A commercial example of a metal-based MEMS fabricated on top of a CMOS substrate using low-temperature processes only is the digital micromirror device (DMD) developed by Texas Instruments [16], [49]. The DMD, an array of electrostatically actuated torsional micromirrors (used as light switches), creates the image in digital light processing-based (DLP) projection displays. The mechanical structure of a DMD pixel consists of alternating layers of patterned aluminum and air gaps and is built on top of a CMOS static random-access memory (SRAM) cell using surface-micromachining techniques. The formation of the 16 μm by 16 μm micromirror superstructure requires six additional photolithographic steps to define four aluminum layers and two sacrificial photoresist layers. The aluminum layers are sputter-deposited and the mirror superstructures are released by etching the polymer sacrificial layer in a plasma etcher. Finally, an antistiction coating is applied to prevent stiction of the micromirrors to the landing pads during operation. The fabrication and packaging process are described in detail in [16] and [49].

Thicker metal structures can be achieved by electroplating techniques. Examples of electroplated microstructures on top of CMOS substrates include a gold acceleration threshold switch developed by Infineon Technologies and the University of Bremen [50] and a nickel ring gyroscope developed by Delphi-Delco Electronics, General Motors, and the University of Michigan, Ann Arbor [51], [52]. Both additive electroplating technologies are room temperature processes and do not affect the performance of the underlying CMOS circuits. As with many surface-micromachined structures, control of thin-film stress and stress gradients is a major challenge.

2) Post-CMOS Micromachining of CMOS Layers: In this approach, microstructures are released by machining the CMOS substrate wafer itself after the completion of the

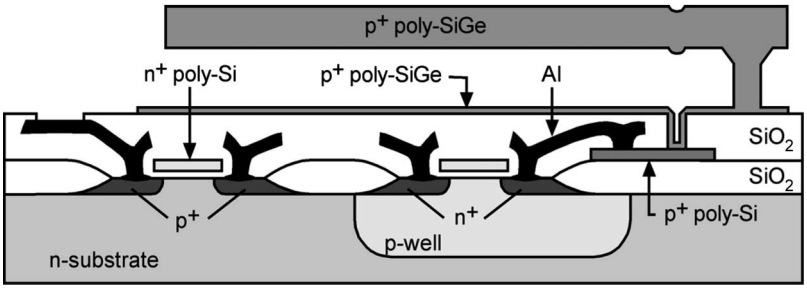

Fig. 5. *Schematic cross section of polycrystalline silicon-germanium (poly-SiGe) microstructure fabricated by post-CMOS surface micromachining techniques on top of a completed CMOS substrate wafer (adapted from [26]).*

regular CMOS process sequence. By far the majority of demonstrated devices rely on bulk micromachining processes, such as wet and dry anisotropic and isotropic silicon etching, but surface-micromachining approaches have been proposed as well.

Piezoresistive pressure sensors based on bulk-micromachined silicon membranes have been the earliest commercially successful application of silicon micromachining (see [1] for an overview of early MEMS efforts). It is thus not surprising that early attempts to cointegrate transducers and electronics have also targeted bulk-micromachined pressure sensors. Fully integrated and temperature-compensated piezoresistive pressure sensors using bipolar technology have been demonstrated in 1979 [53], [54]. Shortly thereafter, the first integrated capacitive pressure sensor with bipolar circuitry has been demonstrated [55]. The first CMOS-integrated piezoresistive silicon pressure sensor has been developed by NEC in the mid-1980s [56]: the sensor consisted of a thin square silicon diaphragm with four piezoresistors in a Wheatstone bridge configuration located along the clamped edges. The membrane was released by anisotropic etching from the back of the wafer in combination with an electrochemical etch-stop technique to automatically stop the etching at the pn-junction between p-substrate and n-epitaxial layer.

Today, CMOS-integrated piezoresistive pressure sensors are commercially available from several companies, including Bosch [57], Freescale [38], and Silicon Microstructures [58]. While the basic transducer structure of these microsystems is still a bulk-micromachined silicon membrane with implanted piezoresistors, far more circuitry components are implemented in these modern systems. As an example, Motorola (now Freescale) proposed a design featuring an on-chip digital signal processor (DSP) and nonvolatile memory for calibration, temperature compensation, and the ability to implement customer-specific features [59]. The employed CMOS process is only slightly modified to provide the optimal doping profile for the piezoresistors and to deposit the etch mask for the membrane release on the back of the wafer. The membrane is released using a timed wet etching step, yielding membranes with ± 2-μm thickness tolerance across the wafer. Finally, the sensor wafer is anodically bonded to a glass wafer in vacuum.

Bulk micromachining from the back of the wafer using silicon anisotropic etching has become one of the standard post-CMOS micromachining modules, releasing not only membranes but also cantilevers and suspended microstructures [60], [61]. Besides the pressure sensors mentioned earlier, e.g., accelerometers, flow sensors, ultrasound proximity sensors, thermal converters, infrared radiation sensors, and chemical sensors have been fabricated using this approach [60]. The etching step requires the deposition and patterning of a hardmask on the back of the wafers. Prior to the deposition of the hardmask, any processing residues and damages caused by the CMOS process have to be removed from the backside of the wafer. In particular, damages in the wafer surface can lead to an intolerable large mask underetching during the MEMS release. The hard mask typically consists of a PECVD silicon nitride layer, if necessary with a pad oxide underneath. While potassium hydroxide (KOH) solutions have become the most common wet etchant used in bulk micromachining from the back of the wafer, various etch-stop techniques are employed to control the etch result. Besides a timed etch, silicon dioxide layers, highly p^{++}-doped silicon regions and pn-junctions are commonly used. Membranes consisting of the dielectric layers of the CMOS process are, e.g., released using the field oxide on top of the silicon substrate as an intrinsic etch-stop layer [61]. The use of SOI-based CMOS processes offers the possibility to employ the buried oxide layer of the SOI substrates as etch-stop layer in order to release single-crystalline silicon structures. Electrochemical etch-stop techniques (ECE) can be used to accurately stop the wet etching process at the pn-junction between the CMOS n-well and the p-type substrate. For this process, at least the electrochemical potential provided by a potentiostat has to be connected to each individual "mechanical" n-well on the wafer. A suitable scheme to modify commercial CMOS device technologies for the application of ECE in a four-electrode configuration has been presented in [62]: to supply the ECE potentials to the sensor structures, a contact field and a wafer-wide contact network are generated (see Fig. 6). The contact network routes the n-well and p-substrate potential to the respective contacts on the sensor structures. The chosen process sequence comprises additional standard photolithography steps at the metallization and passivation mask levels performed exclusively on wafer steppers. Thus, there are no restrictions on the minimum feature size of the process or the wafer diameter. During the wet etching, the CMOS wafer is typically mounted in a wafer holder to protect the wafer front with the CMOS circuits from the wet etchant. In case of wet anisotropic etching with an electrochemical etch-stop technique, the wafer holder supplies the etching potentials to the wafer (see, e.g., [63]).

Alternative to the wet etching, bulk micromachining from the back of the wafer can be performed with DRIE etching systems, resulting in almost vertical sidewalls independent of the silicon crystal orientation [13]. DRIE techniques have gained significant momentum over the past couple of years, but the required equipment is expensive, only single wafers can be processed at a time and no ECE or p^{++} etch-stop can be used. On the other hand, DRIE can achieve structures, e.g., narrow support bars, which cannot be achieved by KOH etching of $\langle 100 \rangle$ wafers [64].

To release microstructures from the front side of the wafer in a post-CMOS approach, silicon areas on the wafer surface are exposed to the ambient at the end of the regular CMOS process sequence by superimposing active area,

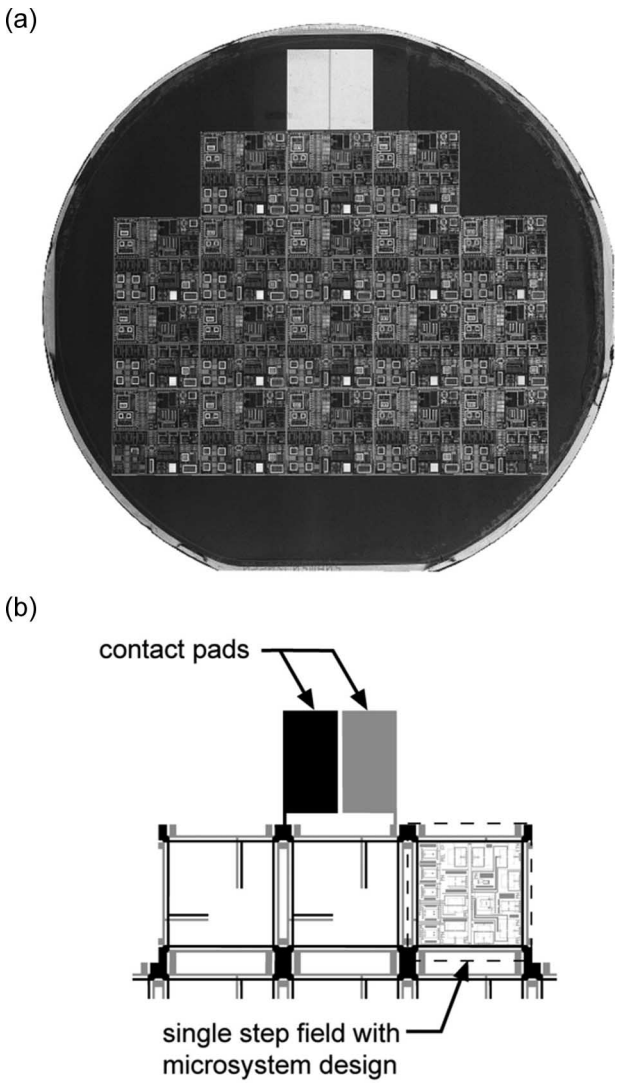

Fig. 6. *(a) 100-mm CMOS wafer with large contact pads to enable anisotropic wet etching from the back of the wafer with an electrochemical etch-stop technique. (b) Schematic of etch network routing the etching potentials for the structural n-well and substrate contacts from the contact pads to the individual microstructures [62].*

contact, via, and pad opening in the design [65]. Anisotropic wet etchants, such as EDP and TMAH, or isotropic dry etching techniques based on, e.g., XeF_2, etch the silicon substrate in these areas, allowing to release dielectric microstructures, such as cantilever beams and bridges with embedded polysilicon and metal layers [13], [61], [65]. Care must be taken to protect the aluminum contact pads and the passivation of the CMOS process during the etching step. Certain TMAH and EDP formulations have relatively small aluminum etch rates, enabling a maskless wet release of the microstructures if the etching step is not too long.

An alternative bulk micromachining technology from the front side of CMOS wafers using dry etching steps has been developed at Carnegie Mellon University [66]. The post-CMOS micromachining module uses the top metal interconnect layer as etch mask for the microstructure definition. This way the minimal feature sizes, such as minimum beam widths and gaps, are defined by the CMOS design rules and can be scaled with the CMOS technology. The actual laminated microstructures consisting of the CMOS dielectrics with polysilicon and metal layers sandwiched in between are released using two dry etching steps [see schematic in Fig. 7(a)]: in the first anisotropic etching step using a CHF_3/O_2 etch chemistry, the oxide areas not protected by the metal mask are etched to the silicon substrate; in the second isotropic etching step using a SF_6/O_2 chemistry, the oxide beams are underetched, releasing the microstructures. The process technology has been used to fabricate, e.g., integrated accelerometers [67], gyroscopes [68], as well as acoustic devices [69], [70]. To construct a speaker or microphone, a mesh-type membrane is released with the described post-CMOS dry etching sequence. The released mesh is conformally coated with a polymer in a CVD process, yielding a continuous, airtight membrane [70], [71]. Depending on the CMOS process, the released dielectric layer sandwich with embedded polysilicon and metallization lines can be subject to large residual stress and stress gradients, causing large microstructures to curl. To be able to release single-crystalline silicon microstructures, the maskless post-CMOS micromachining process developed at Carnegie Mellon has been combined with DRIE and an anisotropic etch step from the back of the wafer [72] [see Fig. 7(b)].

While bulk-micromachining processes dominate the post-CMOS micromachining modules, surface-micromachining techniques can be used to selectively remove thin film layers of the CMOS process. An example is the SALE technique developed at ETH Zurich [73]. In this post-CMOS micromachining module, the first metal layer of the CMOS process is selectively removed to release microstructures composed of the intermetal dielectric, the upper metallization layer, and the passivation. A complete thermal pressure-sensing system based on surface-micromachined sensor cells is presented in [74].

III. EXAMPLES OF SSoCs

"SoC" refers to technologies that package all the electronic circuits and parts for a complete "system" on a single chip. Such a complete system typically includes a central processor, memory and (most of) the peripheral electronics. Due to integration complexity, customer requirements and economical considerations, very few of today's integrated sensing systems actually comprise an on-chip microcontroller. Often, the expected volume of microsensor systems does not justify their cointegration with deep submicrometer CMOS technologies required for cost-effective (high-volume) fabrication of large digital

circuits. Microsensors are historically far more diversified than microelectronic circuits, with typically smaller volumes per customer/application, and various customer-specific requirements in terms of, e.g., output signal format, calibration, communication, or even packaging.

In the following, we use a somewhat broader definition of SoC, referring to the integration of all the *necessary* electronic circuits of diverse functions onto a single chip. Along this line, an SoC does not require an integrated microcontroller or DSP. An integrated microsystem consisting of a (micromachined) sensing element and analog circuitry for sensor biasing, signal readout and conditioning would already qualify as an SoC. Such CMOS-integrated microsensors can be classified by the way information is processed on-chip and by their interface to off-chip data processing units.

A. SSoC With Analog Signal Chain

Microsystems belonging to this category limit the on-chip circuitry to the necessary analog biasing and signal conditioning circuitry and use external components for further data processing. Because no space-consuming digital circuitry is implemented on chip, microsystems relying on integrated analog circuitry blocks are typically based on "older" CMOS technologies with minimal dimensions ranging from 0.8 to 3 μm with 4- or 6-in wafers as starting material. Besides the relatively low cost for a mask-set (at least compared to the mask-set cost of sub-0.25-μm technologies), these technologies are typically more forgiving if additional thermal process steps have to be integrated in the process flow. As signal-to-noise ratio (SNR) and resolution of a microsensor are determined mainly by the first stages in the signal processing chain, there is usually no loss in system performance compared to solutions with higher integration. A disadvantage of a purely analog implementation is that no digital circuitry for calibration, linearization or temperature compensation is available. This deficiency can, however, be compensated for by proper analog design expertise and the use of fabrication processes with advanced analog features, such as laser or link (e.g., polysilicon fuses) trimming capability on the wafer. Zener zapping is another widely used trimming process, requiring some form of bipolar transistors in the process, but no special processing

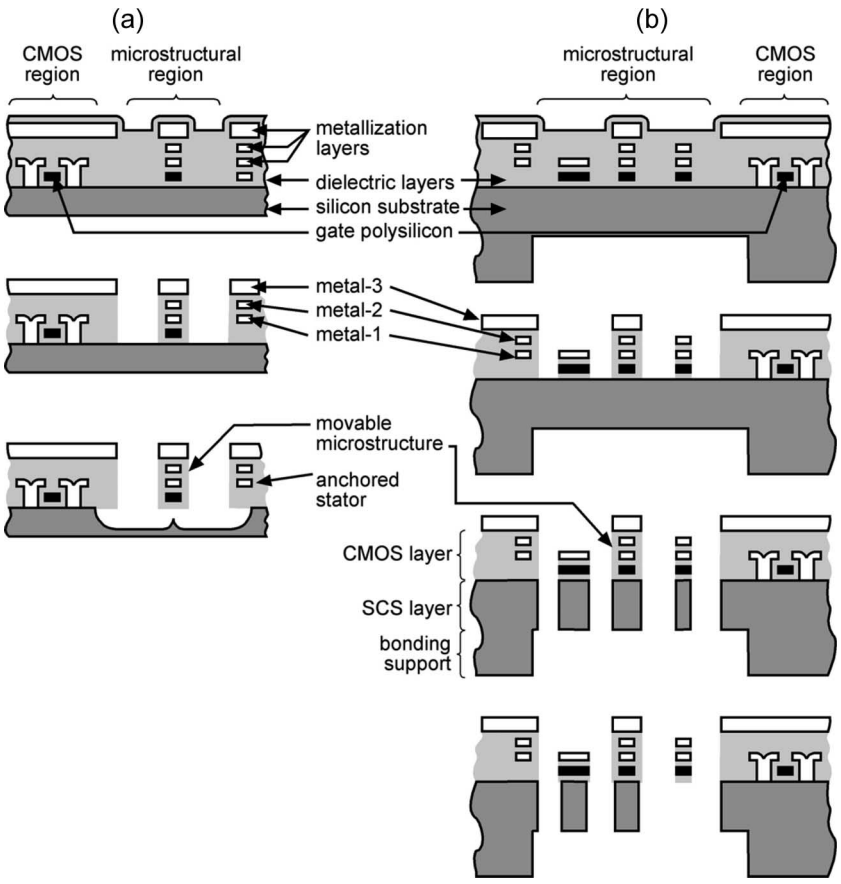

Fig. 7. *Cross section of post-CMOS process sequences developed at Carnegie Mellon University to release (a) dielectric (adapted from [66]) and (b) crystalline silicon microstructures (adapted from [72]); both processes are based on a series of anisotropic and isotropic dry etching steps.*

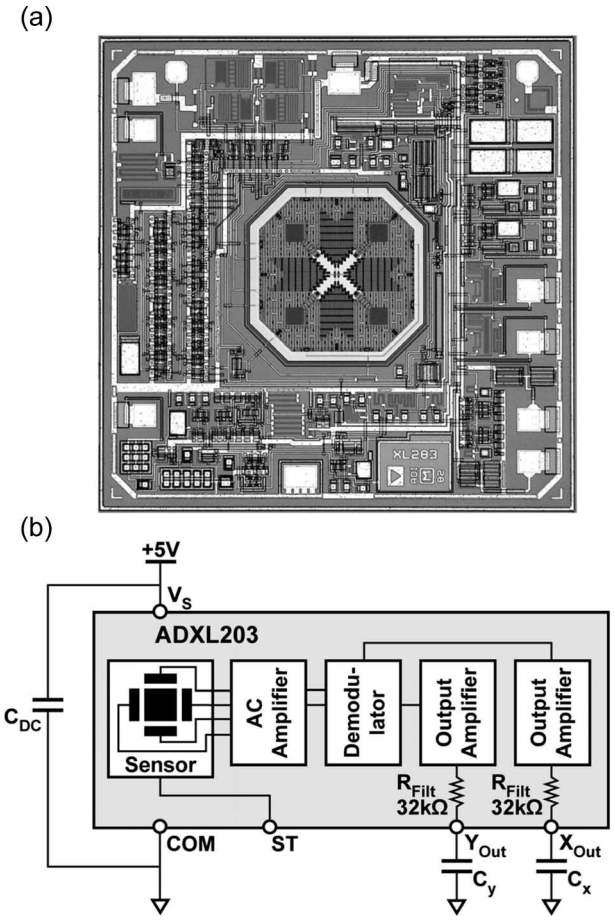

Fig. 8. *(a) Photograph (courtesy of Dr. M.W. Judy, Analog Devices, Cambridge, MA; Copyright Analog Devices, Inc.; All rights reserved) [22], [75] and (b) system architecture (adapted from [76]) of Analog Devices dual axis accelerometer ADXL-203.*

otherwise. Analog trimming capabilities are widely used to adjust sensor offset and sensitivity, thus standardizing the analog output format (e.g., a ratiometric output with respect to the supply voltages). This way, the SSoC can be used by different customers, which have the design freedom to implement the subsequent signal processing blocks as needed for their particular application.

This integration approach is successfully employed by Analog Devices since 1993 for their iMEMS accelerometers and gyroscopes [22], [75]. As an example, Fig. 8 shows a photograph of the ADXL203 dual axis accelerometer with a full-scale range of ± 1.7 g [75] and a schematic of its system architecture [76]. Current members of the ADXL series of acceleration sensors are based on a 3-μm BiCMOS process with a micromachining module implemented before the CMOS metallization in order to produce the 4-μm-thick polysilicon microstructures [22], [75]. The lateral deflection of the suspended microstructure is measured using a differential capacitor with two independent sets of fixed electrodes and movable electrodes connected to the moving mass. The fixed electrodes are driven by 180° out-of-phase square waves [76]. A deflection of the microstructure upon acceleration unbalances the differential capacitor, resulting in an output square wave with an amplitude proportional to the applied acceleration. Phase sensitive demodulation techniques are then used to rectify the signal and determine the direction of the acceleration. The outputs of the demodulators are amplified and brought off-chip through a filter resistor. By connecting proper filter capacitors to the output pins [X_{OUT}, Y_{OUT} in Fig. 8(b)], the user can adjust the signal bandwidth. The same dual axis acceleration sensor is available with pulse-width-modulated outputs to enable connection to a microcontroller without the need for an analog-to-digital converter [77]. The two axis accelerometer has a build-in self-test feature: applying V_S to the test pin ST generates an electrostatic force which deflects the movable mass, resulting in a defined change of the output signal if the device is working properly. Key parameters (offset, gain) of the sensing system are laser trimmed on a wafer level using trimmable thin film resistors. Without any additional (digital) temperature compensation circuitry, the complete microsystem features a temperature hysteresis of typically less than 10 mg over the temperature range from -40 °C to $+125$ °C and a sensitivity change due to temperature of less than 0.3% over the same temperature range [76].

Using the same underlying process, Analog Devices commercialized the first CMOS-integrated gyroscope (ADXRS150/300) in late 2002 [22], [75], [78]. The used analog detection electronics is able to detect capacitance changes as low as 12 zF ($12 \cdot 10^{-21}$ F) [78].

Additional examples of integrated sensing system featuring analog front-end circuitry and an analog output signal include Freescale Semiconductor's integrated pressure sensor lines MPX4000 through MPX6000 [79] and thermal imagers developed at ETH Zurich [80].

In contrast to using analog trimming techniques, digital circuit blocks can be introduced for calibration, while still keeping an analog signal chain. Examples are the integrated pressure sensors MLX90269 and MLX90257 by Melexis [81]. Here, the analog signal chain, consisting of chopper instrumentation amplifier stage, differential to single-ended converter, demodulator, gain adjustment stage, and output stage, interacts with a digital core to calibrate offset and sensitivity and cancel temperature related parameter drifts. To this end, the output signal of an on-chip temperature sensor is connected to the digital circuitry via an analog-to-digital converter. The pressure sensor system requires a 3-point temperature and 2-point pressure calibration with the calibration parameters programmed into Zener zapping cells, resulting in less than $\pm 1\%$ total error over the complete temperature range from -40 °C to $+125$ °C.

Freescale Semiconductor also uses a mostly analog signal chain with digital control of trimming parameters

for their MPX8000 line of tire pressure sensors [79]. The CMOS-based microsystem features surface-micromachined, capacitive structures as pressure-sensitive elements [82]. The signal conditioning chain of the pressure signal begins with a capacitance to voltage conversion followed by an amplification stage with adjustable offset and gain trimming [79]. In contrast to the Melexis approach, the sensor output is, however, digital. The pressure is actually monitored by a voltage comparator, comparing the measured (analog) value with an 8-bit threshold adjusted via a serial input. This way the digital output of the comparator can either be used to monitor a pressure threshold or to actually get an 8-bit pressure reading by properly adjusting the threshold for each bit. Trim data is stored in on-chip electrically erasable programmable ROM (EEPROM) and an integrated temperature sensor enables temperature compensation of the output signal. The actual operation mode of the sensing system (pressure-sensing mode, temperature measurement mode, trim mode) is controlled from the outside by properly setting state pins connected to the digital control circuit.

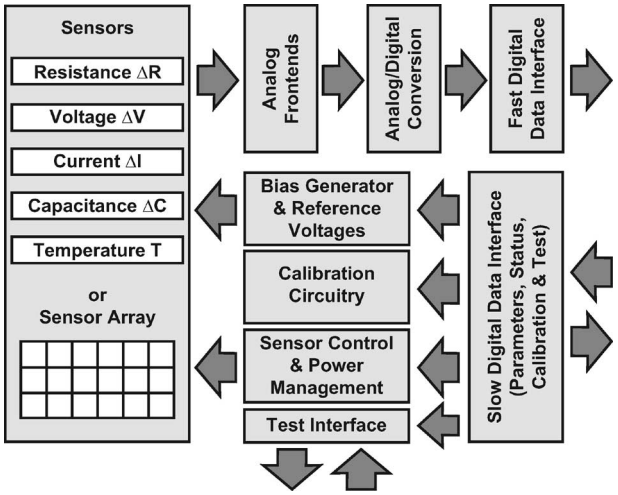

Fig. 9. *Template for the system architecture of an SSoC with digital interface to signal processing unit (adapted from [83]).*

B. SSoC With Mixed-Signal Data Processing

Sensing microsystems belonging to this group contain at least an analog-to-digital converter (ADC) to convert the sensor signals from the analog to the digital domain. In combination with a digital interface, the data can then be directly transferred to an external microprocessor or field-programmable gate array (FPGA) for further processing. Often, additional digital circuitry, together with some form of memory (registers, RAM, or nonvolatile flash memory) to store calibration/compensation parameters, is implemented on-chip for calibration and compensation purposes. The strength of the mixed-signal approach is its flexibility. Digital circuitry enables highly customized signal calibration and compensation procedures, including not only offset compensation and sensitivity adjustment but also correction for linear and higher order temperature errors and signal linearization. The price to pay for this design flexibility is typically an increased chip area to accommodate the digital circuit blocks, resulting in higher manufacturing cost. Digital circuitry efficiently scales by using more advanced CMOS processes, which are, however, usually less forgiving if additional micromachining modules have to be added.

After on-chip signal processing, the digital data can either be transferred off-chip using a digital interface or transformed back to the analog domain using a digital-to-analog converter (DAC) and routed off-chip as a standardized analog signal. A digital interface, such as a serial peripheral interface (SPI) or I^2C interface, avoids transmission of sensitive analog signals through potentially noisy external data channels and enables to directly transfer the data of several sensor chips to an external microcontroller. A standardized analog output signal, on the other hand, might be more suitable for integration into existing customer-specific sensing modules. It is not uncommon that companies either combine a serial interface and an analog (ratiometric) output or offer different versions of a particular microsystem with either analog or digital output. A template for a (generic) system architecture for a sensing microsystem with digital interface to a signal-processing unit is depicted in Fig. 9 [83]. Besides the actual signal conditioning including analog front-end circuitry, A/D conversion and a (fast) digital interface for data transfer, the on-chip circuitry can provide the necessary sensor biasing, perform calibration, compensation, and power management functions, and execute diagnostic procedures to analyze sensor status. Such sensor self-tests are especially important in safety-related applications, such as acceleration sensors for air bag deployment. All of the mentioned additional functionality can typically be controlled from the outside via a proper interface.

The SM5822/SM5872 line of cointegrated pressure sensors by Silicon Microstructures Inc. is an example of an SSoC with mixed-signal circuitry providing both an analog and a digital output signal [84], [85]. The piezoresistive pressure sensors utilize an on-chip DSP and on-chip EEPROM for storage of calibration and compensation data. The sensor is based on a 0.65-μm CMOS process with a post-CMOS micromachining module to release the pressure-sensitive membrane. Fig. 10 shows a die photograph of the pressure-sensing SoC [84] and a schematic of the system architecture [85]. The output signal of the piezoresistive Wheatstone bridge is first amplified and offset-corrected. The signal is then passed to an 11-bit analog-to-digital converter with 4x oversampling, resulting in a 13-bit word. Calibration and correction of the sensor signal is then performed in the on-chip DSP. Up to

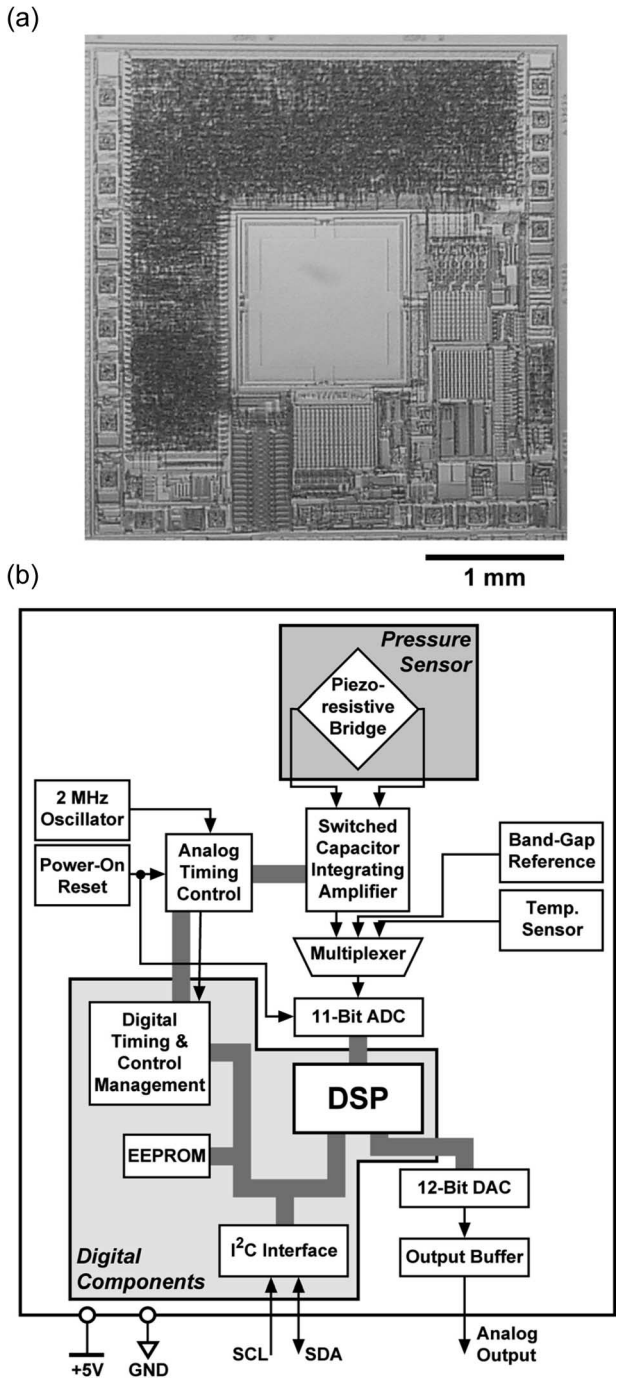

Fig. 10. *(a) Photograph (image courtesy of Dr. N. Kerness, Silicon Microstructures Inc., Milpitas, CA) and (b) system architecture (adapted from [85]) of integrated pressure sensor SM5822/SM5872 by Silicon Microstructures.*

20 factory-programmed coefficients can be used for customized correction of linear and higher order temperature errors and signal nonlinearity correction. The resulting digital word is converted to a ratiometric analog output voltage using a 12-bit digital-to-analog converter. For the end user, the pressure sensor operation requires a minimum of three electrical connections for V_{DD}, GND, and the ratiometric output signal V_{out}. In addition to the analog output, the corrected pressure signal is accessible through a digital I^2C interface. Incorporation of a DSP-based correction engine enables customized calibration and correction procedures. The on-chip EEPROM allows to program coefficients into the SoC multiple times for real-time programming during manufacturing and assembly. In contrast to laser-trimming technologies, the electronic trimming enables final programming after device encapsulation, i.e., the effect of packaging-induced stresses on the pressure signal can be compensated. The price to pay is the additional processing required for EEPROM cells. The sensor system is factory-tested at multiple temperatures and pressures and factory-programmed through the digital interface. The total error of the resulting pressure sensor system is smaller than 1 %FS over the operating temperature range from −40 °C to 125 °C [85].

An example of an integrated microsensor providing solely a digital output is Infineon Technologies' KP100 pressure sensor for side airbag applications [25], [86], [87]. As mentioned earlier, the microsystem is based on a 0.8-μm BiCMOS technology with an intra-CMOS surface micromachining module to release the capacitive pressure sensors. In order to increase the capacitance signal, several polysilicon pressure sensor structures are combined in arrays. A Wheatstone bridge arrangement with two sensor arrays and two reference arrays is used to subtract the zero-pressure capacitance from the sensor signal. Additional calibration capacitors allow offset compensation. A combination of an oversampling $\Sigma\Delta$ converter, a digital decimation filter and a digital low-pass filter converts the analog sensor signal in a 16-bit digital signal at a rate of 7.8 kHz, which is transferred off-chip via an integrated SPI. This interface also communicates information from a number of implemented diagnostic modes and is used to access polysilicon-fuse arrays for programming the trim parameters. With the KP120, Infineon Technologies offers a similar pressure sensor system, which, however, provides an analog signal output for barometric air pressure (BAP) applications [86]. An implemented serial interface is only used for programming at the manufacturing site.

Other examples of SSoC with on-chip digital interface include gas/liquid-flow and humidity sensors commercialized by Sensirion [88] and different chemical-sensing systems developed at ETH Zurich [3], [89]–[92]. These CMOS-based chemical microsystems include, on a single chip, arrays of (different) chemical sensors, the necessary sensor biasing and analog front-end signal conditioning circuitry, analog-to-digital converters, and a serial interface (I^2C interface). Each chip can be identified by a hard-wired address and several sensing chips, controlled by a single microprocessor, can be combined to form a customized chemical sensing system for, e.g., detection

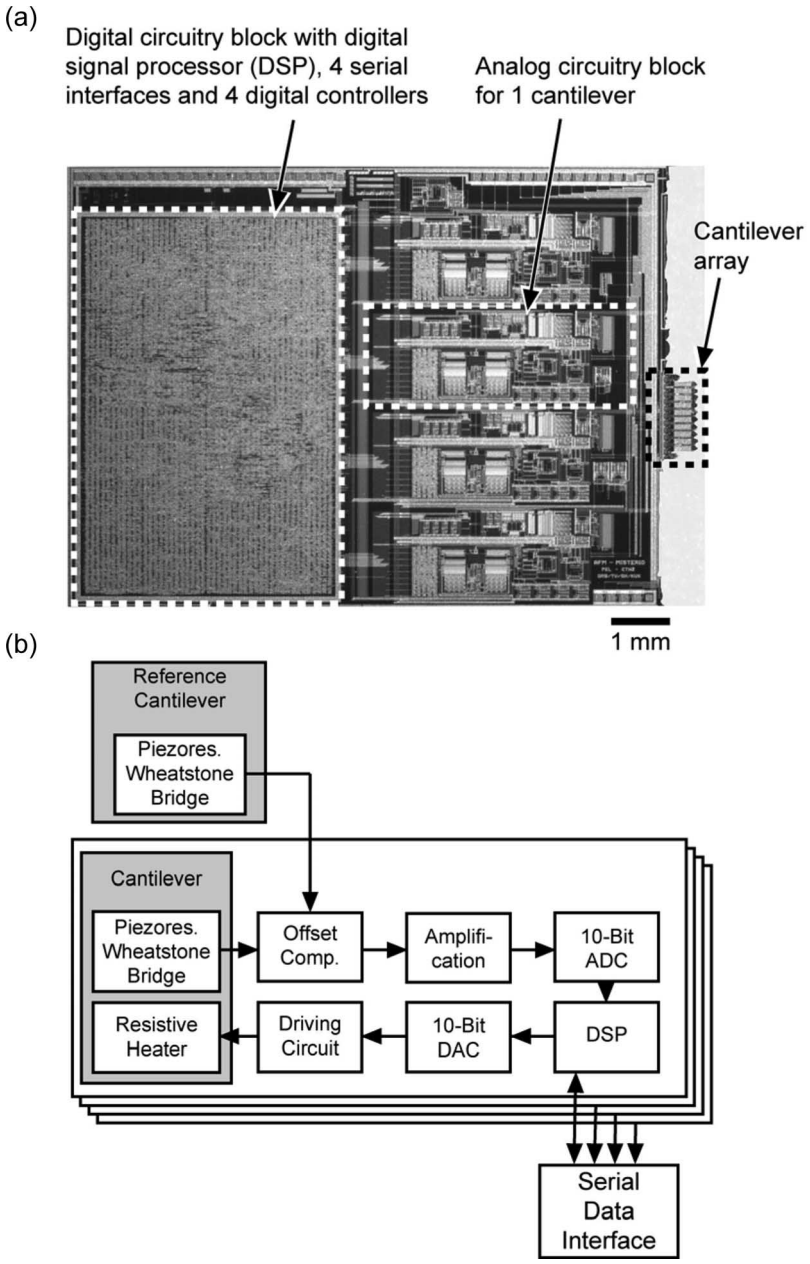

Fig. 11. *(a) Micrograph of a single-chip AFM system, showing the DSP, the four identical analog circuitry units to control four of the ten cantilevers of the integrated cantilever array, and the micromachined sensor array with ten cantilevers and two reference cantilevers (image courtesy of S. Hafizovic, ETH Zurich, Switzerland). (b) System architecture of the integrated AFM system; the four frames indicate the circuitry parts that are repeated for each active cantilever (adapted from [93]).*

of volatile organic compounds in air [89], [90]. Arrays of chemical sensors coated with different chemically sensitive layers in combination with feature extraction algorithms provide the required selectivity toward a specific target analyte, even though the individual sensor is not highly selective [3].

Recently, a CMOS-based atomic force microscope (AFM) on a single chip has been demonstrated [93], [94] [see Fig. 11(a)], making extensive use of digital circuitry. The microsystem includes an array of micromachined cantilevers with integrated piezoresistive sensing structures and thermal bimorph actuators for individual deflection. To enable constant-force imaging with the array without any external controller, each cantilever is embedded in an on-chip analog/digital mixed signal circuitry architecture shown in Fig. 11(b). The output signal of the piezoresistive Wheatstone bridge is offset compensated (using signals from a reference cantilever which is not in

contact with the surface), amplified, filtered and translated into the digital domain with a 10-bit ADC. For maximum system flexibility, all control operations are handled in the on-chip DSP. For constant-force imaging, the DSP blocks can be configured to act as proportional-to-integral-derivative (PID) controllers. Furthermore, the controllers feature averaging functions to enhance force resolution and compensate for the inherent crosstalk between the on-chip sensing and actuator structures. The DSP unit for four cantilevers has a computing power of 16 million arithmetic operations per second, generating up to 105 actuation signals per second per cantilever. The cantilever actuation signals generated by the DSP are converted back into the analog domain with a 10-bit DAC and applied to the thermal actuators via a dedicated analog driving circuitry. Data are transferred off-chip through integrated serial interfaces. The microsystem can be used to perform multiple force-distance measurements or for constant-force imaging if combined with an x-y scanning unit [93]. The chip measures 7 by 10 mm^2 and was fabricated with a 0.8-μm double-metal, double-polysilicon CMOS process (austriamicrosystems, Unterpremstaetten, Austria) in combination with a post-CMOS micromachining module.

SSoCs with embedded general-purpose microcontroller cores are relatively rare. Examples include a pressure sensor system [95] and an integrated pH-meter [96]. Both microsystems are based on a Motorola (now Freescale) 68HC05 core. While the pressure sensor system requires a post-CMOS micromachining module and silicon-on-insulator (SOI) wafers as starting material to release a silicon membrane, the ion-selective FET (ISFET) of the pH-meter uses a floating-electrode design, which can be completely formed within the used 0.6-μm CMOS process.

From a technological point of view, an SSoC with embedded microcontroller can be done and we will likely see more examples in the future. Whether they will become commercially available depends mainly on their economical competitiveness with hybrid solutions, separating the sensor and front-end electronics from the digital core. Cointegration seems to be especially suited for high-volume applications and for sensing systems requiring only minor modifications to the base CMOS technology. Finally, the system cost will determine whether a monolithic integration as SoC or a hybrid integration as, e.g., a system-in-package (SiP) is preferable. Tire pressure monitors are potential candidates for an SSoC. With an estimated volume of 120 million–150 million units per year by 2008 [97], many semiconductor and sensor companies now offer or are in the final development stages of direct tire-pressure monitoring systems (or components thereof) based on micromachined pressure sensors. Currently, the sensing units mounted inside the tire are multichip solutions comprising a sensor chip (potentially with on-chip electronics), a microcontroller, and a wireless transmitter/receiver to communicate with the vehicle's information system. Freescale Semiconductor's solution currently uses a microcontroller with embedded RF electronics to cointegrate the latter two components, effectively only requiring a battery, the sensor chip and the microcontroller chip on a small printed circuit board (PCB) with integrated antenna [79]. Because of the expected high production volumes, further system integration in the near future is likely.

IV. CONCLUSION

Various fabrication approaches to cointegrate micromachined sensors with microelectronic circuitry have been successfully implemented over the past decades and an increasing number of SSoCs are commercially available. Even though very complex integrated sensing systems with extensive digital circuitry have been demonstrated recently, showcasing today's technological capabilities in this area, the optimal amount of system integration will depend on the particular application and ultimately the system cost in comparison to alternative solutions. In certain applications, a microcontroller might be already available, "only" requiring a sensing system with standardized analog (or digital) output format. Other microsystems, such as the above-mentioned wireless tire pressure monitors, are likely to benefit from higher integration levels. With continuous advances in miniaturization and integration, the trend toward cointegration of sensing and circuitry functions is likely to continue. Besides system cost, the benefit of added system features, such as calibration, self-test, and standardized communication via bus interfaces, is fueling this trend. Moreover, sensor arrays and sensor networks for, e.g., chemical and biochemical surveillance applications demand for substantial circuit integration in order to reduce system-level complexity.

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