A Calibrated Pulse Generator for Impulse-Radio UWB Applications

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***Abstract*—A 100-Mb/s pulse position modulation generator is presented for impulse-radio ultra-wideband applications. The pulse generator provides a data rate of 100 Mb/s and a pulse width of 1 ns. To achieve an accurate pulse position and pulse width, a mixed-mode calibration circuit is used to calibrate the output buffer of the delay-locked loop. The proposed circuit has been fabricated in a 0.35-μm CMOS process. After the calibration, the measurement results show that both the pulse-width error and the pulse-position error are less than 4%.**

***Index Terms*—Calibration, delay-locked loop (DLL), pulse generator, pulse-position modulation, ultra-wideband (UWB).**

I. Introduction

ULTRA-WIDEBAND (UWB) wireless transceivers are becoming a promising technique for short-distance and high-data-rate communications. There are several ways to implement a UWB transceiver [1]. In this paper, an impulse-radio UWB system is adopted due to its simplicity. Because it is a baseband (carrier-free) technique, no up-/down-conversions or mixers are needed. It may greatly reduce the complexity and cost of the chip. Therefore, the impulse-radio UWB system is a good candidate to be integrated with today's low-cost CMOS circuits.

Several circuit topologies can be used to generate the pulse trains for UWB systems. One researcher used monocycle pulse generators and filters to generate the pulse trains [2], [3], and others have used digital gates [4], [5]. For pulse generators utilizing digital gates, a multiphase clock should be provided. Both phase-locked loops (PLLs) and delay-locked loops (DLLs) can serve as a clock source. A DLL is easier to be implemented and has better jitter performance than a PLL. Due to the process variations and mismatches, the delay times are not equal for delay cells [6]. In [6], many calibration loops are used to calibrate the delays. This may increase hardware cost and introduce mismatch among the calibration loops. In this paper, a mixed-mode calibration circuit [7] is used to avoid mismatch among the calibration circuits and reduce the number of calibration circuits.

This paper is organized as follows. Section II introduces this pulse-position modulation (PPM) generator and its building blocks. The mixed-mode calibration method is analyzed in Section III. The experimental results are given in Section IV, and the conclusions are given in Section V.

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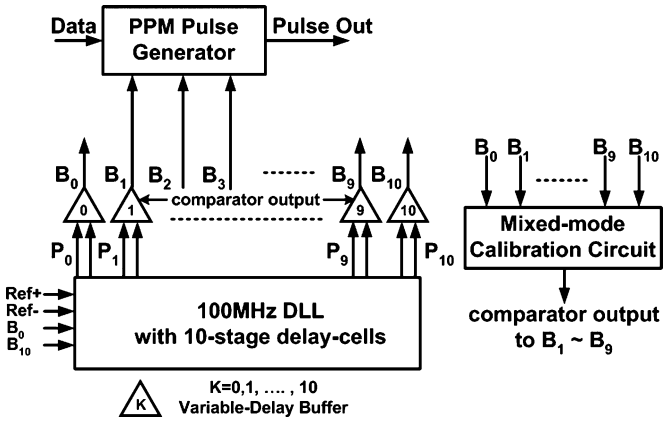


Fig. 1. PPM generator.

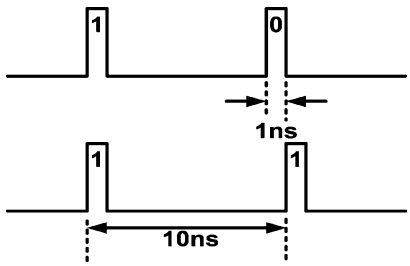


Fig. 2. Ideal PPM pulse output.

II. Circuit Description

The proposed PPM generator is shown in Fig. 1. It is composed of a DLL with ten delay cells, a mixed-mode calibration circuit, eleven variable-delay buffers (VDBs), and a pulse generator. With an input reference clock of 100 MHz, 1-ns spacing can be produced between adjacent delay cells. At the beginning, the main DLL is locked by comparing the signals B_0 and B_{10} in Fig. 1. Then, the mixed-mode calibration circuit starts to sense the spacing among the remaining outputs of VDBs. It tries to calibrate the delay time to the desired value of 1 ns.

After the calibration is completed, three of the calibrated VDB's outputs are sent into the PPM pulse generator, and the pulse train will be produced at the output. The ideal pulse train waveform is shown in Fig. 2. The pulse train has a pulse repetition rate of 100 Mb/s and a pulse width of 1 ns. When the input data switch from 0 to 1, the generated pulse will be postponed for 1 ns to realize the PPM pulses. The circuits of Fig. 1 will be discussed in detail in the following.

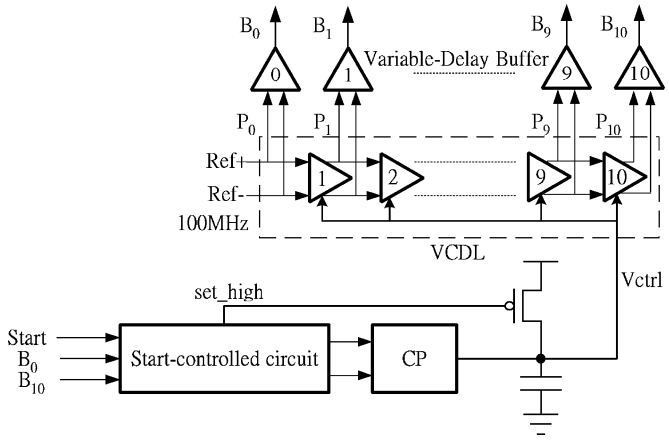


Fig. 3. DLL.

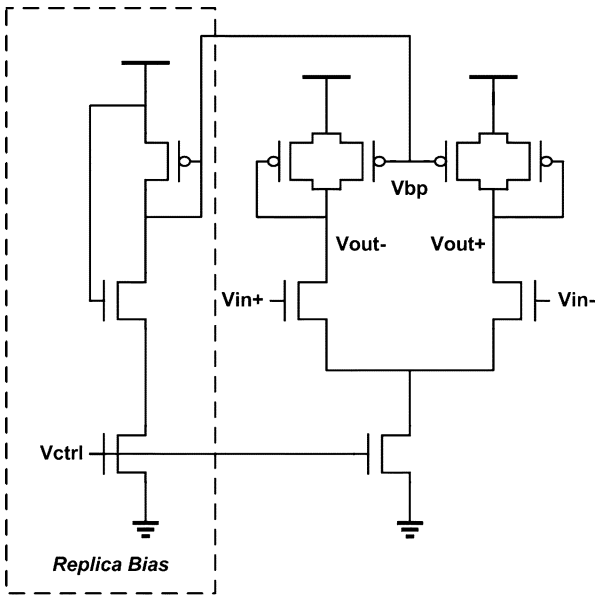


Fig. 4. Delay cell.

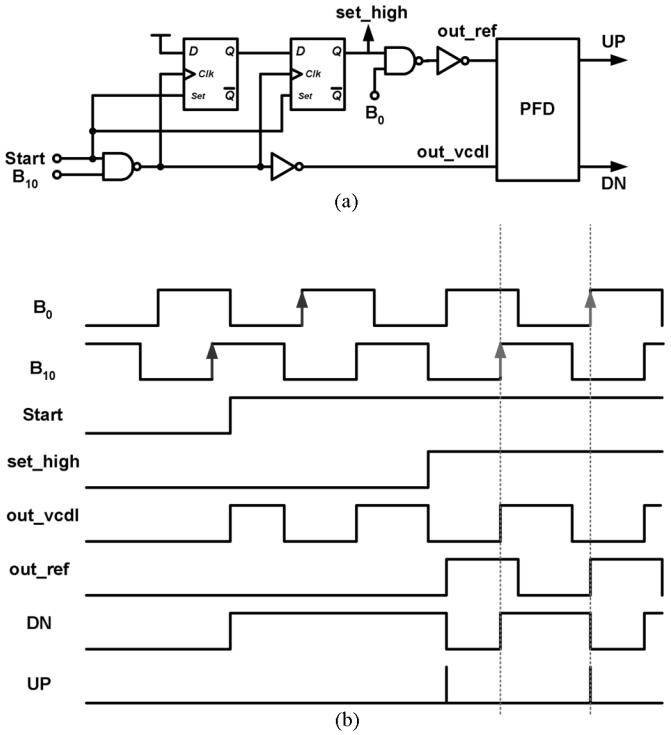


Fig. 5. (a) Start-controlled circuit. (b) Timing diagram of the start-controlled circuit.

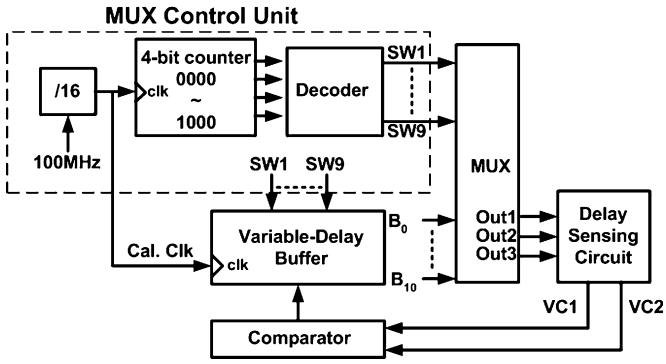


Fig. 6. Mixed-mode calibration circuit.

A. DLL

The DLL is shown in Fig. 3. This DLL is composed of ten delay cells, a start-controlled circuit, a charge pump, and a capacitor. The delay cell is a differential amplifier with symmetric loads as shown in Fig. 4 [8]. A replica bias circuit is used to maintain the output amplitude under all control voltages. Each delay cell may provide a delay range from 0.67 to 2 n to make the DLL function correctly from 50 to 150 MHz. For a conventional DLL, the delay time $T_{\rm vcdl}$ of the voltage-controlled delay line (VCDL) must satisfy the following equation:

$$0.5 \cdot T_{\rm clock} < T_{\rm vcdl} < 1.5 \cdot T_{\rm clock} \tag{1}$$

where $T_{\rm clock}$ represents the input reference clock period of 10 ns. Due to the PVT variations, it is hard to constrain the delay time within the specific range. To avoid the harmonic locking problem, a start-controlled circuit [9] is used to ensure normal locking and have a correct VCDL. The start-controlled circuit is shown in Fig. 5(a), and its timing diagram is shown in Fig. 5(b). In the beginning, this circuit will charge the control voltage to the supply voltage by the signal "set_high," and the delay cell has the shortest delay time. When the signal "start" goes up, the start-controlled circuit neglects the first rising edge of the signal $\rm B_0$ and avoids the false lock problems. When the DLL is locked, it aligns the phases of $\rm B_0$ and $\rm B_{10}$ in Fig. 1. The time difference between $\rm B_0$ and $\rm B_{10}$ is 10 ns.

B. Mixed-Mode Calibration Circuit

The mixed-mode calibration circuit aims to adjust the VDBs and has the time spacing of 1 ns. It consists of a delay sensing circuit (DSC), a comparator, a multiplexer (MUX), and the MUX control unit, as shown in Fig. 6. The basic principle takes the DSC to sense three VDBs' outputs [10]. One can compare two time differences among three adjacent VDBs to adjust the delay of the central buffer. For example, if $\rm B_0$, $\rm B_1$, and $\rm B_2$ are sent to the DSC, then $\rm T_1$ is defined as the time difference between $\rm B_0$ and $\rm B_1$. Similarly, $\rm T_2$ is defined as the

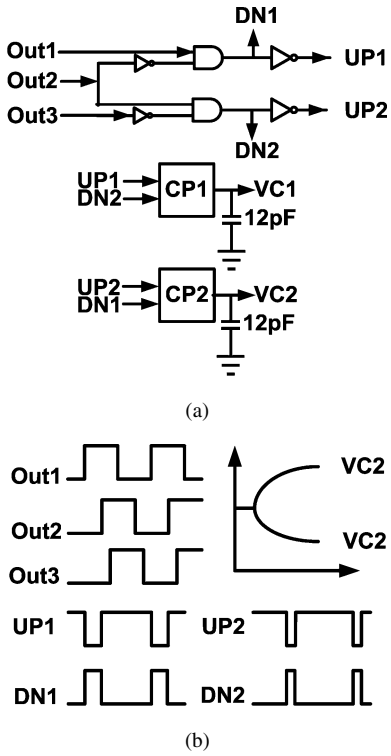


Fig. 7. (a) DSC. (b) Timing diagram of the DSC.

time difference between B_1 and B_2. Then, the DSC performs the time-to-voltage conversion by using the charge pumps and loop filters to compare T_1 with T_2. Assume the bias current I_1 of the buffer B_1 is digitally programmable. The calibration algorithm is

$$I_1 \text{ is increased,} \quad \text{if } T_1 > T_2 \tag{2a}$$

$$I_1 \text{ is decreased,} \quad \text{if } T_1 < T_2. \tag{2b}$$

The process is repeated for the remaining VDBs until the calibration is complete.

Intuitively, nine DSCs are needed to calibrate the signals $\mathrm{B}_1 \sim \mathrm{B}_9$ (assume that B_0 and B_{10} are locked to 2π). However, this may introduce a lot of hardware and power consumption. To avoid this problem, the MUX and the MUX control unit are adopted to reuse this DSC. A divide-by-16 counter generates the calibration clock, and this calibration clock is connected to a 4-bit counter, which counts from 0000 to 1000. Then, the counter outputs are sent to a decoder to generate the nine switching signals SW1–SW9. The nine switching signals control the MUX to select sequentially three consecutive buffers' outputs (e.g., B_1, B_2, and B_3) for the DSC to save the hardware.

The DSC is shown in Fig. 7(a), and it is composed of an up/down signal generator, two charge pumps, and two capacitors. Its timing diagram is shown in Fig. 7(b). When three outputs from the MUX are sent into the DSC, the up/down signal generator produces four signals, UP1, DN1, UP2, and DN2, for two charge pumps to charge/discharge two capacitors. They generate the voltage being proportional to the time difference. If two time differences among three outputs are not equal, the comparator shown in Fig. 8 following the DSC produces a high/low signal to increase/decrease the delay time of the VDB. Then, after several calibration cycles, nine VDB outputs will be calibrated to have the equal time spacing of 1 ns.

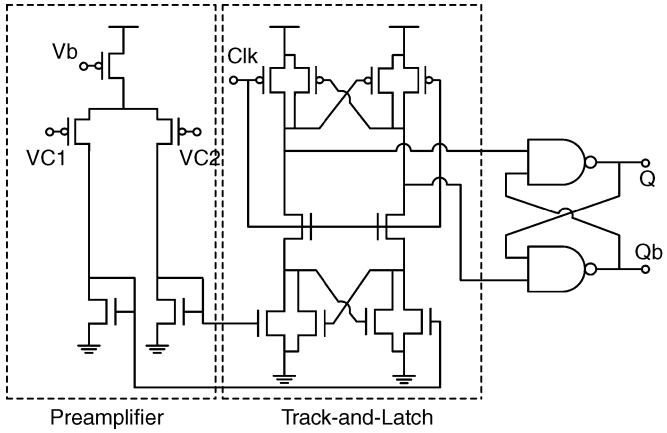


Fig. 8. Comparator.

C. Variable-Delay Buffer

The VDB is shown in Fig. 9(a). It is composed of an up/down counter and a buffer with a 3-bit binary-weighted current source in Fig. 9(b). Because the signal generated by the comparator is only 1-bit, a 3-bit up/down counter is triggered by the calibration clock. With this manner, the current through the buffer can be increased or decreased to set the appropriate delay time. There are eleven VDBs in Fig. 1, but the first and last buffers' current sources are fixed. Only nine buffers in Fig. 1 are controlled by the mixed-mode calibration circuit. Because there is only one comparator in the calibration circuit, nine switching signals from the decoder in Fig. 6 select the desired VDB to calibrate.

D. PPM Pulse Generator

After all of the VDBs are calibrated, the calibrated buffers' outputs are used to generate the PPM pulse. The PPM pulse generator is shown in Fig. 10. It is composed of AND gates, inverters, a two-to-one multiplexer, and the output buffer. Taking two adjacent buffers' outputs into the PPM pulse generator, it generates a pulse with the pulse width of 1 ns. Similarly, the next two adjacent buffers' outputs with the delay of 1 ns from previous ones are used to produce another pulse, which is delayed by 1 ns compared with the previous one. Therefore, the data are used to select the multiplexer to have the pulse train similar to Fig. 2. In this work, the differential input reference clock (Ref+ and Ref- in Fig. 1) and input data are both generated by a pattern generator so they are synchronized automatically. The relative phase between reference clock and input data can also be adjusted by the pattern generator. Compared with [4] and [5], although the modulation scheme is different, the PPM pulse generator is suitable for PPM applications because of the calibrated pulse widths and pulse positions.

III. Mixed-Mode Calibration Method

The calibration principle was described in the previous section. However, it should be discussed further to gain more in-

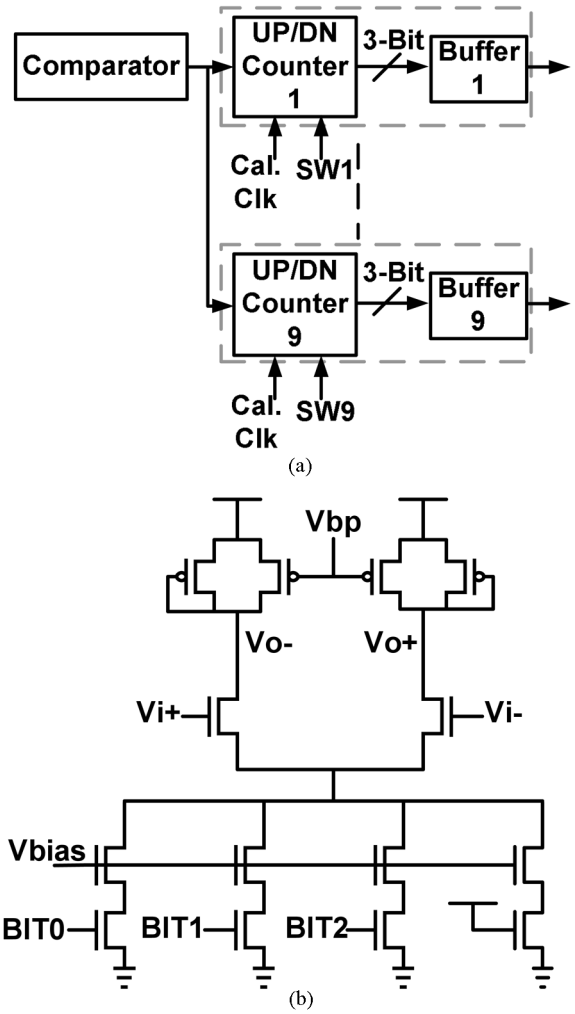


Fig. 9. (a) VDBs. (b) Buffer core.

sight for design considerations. Basically, the calibration procedure is similar to that of [11], but some modifications are made for our applications. First of all, to ensure the loop stability, the calibration process should not affect the main DLL. As shown in Fig. 1, there are eleven output buffers ($\mathrm{B}_0 \sim \mathrm{B}_{10}$) connected to the DLL. The initial time difference between two adjacent output buffers is defined as

$$T_i = \text{the time difference between } \mathrm{B}_{i-1} \text{ and } \mathrm{B}_i, \quad i = 1 \sim 10. \tag{3}$$

Assume that the DLL is locked and the time difference between B_0 and B_{10} is T_{clock}, which is 10 ns. In order not to affect the DLL's operation, the following equation should always be satisfied:

$$\sum_{i=1}^{10} T_i = T_{\mathrm{clock}}. \tag{4}$$

Based on the analysis in [11], the calibration algorithm makes ten time differences ($T_1 \sim T_{10}$) as equal as possible. A calibration round is defined as the time that nine VDBs are calibrated. Assume infinite calibration rounds are adopted and the updated

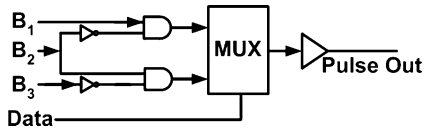


Fig. 10. PPM pulse generator.

step of the delay of the VDBs is extremely small. The final time differences are given in [11] as

$$T_{i,\mathrm{final}} = \frac{\sum_{k=1}^{10} T_{k,\mathrm{initial}}}{10}, \qquad i = 1 \sim 10 \tag{5}$$

where $T_{k,\mathrm{initial}}$ is the time difference of the$k$th VDB before calibration and $T_{i,\mathrm{final}}$ is the time difference of the ith VDB after calibration. In (5), all of the time differences are equal and (4) still holds. However, it is not correct for the mixed-mode calibration method. Because the updated step is not small, any two consecutive time differences are not perfectly averaged. As a result, some modifications should be made to fit for the actual case. As described in the previous section, the mixed-mode calibration circuit will calibrate the outputs from $\mathrm{B}_1 \sim \mathrm{B}_9$. Therefore, in the first calibration round, nine comparisons and corrections are made to update $\mathrm{T}_1 \sim \mathrm{T}_9$. For every comparison, the time difference is corrected and updated according to (2).

Now, the updated step of the delay of the VDBs is defined as ΔT. After the first calibration round, nine sets of the consecutive time differences are compared and the updated time difference is given as

$$\begin{cases} T_i' = T_i + \Delta t_i, & \text{for } i = 1 \\ T_i' = T_i - \Delta t_{i-1} + \Delta t_i, & \text{for } i = 2 \sim 9 \\ T_i' = T_i - \Delta t_{i-1}, & \text{for } i = 10 \end{cases} \tag{6}$$

where Δt_i means the updated step after T_i and T_{i+1} are compared with each other. Δti may be $+\Delta T$ or $-\Delta T$ according to the comparison result between T_i and T_{i+1}. Not to affect the DLL, (4) should hold. Based on (4) and (6), the summation of all the ten time differences after one calibration round is

$$\begin{aligned} \sum_{i=1}^{10} T_i' &= T_1 + \Delta t_1 + T_2 - \Delta t_1 + \Delta t_2 + T_3 - \Delta t_2 + \Delta t_3 + \\ &\quad \ldots\ldots + T_{10} - \Delta t_9 \\ &= T_{\mathrm{clock}}. \end{aligned} \tag{7}$$

This means that the DLL is not influenced.

Although a steady-state condition in (5) has been derived by [11], this is not the case in the actual case. The final timing differences do not converge to unique values, and they are bounded in a constrained range. Assume that the ith time difference enters the final steady state or the final bounded region after $N_{i,\mathrm{steady}}$ cycles. According to (6), the ith final timing difference, $T_{i,\mathrm{final}}$, is represented as

$$\begin{cases} T_{i,\mathrm{final}} = T_{i,\mathrm{static}} \pm \mathrm{mod}_2(N) \cdot \Delta T, & \text{for } i = 1 \\ T_{i,\mathrm{final}} = \begin{cases} T_{i,\mathrm{static}} \pm \mathrm{mod}_2(N) \cdot 2\Delta T \\ \text{or} \\ T_{i,\mathrm{static}}, \end{cases} & \text{for } i = 2 \sim 9 \\ T_{i,\mathrm{final}} = T_{i,\mathrm{static}} \pm \mathrm{mod}_2(N) \cdot \Delta T, & \text{for } i = 10 \end{cases} \tag{8}$$

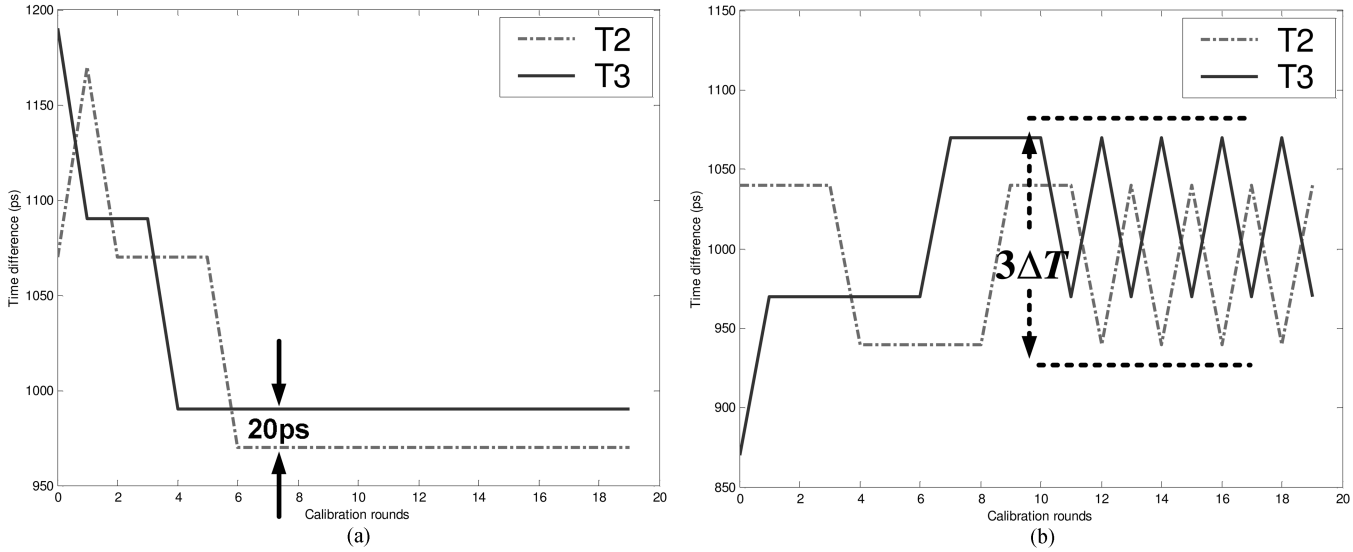


Fig. 11. (a) $T_{2,\mathrm{final}}$ and $T_{3,\mathrm{final}}$ settle to the static time differences, respectively. (b) $\mathrm{T}_{2,\mathrm{final}}$ and $\mathrm{T}_{3,\mathrm{final}}$ bounce within $2\Delta\mathrm{T}$ (100 ps) in a reverse fashion.

where N is the number of the calibration rounds performed, $\mathrm{mod}_2()$ is the signed remainder after division by 2, and $T_{i,\mathrm{static}}$ are constants $(i = 1 \sim 10)$. These equations indicate that the final time difference will be a static time difference or it will bounce within a specific range, which is determined by the finite updated step ΔT.

In Section II, the pulse generator utilizes the buffers $\mathrm{B}_1 \sim \mathrm{B}_3$ to generate the output PPM pulse. Hence, the final timing differences $T_{2,\mathrm{final}}$ and $T_{3,\mathrm{final}}$ determine the output pulse width and pulse spacing. From (8), both $T_{2,\mathrm{final}}$ and $T_{3,\mathrm{final}}$ may bounce within $2\Delta T$. In the worst case, they may even increase or decrease in a reverse fashion. Hence, it seems that the maximum relative error between $T_{2,\mathrm{final}}$ and $T_{3,\mathrm{final}}$ is $4\Delta T$. However, it would not happen. If $T_{2,\mathrm{final}} = T_{2,\mathrm{static}} + 2\Delta T$, and $T_{3,\mathrm{final}} = T_{3,\mathrm{static}} - 2\Delta T$ in a certain calibration round, $T_{3,\mathrm{static}}$ must be larger than $T_{2,\mathrm{static}} + \Delta T$ or $T_{2,\mathrm{final}}$ may not increase twice in this calibration round. As a result, the worst cases happen when the following equations are satisfied:

$$T_{2,\mathrm{final}} = T_{2,\mathrm{static}} \pm \mathrm{mod}_2(N - N_{2,\mathrm{steady}}) \cdot 2\Delta T \quad (9a)$$

$$T_{3,\mathrm{final}} = T_{3,\mathrm{static}} \mp \mathrm{mod}_2(N - N_{3,\mathrm{steady}}) \cdot 2\Delta T \quad (9b)$$

$$\mathrm{mod}_2(N - N_{2,\mathrm{steady}}) = \mathrm{mod}_2(N - N_{3,\mathrm{steady}}) \quad (9c)$$

$$T_{2,\mathrm{static}} = T_{3,\mathrm{static}} \mp \Delta T \quad (9d)$$

where (9a)–(9c) indicate that $T_{2,\mathrm{final}}$ and $T_{3,\mathrm{final}}$ increase or decrease in a reverse fashion. In these cases, the absolute maximum relative error is $3\Delta T$. Therefore, the relative error between $T_{2,\mathrm{final}}$ and $T_{3,\mathrm{final}}$ is written as

$$-3\Delta T \le (T_{2,\mathrm{final}} - T_{3,\mathrm{final}}) \le +3\Delta T. \quad (10)$$

The behavior simulation is performed to justify the equations as shown the above. Assume 20% random mismatch among the buffers and the finite updated step, ΔT, is set to 50 ps. The simulation results for the final time differences, $T_{2,\mathrm{final}}$ and $T_{3,\mathrm{final}}$, are shown in Fig. 11(a) and (b). Fig. 11(a) shows the case that both $T_{2,\mathrm{final}}$ and $T_{3,\mathrm{final}}$ settle to the static time difference, respectively. Fig. 11(b) shows the case that $T_{2,\mathrm{final}}$ and $T_{3,\mathrm{final}}$ increase or decrease within $2\Delta T$ (100 ps) in a reverse fashion. The result shows that the absolute maximum relative error will be less than $3\Delta T$ (150 ps), as indicated by (10).

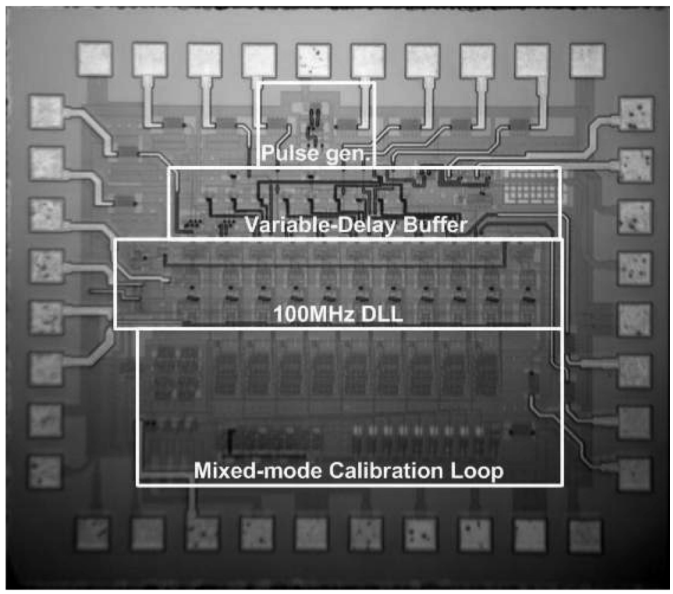


Fig. 12. Die photograph.

IV. Experimental Results

The proposed circuit has been realized in a 0.35-μm CMOS process and has a total area of 1.5 mm $\times$ 1.3 mm. Its die photograph is shown in Fig. 12. The total power dissipation is 180 mW from a 3.3-V supply. The proposed circuit is realized on a two-layer FR4 board.

Fig. 13 shows the input (B_0) and output (B_{10}) waveforms of the DLL. They are locked to make the total delay time 10 ns. The output waveforms for $\mathrm{B}_0 - \mathrm{B}_3$ before and after calibration are also measured. The output waveforms for VDBs before and after calibration are shown in Fig. 14(a) and (b), respectively. After

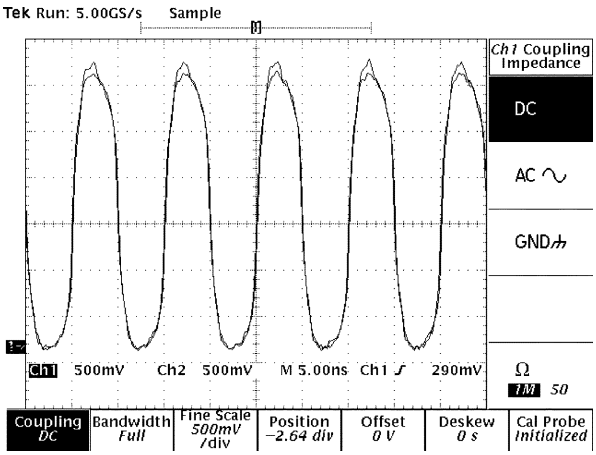
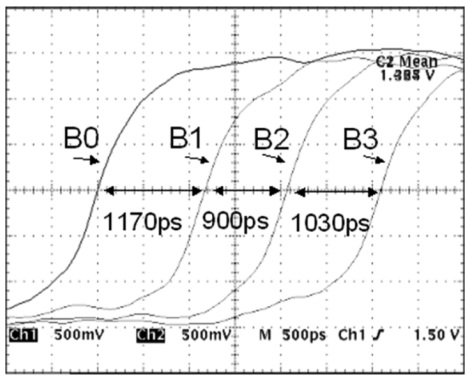
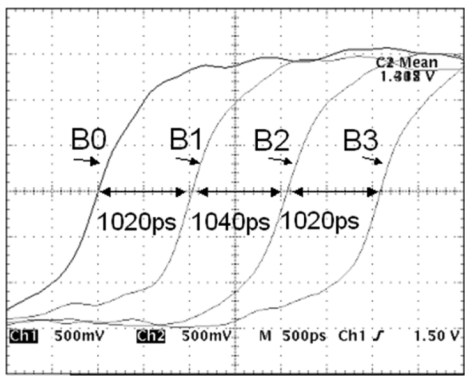


Fig. 13. Input and output of the DLL under locking.

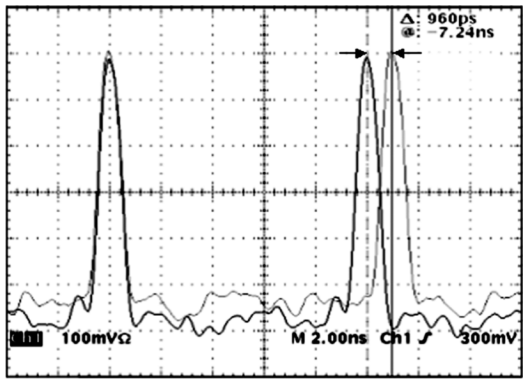


(a)

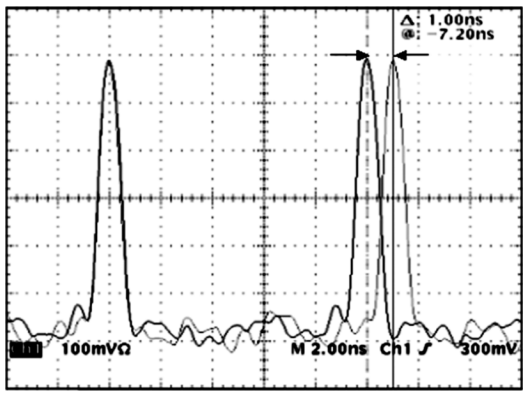


(b)

Fig. 14. Output waveforms of VDBs (a) before and (b) after calibration.



(a)



(b)

Fig. 15. Output of the pulse generator (a) before and (b) after calibration.

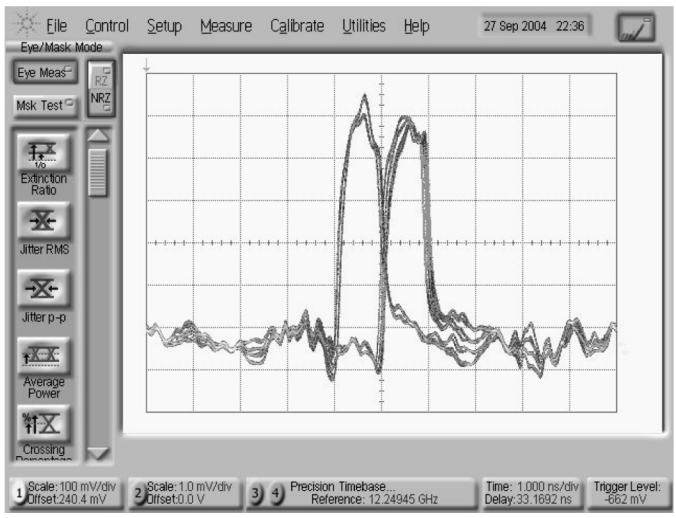


Fig. 16. Measured PPM eye diagram ($2^{31}-1$ PRBS); horizontal: 1 ns/div; vertical: 100 mV/div.

calibration, the measured error of the pulse spacing is reduced to be within 4%.

The output waveforms of the pulse generator before and after calibration are also measured in Fig. 15(a) and (b), respectively. In order to show the PPM function, we demonstrate the calibration result with a relatively large timing span. Therefore, it is hard to determine the final calibration resolution from this figure. However, because the pulse position difference is mainly determined by the timing spacing of the VDBs, we still can declare a 4% error by the VDBs' calibration results shown in Fig. 14(a) and (b). To the authors' knowledge, there is no clear specification for the impulse-radio UWB systems because that they are still under development. If we neglect the channel nonidealities and assume that the output pulses are triangular shape with 0.05-UI rms jitter, we can derive a BER less than 10^{-2} under a 10% pulse width and pulse position error. If the pulse width and pulse position error can be reduced to 5%, the BER is less than 10^{-4}, which is sufficient for general wireless systems. Hence, the developed 4% error should be satisfactory.

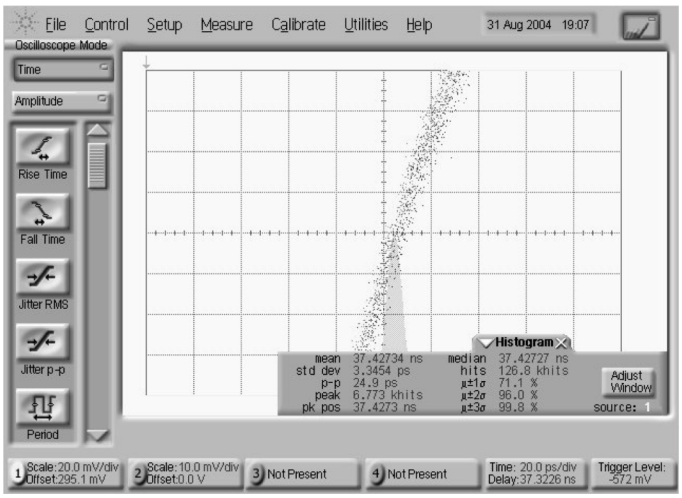


Fig. 17. Jitter histogram; horizontal: 20 ps/div; vertical: 20 mV/div.

TABLE I
PERFORMANCE SUMMARY

Process	CMOS 0.35um
Die area	1.5mm x 1.3mm
Supply	3.3V
Power consumption	180mW
Data rate	100Mbps
Pulse width	1ns ±4%
Pulse position difference	1ns ±4%
Rms jitter	3.35ps
Peak-to-peak jitter	24.9ps

To demonstrate the data-dependent jitter performance, Agilent 86130A generates a $2^{31} - 1$ PRBS signal as input data. The measured PPM eye diagram and the measured jitter histogram are shown in Figs. 16 and 17, respectively. The results are measured by Agilent 86100B Wide-Bandwidth Oscilloscope. The rms and peak-to-peak jitters are 3.35 and 24.9 ps, respectively. The performance summary of this chip is listed in Table I.

V. CONCLUSION

A calibrated PPM pulse generator for UWB applications has been fabricated in a 0.35-μm CMOS process. The DLL-based topology facilitates the PPM pulse generator using only one 2-1 MUX and simple logic gates. By using the mixed-mode calibration circuit, the delay times for the multiple outputs of the DLL are calibrated to a correct value. Experimental results demonstrate the feasibility.

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