# An SC Voltage Doubler with Pseudo-Continuous Output Regulation Using a Three-Stage Switchable Opamp

Hoi Lee, *Member, IEEE*, and Philip K. T. Mok, *Senior Member, IEEE*

***Abstract*—This paper presents a switched-capacitor voltage doubler using pseudo-continuous control (PCC). The proposed PCC does not require extra power transistor to continuously regulate the output of the doubler, thereby saving chip area. The PCC also allows the doubler to operate at lower switching frequencies without sacrificing transient response. The light-load efficiency of the regulated doubler can thus be enhanced by reducing the switching power loss. In addition, a three-stage switchable opamp with time-multiplexed enhanced active-feedback frequency compensation is developed to implement the controller. The proposed implementation enhances the speed of the loop response and then improves the load transient response of the regulated doubler.**

**The SC voltage doubler with the proposed PCC controller has been fabricated in a 0.6-$\mu$m CMOS process. The regulated doubler achieves $>87\%$ power efficiency even for the load current of 5 mA. By operating the doubler at switching frequency of 200 kHz and using a output capacitor of 2.2 $\mu$F, a maximum output ripple of 20 mV is maintained for the load current changing from 50 mA to 150 mA. The output transient recovery time of the regulated doubler is $\sim$25 $\mu$s with load-current step changes of 100 mA/1 $\mu$s.**

***Index Terms*—Charge pumps, power management integrated circuits, switched-capacitor regulators, three-stage switchable amplifier, voltage doublers, voltage regulators.**

## I. Introduction

DRIVEN by the growing demand of battery-operated portable electronic devices like PDAs, cellular phones, MP3 players and camcorders in recent years, switched-capacitor (SC) DC-DC regulators capable of delivering hundred-milliampere load current are becoming important for the power management purpose. This is due to the fact that SC regulators are capable to provide up/down DC-DC conversions without inductors and thus generate less conducted electromagnetic interference to other systems compared to switched-mode power converters. Fig. 1 shows a block diagram of an SC regulator, which consists of a power stage and a controller. The power stage is used to carry out DC-DC conversion from the input to the output with different configurations of switches and capacitors, while the controller regulates the output voltage to the desired value against variations of load current and input supply through negative feedback mechanism. When the SC regulator is used in portable applications, it should have four major capabilities: 1) to be highly power efficient especially in light-load conditions for prolonging the battery lifetime; 2) to be low cost in terms of using small-value off-chip capacitors and consuming small chip area; 3) to have accurate output voltage in terms of good line and load regulations as well as small output ripple; and 4) to have fast load transient response. These four major performance requirements of the SC regulator depend on both control scheme and its implementation and are difficult to achieve simultaneously.

Existing control schemes have some issues that limit the performance of the SC regulator [1]–[6]. When the SC regulator is controlled by the reported PWM scheme [1], [2] or quasi-switched method [3], [4], the regulator is operated under discontinuous regime, as the regulated transistors are not connected to the output. The transistor being regulated controls the amount of charge stored in the flying capacitor during the input charge transfer phase. After waiting for half clock period, the charge can then be transferred to the output for regulating the output voltage through other power switches during output charge transfer phase. As a result, the load transient response depends on the clock period or switching frequency of the regulator. In particular, the output transient recovery time can only be reduced by operating the regulator at higher switching frequency. However, higher switching frequency leads to larger switching power loss, which degrades the light-load power efficiency of the SC regulator. In order to allow load transient response independent of switching frequency, the output of the SC regulator needs to be continuously regulated. However, existing continuous output regulation schemes require to use one extra power transistor cascaded either in front of [5] or behind [6] the power stage for regulating the output voltage. The additional power transistor increases the chip area of the regulator. Motivated by above concerns, it is critical to develop an effective control scheme and its implementation to further improve the performance of the SC regulator.

This paper presents a pseudo-continuous control (PCC) for the SC regulator. A cross-coupled voltage doubler shown in Fig. 2(a) is adopted as the power stage of the SC regulator to deliver hundred-milliampere load current [7]–[9]. The cross-coupled doubler contains eight power switches (Sl1-Sl4, Sr1-Sr4), two off-chip flying capacitors ($C_{f1}$, $C_{f2}$) and an

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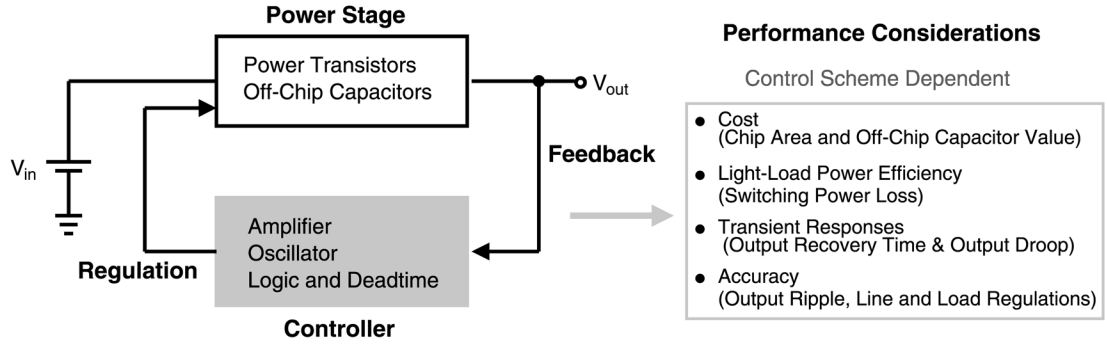


Fig. 1. Block diagram and design considerations of an SC DC-DC regulator.

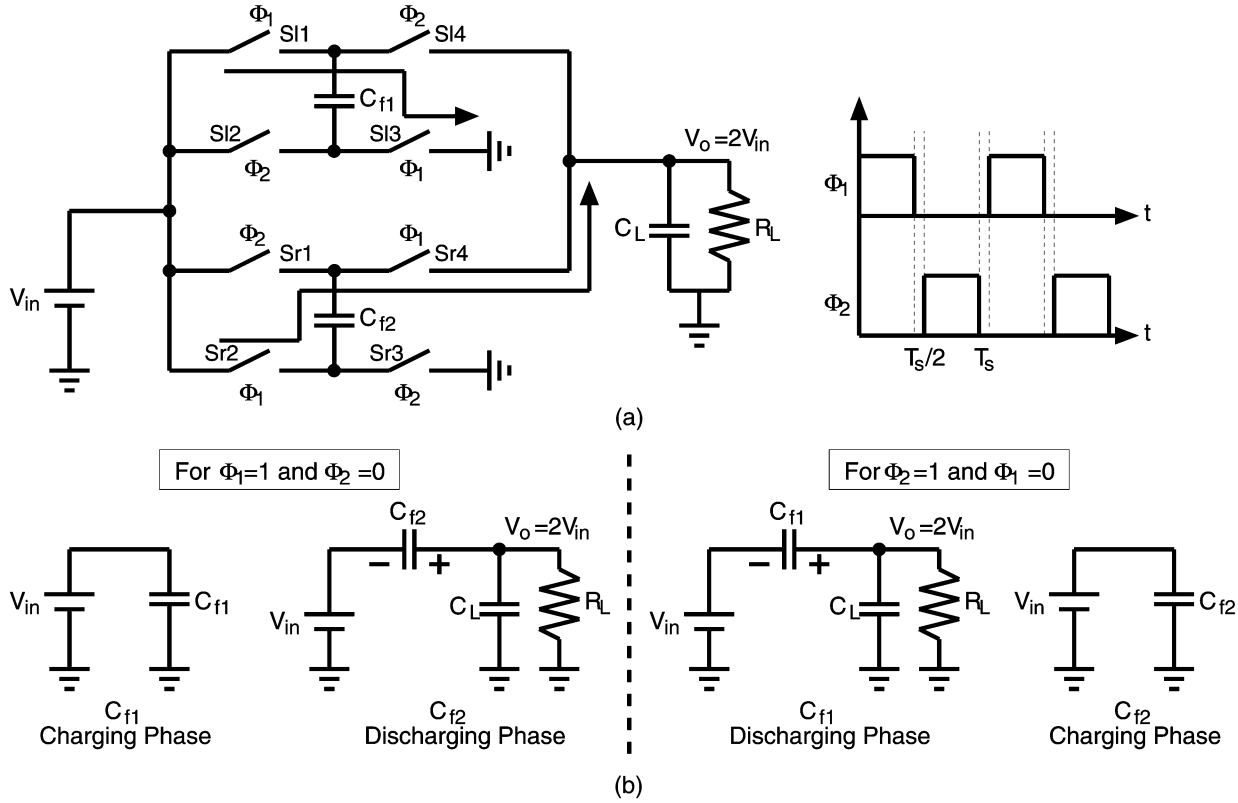


Fig. 2. (a) Cross-coupled voltage doubler and (b) its circuit operation in different clock phases.

output capacitor $C_L$ to give the output voltage of $\sim 2\ V_{\rm in}$ in all clock phases based on operations shown in Fig. 2(b). The cross-coupled design allows the doubler to operate at twice the switching frequency such that either the output ripple or the output capacitor can be halved. With the proposed PCC, the doubler can achieve continuous output regulation without extra power transistor. Therefore, the regulated doubler can operate at lower switching frequencies for minimizing the switching power loss and achieving better light-load power efficiency. A three-stage switchable opamp with time-multiplexed enhanced active-feedback frequency compensation is also developed to implement the controller. The proposed implementation enhances the loop-gain magnitude and loop response, thereby improving the output accuracy and load transient response of the regulated doubler. The paper is organized as follows. Section II discusses the operational principle, control characteristics and implementation considerations of the proposed PCC technique for the cross-coupled voltage doubler. The stability analysis of the regulated doubler by using PCC with a three-stage switchable opamp is addressed in Section III. Sections IV and V then provide the circuit implementation and experimental results of the proposed regulated doubler. Finally, conclusions are given in Section VI.

## II. Proposed Pseudo-Continuous Output Regulation

### A. Principle of Operation

Fig. 3(a) shows the structure of the regulated doubler with the proposed PCC. With PCC, both Ml2 and Mr2 operate as regulation transistors, while other power transistors function as

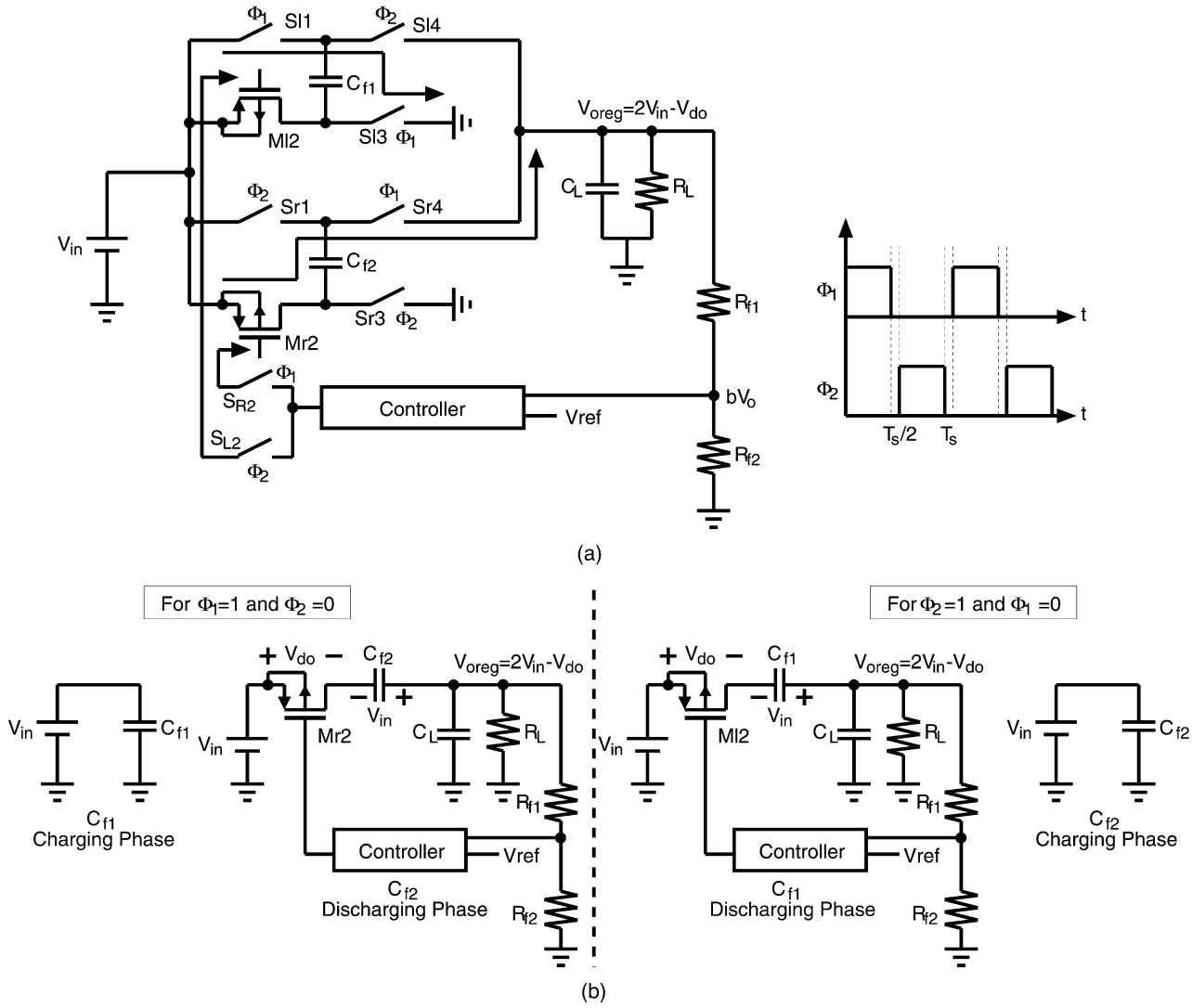


Fig. 3. (a) Proposed regulated voltage doubler with pseudo-continuous output regulation and (b) its circuit operation in different clock phases.

switches. The control mechanism operates in non-overlapping clock phases $\Phi_1$ and $\Phi_2$ alternately and explains in Fig. 3(b). When $\Phi_1 = 1$, both power transistors Sl1 and Sr3 are on and Ml2 and Sl4 are off, so the voltage across $C_{f1}$ is charged to $\sim V_{\rm in}$. At the same time, Mr2 and Sr4 are on and $C_{f2}$ is in the discharging phase. Since the switch $S_{R2}$ is on, an appropriate dropout voltage $V_{\rm do}$ is regulated across Mr2 by the proposed controller through negative feedback. As a result, a regulated output voltage $V_{\rm oreg}$ is kept at the desired value of $V_{\rm oreg} = 2V_{\rm in} - V_{\rm do} = (1 + R_{f1}/R_{f2})V_{\rm ref}$, where $V_{\rm ref}$ is the reference voltage. Constant $V_{\rm oreg}$ is continuously maintained against variations of input supply voltages and load currents by adjusting $V_{\rm do}$ during the discharging phase of $C_{f2}$. In the next half-clock cycle of $\Phi_2 = 1$, the operating phases of $C_{f1}$ and $C_{f2}$ are swapped and the same $V_{\rm oreg}$ is still maintained by regulating Ml2 through the controller. The above actions repeat in every clock period, so continuous-output regulation is achieved. Since both power transistors Ml2 and Mr2 are regulated alternately corresponding to discharging phases of $C_{f1}$ and $C_{f2}$, respectively, to provide the desired output voltage, the proposed mechanism in fact operates in a pseudo-continuous mode.

### B. Control Characteristics

In applications requiring hundred-milliampere load current, the chip area of the regulated doubler is mainly determined by the number of power transistors used in the power stage. Compared the PCC doubler to the generic open-loop cross-coupled voltage doubler shown in Fig. 2(a), no extra power transistor is needed in the power stage for output regulation. In fact, if an extra power transistor is used, the size of all existing power transistors should be increased in order to maintain the same on resistance for the power efficiency consideration. Both the extra transistor and other enlarged power transistors in the power stage increase the chip area. As a result, the proposed PCC is an area-efficient regulation scheme without using any extra power transistor.

Since the output of the doubler is always continuously regulated by the proposed controller in all clock phases, the load transient response is independent of the operating switching frequency. Instead, load transient response is determined by the loop response of the regulated doubler. Better load transient response can be achieved with faster loop response. In addition, by

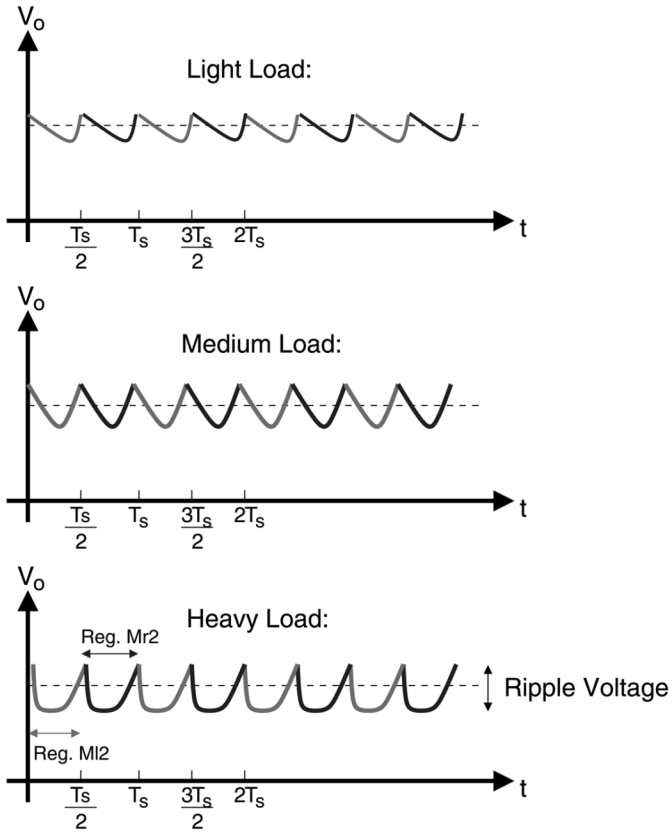


Fig. 4. Ripple voltages of the proposed doubler under different load current conditions.

operating the regulated doubler at a lower switching frequency, the switching power loss can be reduced and hence the regulated doubler achieves high light-load power efficiency.

The output ripple voltage $\Delta V_{\rm o}$ of the doubler is given as

$$\Delta V_o \propto \frac{I_L}{f_s C_L} \tag{1}$$

where $I_L$ is the load current and $f_s$ is the switching frequency. Based on (1), the output ripple of the doubler increases with the load current. If the doubler needs to deliver hundred-milliampere load current, then it has to either operate at high switching frequency or use a large output capacitor in order to reduce the amplitude of the output ripple. However, as mentioned before, the doubler operating at higher switching frequency leads to larger switching power loss, and it is not cost effective to use large-value output capacitor. The proposed PCC, on the other hand, is capable of limiting the maximum output-ripple amplitude. Fig. 4 shows the output ripple of the regulated doubler with PCC under different load-current conditions. Initially, the ripple increases from the light-load to medium-load conditions. When the ripple amplitude reaches the limit defined by the loop-gain magnitude beyond the medium load, the capabilities of continuous output regulation and fast loop response keep the ripple constant with respect to any further increase of the load current. This is due to fact that both upper and lower bounds of the output ripple are fast enough to be maintained at particular values by varying $V_{\rm do}$ across regulation transistors (Ml2 and Mr2) in alternate clock phases. The proposed PCC thus allows the regulated doubler using a small output capacitor to achieve small output ripple at low switching frequency provided that the doubler has large loop-gain magnitude and fast loop response. In fact, large loop-gain magnitude can also improve both line and load regulations of the regulated doubler.

To conclude, the proposed PCC scheme is a cost-effective way to continuously regulate the output without using extra power transistor and requiring only a small output capacitor. Light-load power efficiency can be enhanced by operating the regulated doubler at a lower switching frequency. In addition, good load transient response and output accuracy (output ripple as well as line and load regulations) of the regulated doubler can be achieved if the implementation of the controller provides fast loop response and large loop-gain magnitude.

### C. Implementation Considerations

In order to increase the loop-gain magnitude of the regulated doubler, the PCC controller is implemented using a three-stage amplifier as shown in Fig. 5(a), which consists a differential input stage $\rm A_1$, a positive gain second stage $\rm A_2$, and the common-source configuration of power transistors Ml2 (Mr2) during the capacitor discharging phase of $C_{f1}(C_{f2})$. Switches S1-S4 driven by two-phase non-overlapping clock signals are used to synchronize both operations of the controller and flying capacitors $C_{f1}$ and $C_{f2}$ in the power stage such that one of power transistors Ml2 and Mr2 is regulated during the capacitor discharging phase. However, the use of serial complementary switches S2 and S4 is known to have turn-on problems in low-voltage condition [10]. The discontinuous-output regulation results from this implementation if $V_{\rm in} < (|V_{\rm thp}| + V_{\rm thn})$, where $|V_{\rm thp}|$ and $V_{\rm thn}$ are threshold voltages of pMOS and nMOS transistors, respectively. Fig. 5(b) shows that when $V_{\rm in} = 1.5$ V and $|\,{\rm V_{thp}}| = {\rm V_{thn}} = 0.88$ V, both pMOS and nMOS transistors in the complementary switch are off ranging from 0.62 V to 0.88 V. The controller loses the regulation capability in this range.

Fig. 6 shows the proposed three-stage switchable opamp to implement the PCC scheme. Large loop-gain magnitude is achieved by using gain stages $\rm A_1$, $\rm A_{L2}$ ($\rm A_{R2}$) and $\rm A_{L3}$ ($\rm A_{R3}$). Instead of using serial complementary switches, both second gain stages $\rm A_{L2}$ and $\rm A_{R2}$ are switchable to regulate the output or turn off alternately in every half-clock period for saving the static current dissipation in the controller and providing continuous regulation capability at low voltage. In addition, the time-multiplexed enhanced active-feedback frequency compensation (AFFC) is developed to stabilize the regulated doubler. The details of stability of the regulated doubler using the proposed time-multiplexed enhanced AFFC under different load-current conditions will be discussed in the following section. From Fig. 6, the enhanced AFFC structure consists of a damping-factor-control block [11], [12] and time-multiplexed active-capacitive feedback networks. Two compensation capacitors $C_{\rm al}$ and $C_{\rm ar}$, with the positive gain stage $\rm A_a$, establish an active-capacitive feedback network [12]–[14] in every alternate half-clock period. The damping-factor-control

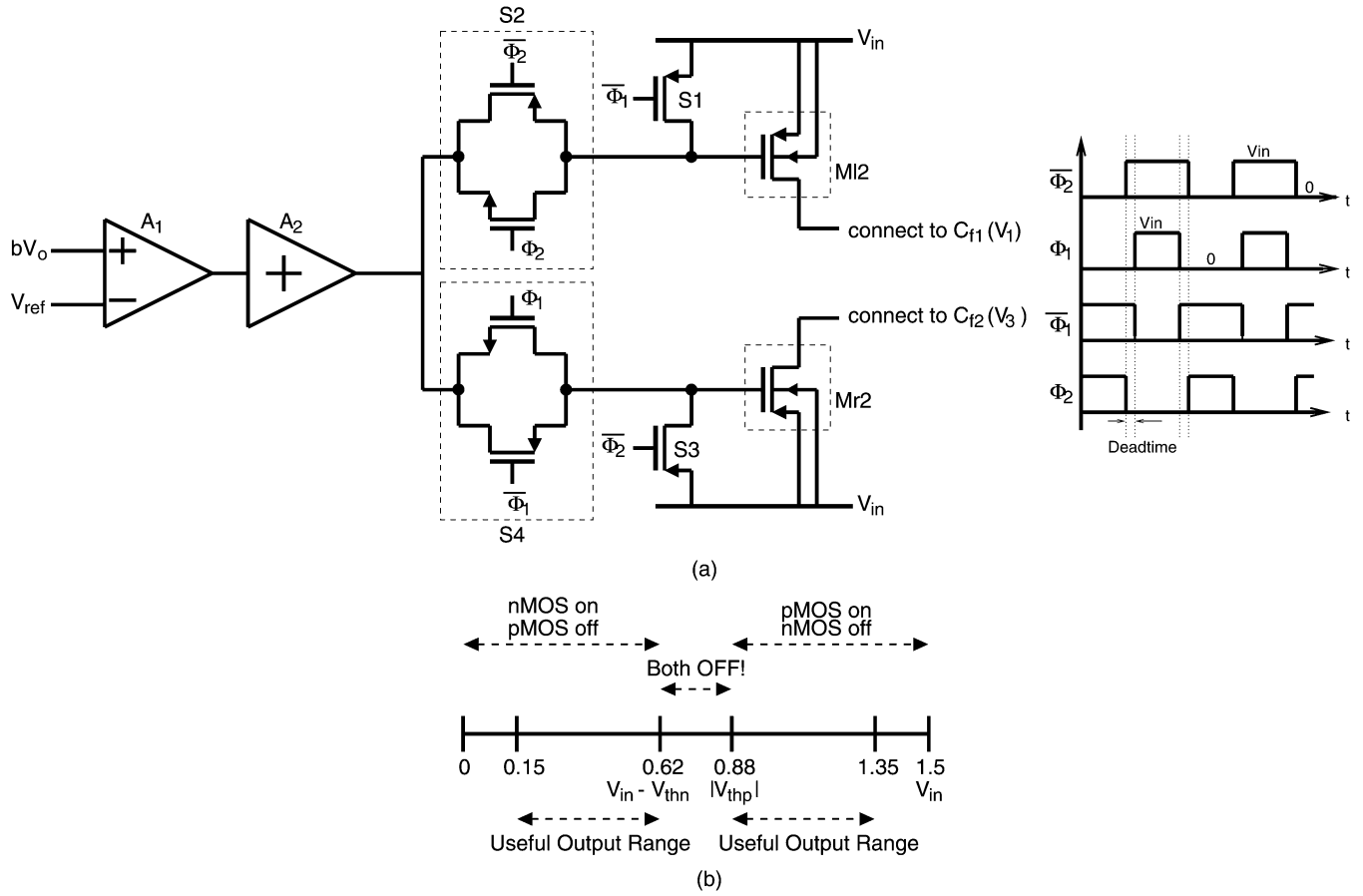


Fig. 5. (a) Structure of the pseudo-continuous output regulation using a three-stage amplifier with serial switches and (b) serial switch problem in low-voltage condition.

(DFC) block is located at the output of the first gain stage in order to eliminate the use of Miller capacitor. The enhanced AFFC structure is used to enhance the loop-gain bandwidth in low-power condition. The time-multiplexed dynamic feed-forward stage generates extra dynamic current to the output of either second gain stages $\mathrm{A}_{L2}$ or $\mathrm{A}_{R2}$, according to clock signals $\Phi_1$ and $\Phi_2$ in order to realize a push-pull effect at the gates of power transistors Ml2 and Mr2. The push-pull effect relaxes the slew-rate limitation of driving power transistors Ml2 and Mr2 in low-power condition and allows both Ml2 and Mr2 to be turned on and off much faster during switching. By both widening the loop-gain bandwidth and relaxing slew rate limitation of driving power transistors, the loop response and hence the load-transient response is improved.

## III. Stability Analysis

Since the proposed structure shown in Fig. 6 achieves continuous output regulation during every discharging phase of flying capacitors $C_{f1}$ and $C_{f2}$, the stability of the regulated doubler is analyzed in s-domain using loop-gain transfer functions L(s). In particular, Fig. 7 is an equivalent structure of Fig. 6 for analyzing the stability of the regulated doubler, in which $C_a = C_{\mathrm{al}} = C_{\mathrm{ar}}$ is the compensation capacitor for the active-capacitive feedback network, $\mathrm{A}_p$ is the gain of power transistors Ml2, Mr2, and $|\mathrm{A}_2| = |\mathrm{A}_{L2}| = |\mathrm{A}_{R2}|$. In the figure, $\mathrm{g}_{\mathrm{mi}}$, $R_i$ and $C_i$ are defined as transconductance, output resistance and lumped output parasitic capacitance of the $i$th gain stage, respectively. In addition, $C_f$ and $C_L$ are the flying capacitor and output capacitor, while $R_{\mathrm{op}}$, $R_s$, $R_L$, and $R_{\mathrm{esr}}$ are the output resistance of the power transistor, on-resistance of power switch Sl4 or Sr4, the load resistance, and the equivalent series resistance of $C_L$, respectively. The loop-gain transfer function is derived based on the following conditions.

1) The flying capacitor $C_f$, output capacitor $C_L$, gate capacitance of the power transistor $C_2$ and compensation capacitors ($C_{\mathrm{a}}$ and $C_{\mathrm{b}}$) are much larger than $C_1$ and $C_4$.
2) Transconductance $\mathrm{g}_{\mathrm{mp}}$ and output resistance $R_{\mathrm{op}}$ of the power pMOS as well as the gain of the last stage $\mathrm{A}_p = \mathrm{g}_{\mathrm{mp}} R_{\mathrm{op}}$ vary with the change of the load current. In particular, $\mathrm{g}_{\mathrm{mp}}(R_{\mathrm{op}})$ decreases (increases) with the load current. In addition, $\mathrm{A}_p = \mathrm{g}_{\mathrm{mp}} R_{\mathrm{op}}$ is inversely proportional to $\sqrt{I_L}$.
3) For simplicity, both compensation capacitors are set to equal to each other (i.e., $C_{\mathrm{a}} = C_{\mathrm{b}}$).

Based on the above conditions, the loop-gain transfer function of the proposed regulated doubler is given as

$$L(s) = \frac{bV_{\mathrm{oreg}}}{V_{\mathrm{in}}} = \frac{-L_o\left(1+\frac{s}{z_{\mathrm{esr}}}\right)\left(1+\frac{s}{z_b}\right)}{1+as+bs^2+cs^3} \qquad (2)$$

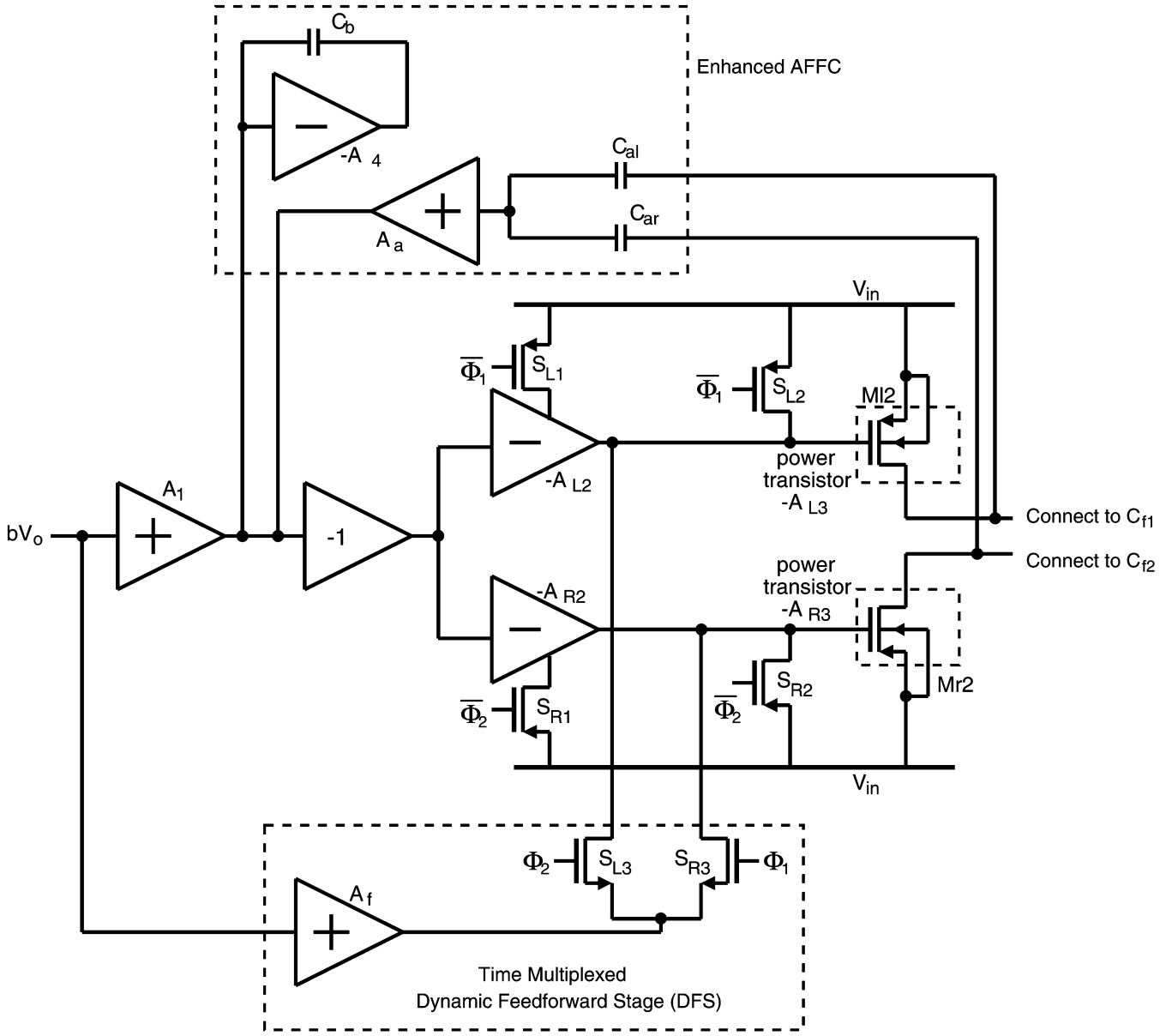


Fig. 6. Proposed three-stage switchable opamp for pseudo-continuous output regulation.

where

$$L_o = \frac{R_{f2}}{R_{f1}+R_{f2}} g_{m1}g_{m2}g_{\rm mp}R_1R_2R_{\rm op} \tag{3}$$

$$z_{\rm esr} = \frac{1}{C_L R_{\rm esr}} \tag{4}$$

$$z_b = \frac{1}{\left(1+\frac{g_{\rm mf}g_{m4}}{g_{m1}g_{m2}}\right)C_bR_4} \tag{5}$$

$$a = (C_L//C_f)R_{\rm op} + g_{m2}g_{\rm mp}C_aR_1R_2R_{\rm op} \tag{6}$$

$$b = g_{m4}C_b(C_L//C_f)R_1R_2R_{\rm op} \tag{7}$$

$$c = g_{m4}C_2C_b(C_L//C_f)R_1R_2R_4R_{\rm op}. \tag{8}$$

From (2), the loop gain is negative due to negative feedback established by the proposed PCC controller for output voltage regulation. There exist two left-half-plane zeros $z_{\rm esr}$ and $z_{\rm b}$ in (2), which provides positive phase shift to the system for better stability. In addition, the third-order polynomial in (2) implies that three poles are created. According to (6)–(8), locations of poles depend on the different load currents due to the existence of $R_{\rm op}$ and $g_{\rm mp}$. As a result, the stability of the proposed regulated doubler is studied for two conditions: $I_L = 0$ and $I_L > 0$.

When $I_L = 0$, it is the worst case stability of the proposed regulated doubler. In this situation, the current drain from the power transistor is $V_{\rm oreg}/(R_{f1}+R_{f2})$, which is around 3–7 $\mu$A for low-power design. Hence, $g_{\rm mp}$ and $R_{\rm op}$ are at the minimum and maximum, respectively. These values cause $(C_L//C_f)R_{\rm op} \gg g_{\rm m2}g_{\rm mp}C_{\rm a}R_1R_2R_{\rm op}$ in (6). As a result, (2) can be approximated to

$$L(s)|_{I_L=0} \approx \frac{-L_o\left(1+\frac{s}{z_{\rm esr}}\right)\left(1+\frac{s}{z_b}\right)}{\left(1+\frac{s}{p_{10}}\right)(1+sg_{m4}C_bR_1R_2+s^2g_{m4}C_2C_bR_1R_2R_4)} \tag{9}$$

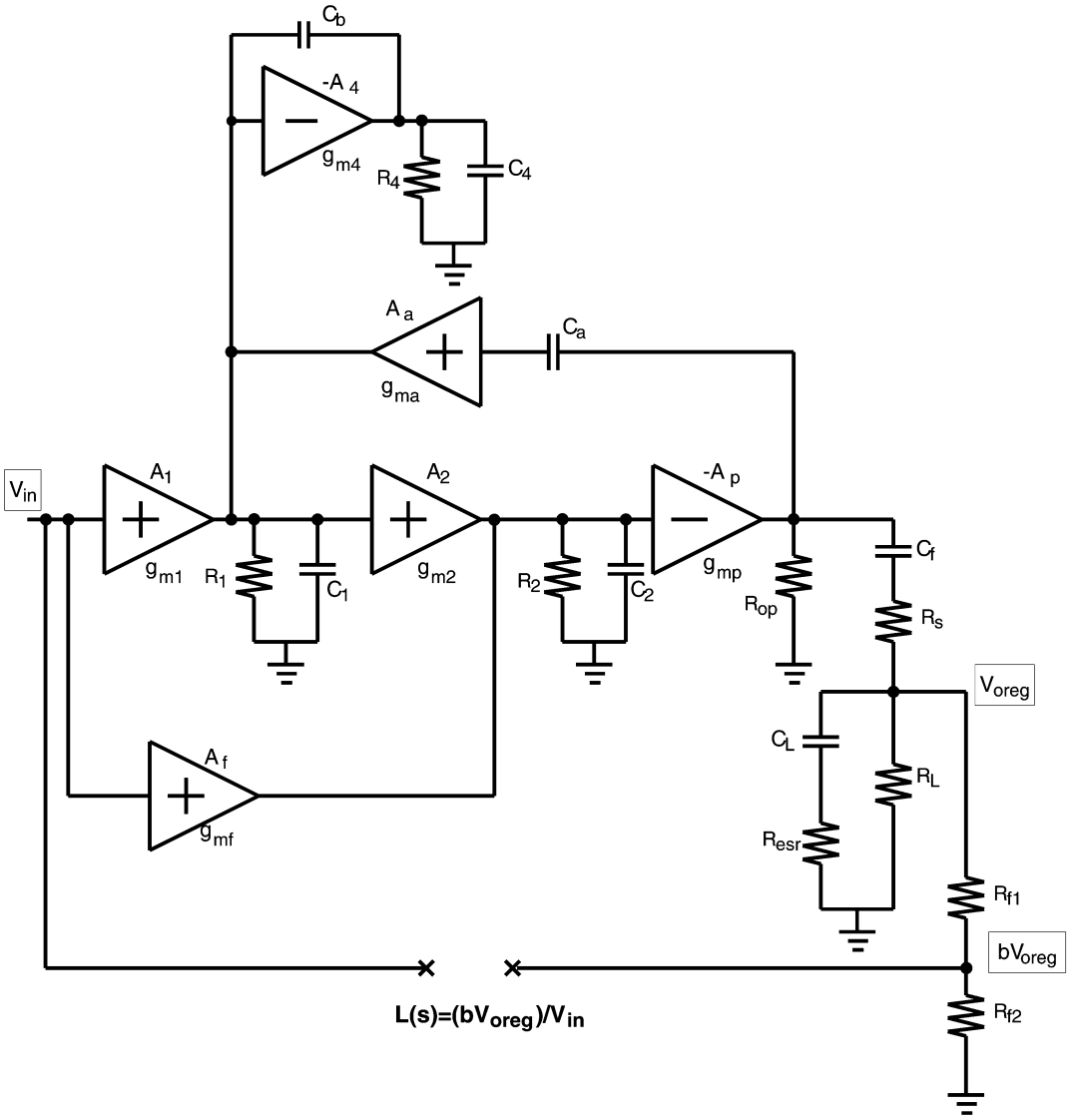


Fig. 7. Structure of the proposed regulated SC doubler for loop-gain analysis.

where $p_{10} = 1/[(C_L//C_f)R_{\rm op}]$. As the discriminant of the second-order polynomial in (9) is smaller than zero, a pair of complex poles exists in the system. When the second-order polynomial is compared with a standard second-order function as

$$F(s) = 1 + s\left(\frac{1}{Qp_c}\right) + s^2\left(\frac{1}{p_c^2}\right) \tag{10}$$

where $Q$ and $p_c$ are the $Q$-factor and the frequency of the complex poles, respectively. The values of $p_c$ and $Q$ are given by

$$p_c = \frac{1}{\sqrt{g_{m4}C_2C_bR_1R_2R_4}} \tag{11}$$

$$Q = \sqrt{\frac{C_2R_4}{g_{m4}C_bR_1R_2}}. \tag{12}$$

Fig. 8 shows a magnitude plot of L(s) under no-load condition. From the figure, $Q$, $p_c$ and $z_{\rm esr}$ are critical to the stability of the regulated doubler, as $p_c$ is at a lower frequency than other left-half-plane zeros. If the $Q$-value is too large, a magnitude peak occurs, which can degrade the stability due to the decrease in both phase margin and gain margin. In this design, the $Q$-value is set to $1/\sqrt{2}$ under the condition that

$$C_b = \frac{2C_2R_4}{g_{m4}R_1R_2}. \tag{13}$$

In addition, in order to provide around 60° phase margin to the system, $z_{\rm esr}$ is set as $z_{\rm esr} = 2p_c = 4(L_{\rm o} \times p_{10})$ with the following conditions:

$$p_c = \frac{1}{\sqrt{2}C_2R_4} = 2L_o\frac{1}{(C_L//C_f)R_{\rm op}}$$

$$\Rightarrow L_o = \frac{(C_L//C_f)\,R_{\rm op}}{2\sqrt{2}C_2R_4} \tag{14}$$

$$z_{\rm esr} = \frac{1}{C_LR_{\rm esr}} = 2\frac{1}{\sqrt{2}C_2R_4} \Rightarrow R_{\rm esr} = \frac{C_2R_4}{\sqrt{2}C_L}. \tag{15}$$

Based on (13)–(15), the output resistance of DFC block $R_4$ can be reduced in order to decreases compensation capacitors for better area efficiency, increases DC loop-gain magnitude $L_{\rm o}$ for

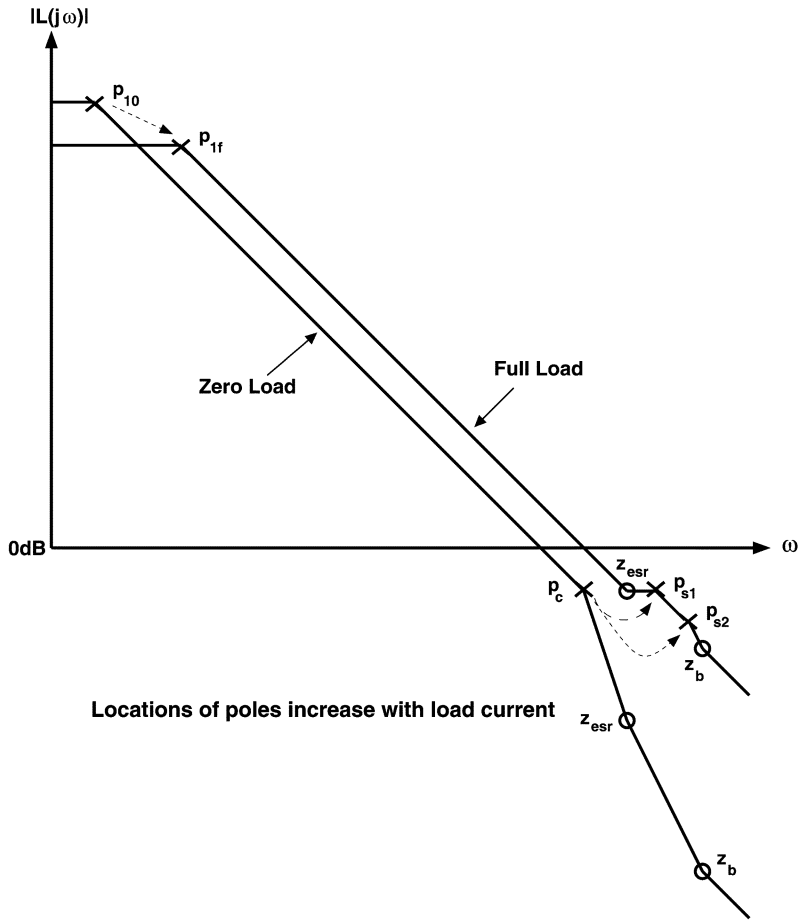


Fig. 8. Loop gain (magnitude plot only and not in scale) of the proposed SC regulated doubler under different load-current conditions.

better output accuracy, and reduces $R_{\rm esr}$ for better load transient response.

When there is an increase in the load current, $g_{\rm mp}$ becomes larger. Hence, a $\approx g_{\rm m2}g_{\rm mp}C_{\rm a}R_1R_2R_{\rm op}$ in (6), and (2) is approximated to

$$L(s) \approx \frac{-L_o\left(1+\frac{s}{z_{\rm esr}}\right)\left(1+\frac{s}{z_b}\right)}{\left(1+\frac{s}{p_{1f}}\right)\left[1+s\frac{g_{m4}(C_L//C_f)}{g_{m2}g_{\rm mp}}+s^2\frac{g_{m4}C_2(C_L//C_f)R_4}{g_{m2}g_{\rm mp}}\right]} \approx \frac{-L_o\left(1+\frac{s}{z_{\rm esr}}\right)\left(1+\frac{s}{z_b}\right)}{\left(1+\frac{s}{p_{1f}}\right)\left(1+\frac{s}{p_{s1}}\right)\left(1+\frac{s}{p_{s2}}\right)} \quad (16)$$

where

$$p_{1f} = \frac{1}{g_{m2}g_{\rm mp}C_aR_1R_2R_{\rm op}} \quad (17)$$

$$p_{s1} = \frac{g_{m2}g_{\rm mp}}{g_{m4}(C_L//C_f)} \quad (18)$$

$$p_{s2} = \frac{1}{C_2R_4}. \quad (19)$$

The presence of two separate non-dominant poles is due to the discriminant of the second-order polynomial in (16) larger than zero. In order to ensure stability when $I_L$ is little larger than zero, the condition of $p_{s1} = p_c$ should be satisfied, which gives rise to

$$g_{m4} = \frac{\sqrt{2}g_{m2}g_{\rm mp}C_2R_4}{C_L//C_f}. \quad (20)$$

It should be noted that $g_{\rm m4} \propto g_{\rm mp}$ is only true during small $I_L$, so the value of $g_{\rm m4}$ is not necessarily imply large static current dissipation. Since the negative phase shift caused by $p_{s1}$ is smaller than that caused by $p_c$, the phase margin of L(s) increases compared to that in the case of $I_L = 0$. When the load current further increases, $p_{s1}$ is moved to even higher frequencies as its location depends on $g_{\rm mp}$ according to (18). Therefore, the stability of the regulated doubler improves with the load current. The improvement of the stability is also shown in Fig. 8 when the complex non-dominant poles $p_c$ during $I_L = 0$ is pushed to higher frequencies and become separate poles under full-load condition.

## IV. Circuit Implementations

### A. System Integration

Fig. 9 shows the schematic of the proposed regulated voltage doubler [15]. The power stage is an improved transistor-level implementation of the cross-coupled voltage doubler. There are

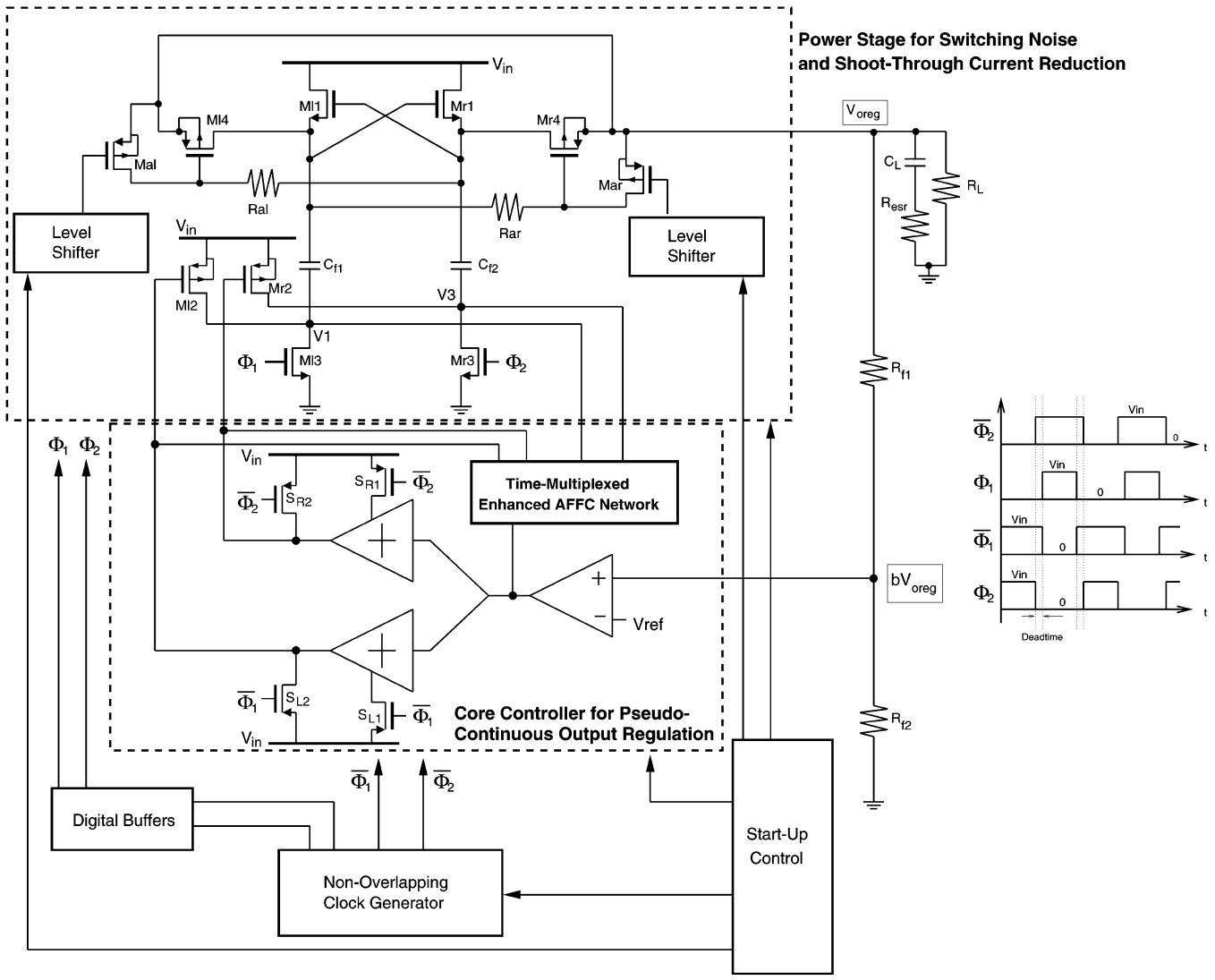


Fig. 9. Schematic of the proposed regulated SC voltage doubler.

eight power transistors Ml1-Ml4, Mr1-Mr4 and two off-chip flying capacitors $C_{f1}$, $C_{f2}$, which form the conventional cross-coupled voltage doubler shown in Fig. 2 for voltage conversion. Additional transistors Mal, Mar and resistors Ral, Rar realize both break-before-make mechanism and gate-slope-reduction technique to reduce shoot-through current and switching noise, respectively [9]. By reducing the shoot-through current in the power stage, the light-load power efficiency of the regulated doubler can be improved.

In the proposed regulated doubler, proper start-up procedure is important to avoid turning on the body diode of both power transistors Ml4 and Mr4, as their substrates are tied to the output. The start-up control block in Fig. 9 mainly consists of a start-up transistor connected between the input and the output, and a start-up comparator. During the initial start-up, all circuits including clock generator, controller, level shifters and all power transistors are turned off by the start-up block, while the output is charged by the start-up transistor until the output voltage reaching $0.8V_{\rm in}$. When the start-up comparator detects this threshold, all circuits of the doubler are turned on and the start-up transistor is turned off. The doubler then begins to operate in the constant switching-frequency mode.

### *B. Three-Stage Switchable Opamp Design*

Fig. 10 shows the circuit of the three-stage switchable opamp. In the amplifier, the input gain stage is realized by transistors M11–M15 and Ma. Transistor Ma and compensation capacitors $C_{\rm al}$, $C_{\rm ar}$ implement an active-capacitive-feedback network in alternate half-clock period. Transistors Md1, Md2, and the compensation capacitor $C_{\rm b}$ realize the damping-factor-control (DFC) stage. The diode-connected Md2 reduces the value of output resistance of the DFC stage, which is helpful for the loop stability as discussed in Section III. The unity-gain inverter is implemented by transistors Mu1 and Mu2 for sign inversion. To ensure fast switching of the push-pull stage for driving the power transistors Ml2 and Mr2, the switchable second gain stages formed by M21 and M22 are controlled to turn on and off alternatively using the differential switches Ms1 and Ms2 with a pair of complementary clock phases ($\overline{\Phi_1}$ and $\overline{\Phi_2}$) [16].

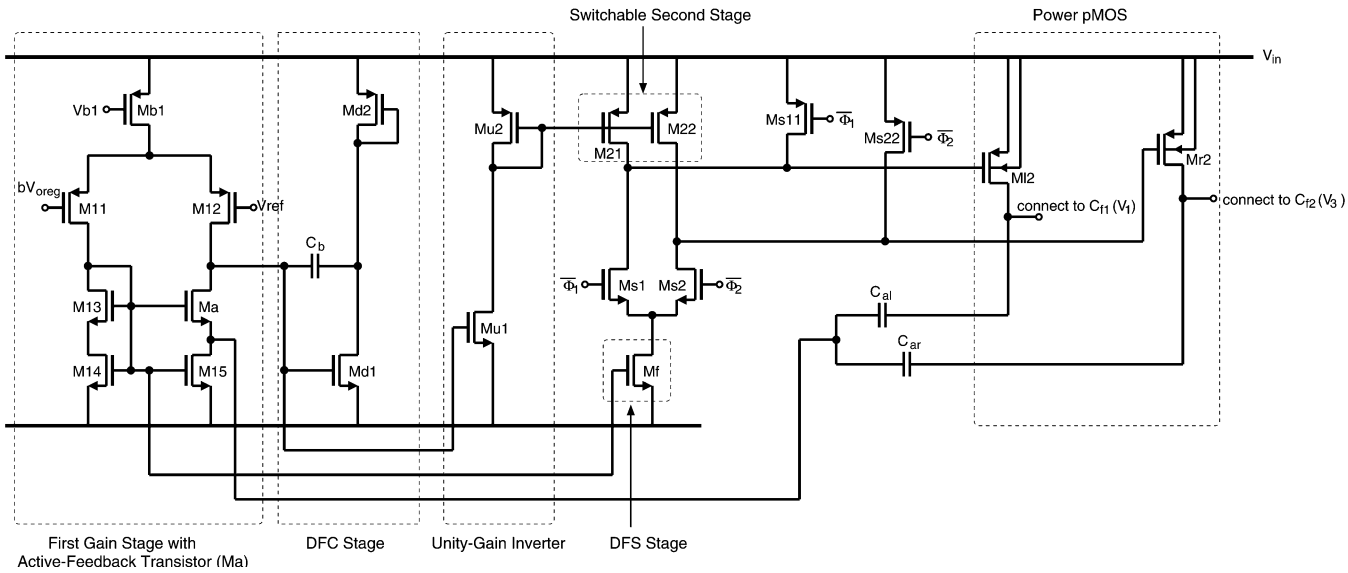


Fig. 10. Circuit implementation of the three-stage switchable opamp with time-multiplexed enhanced AFFC.

This is due to reasons that the bias current provided by the dynamic feedforward stage Mf is always kept active and differential switches (Ms1, Ms11) and (Ms2, Ms22) provide low output impedance at the turn-on instance and thus dramatically reduce the *RC* delay at the gate of the power transistor. In addition, switch Ms11 (Ms22) is used to turn off power transistor Ml2 (Mr2) by providing dynamic current to charge the gate capacitance of Ml2 (Mr2) to $V_{\rm in}$ during $C_{f1}(C_{f2})$ changing from discharging phase to charging phase.

## V. Experimental Results and Discussions

The regulated doubler with the proposed pseudo-continuous control using a three-stage switchable opamp has been implemented in AMS 0.6-$\mu$m CMOS n-well process. Fig. 11 shows the micrograph of the proposed regulated doubler and its chip area including all testing pads is 2.32 mm $\times$ 2.36 mm. In particular, the proposed switchable opamp only occupies less than 10% of the total chip area, and $C_{\rm al} = C_{\rm ar} = 12{\rm pF}$ and $C_{\rm b} = 8$ pF are located within the switchable opamp to implement the time-multiplexed advanced AFFC scheme.

The regulated doubler can operate with the input supply voltage from 1.5 V to 3.2 V and the switching frequency ranging from 200 kHz to 500 kHz to deliver at a maximum of 150 mA load current. Table I summarizes the detailed performance of the proposed regulated doubler.

Figs. 12(a) and (b) show that DC output voltage of the SC doubler is accurately regulated at 3.3 V under different input voltages and switching frequencies by the proposed PCC scheme during zero load. These results verify that the worst-case stability is established by the proposed time-multiplexed enhanced AFFC scheme. Figs. 13(a) and (b) give the measured AC-coupled output voltage under no-load condition. Small output glitch of 3 mV is obtained at different switching frequencies of 200 kHz and 500 kHz.

Figs. 14(a)–(c) show the measured output ripple voltages under different loading conditions. The ripple amplitude increases from 10 mV to 20 mV when $I_L$ initially increases

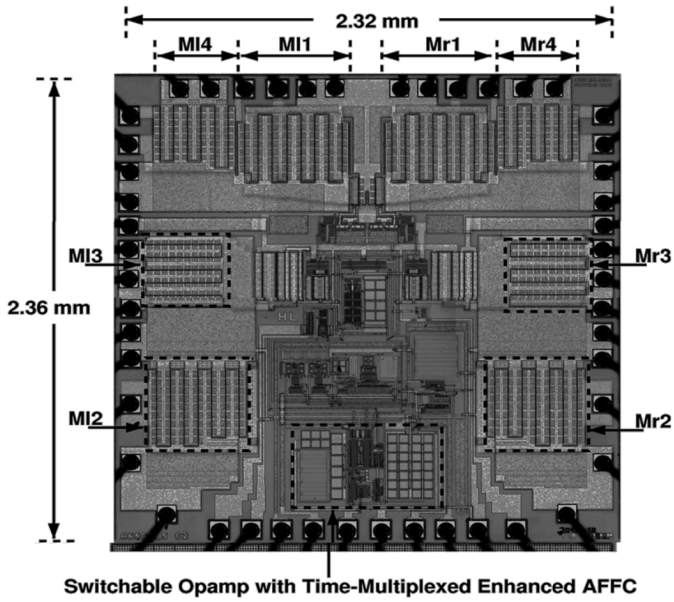


Fig. 11. Micrograph of the proposed regulated voltage doubler.

from 10 mA to 50 mA and then the ripple amplitude is kept constant at 20 mV for any further increase of $I_L$. This justifies that continuous output regulation and fast loop response are achieved. Small ripple of $\leq 20$ mV is obtained by the proposed control scheme and its implementation, even when the regulated doubler operates at a low switching frequency of 200 kHz, uses a small output capacitor of 2.2 $\mu$F and is capable of delivering 150 mA load current.

Fig. 15(a) shows the measured power efficiency of the proposed regulated doubler under different load currents. The power efficiency of the regulated doubler is lower at light loads and increases with the load current, as the percentage of the switching power loss in the total input power decreases when the load current increases. The maximum power efficiency of 90% is achieved at both switching frequencies of 200 kHz and

TABLE I
PERFORMANCE SUMMARY OF MEASUREMENT RESULTS

| | |
|---|---|
| Technology | AMS 0.6-μm CMOS |
| Flying Capacitor ($C_{f1}$, $C_{f2}$) | 1μF (off-chip) |
| Output Capacitor ($C_L$) | 2.2μF (off-chip) |
| Supply Voltage Range ($V_{in}$) | 1.5V - 3.2V |
| Regulated Output Voltage ($V_{oreg}$) | 2.7V ($V_{in}$ = 1.5V – 1.7V)<br>3.3V ($V_{in}$ = 1.8V – 3.2V) |
| Switching Frequency Range ($f_s$) | 200kHz – 500kHz |
| load current Range ($I_L$) | ≤150mA |
| Output Ripple Voltage | ~20mV |
| Output Recovery Time | ~25μs ($I_L$ step of 100mA) |
| Line Regulation | 0.27%/V ($V_{in}$ = 1.8V – 3.2V) |
| Load Regulation @ $V_{in}$ = 1.8V | 0.005%/mA ($I_L$ = 0 – 150mA) |
| Power Efficiency<br>@ $V_{in}$ =1.8V and $f_s$ = 200kHz | Max. 90%<br>≥87% ($I_L$ = 5mA – 150mA) |
| No-Load Input Current | 180μA ($f_s$ = 200kHz) |
| Glitch @ No-Load Condition | ~3mV |

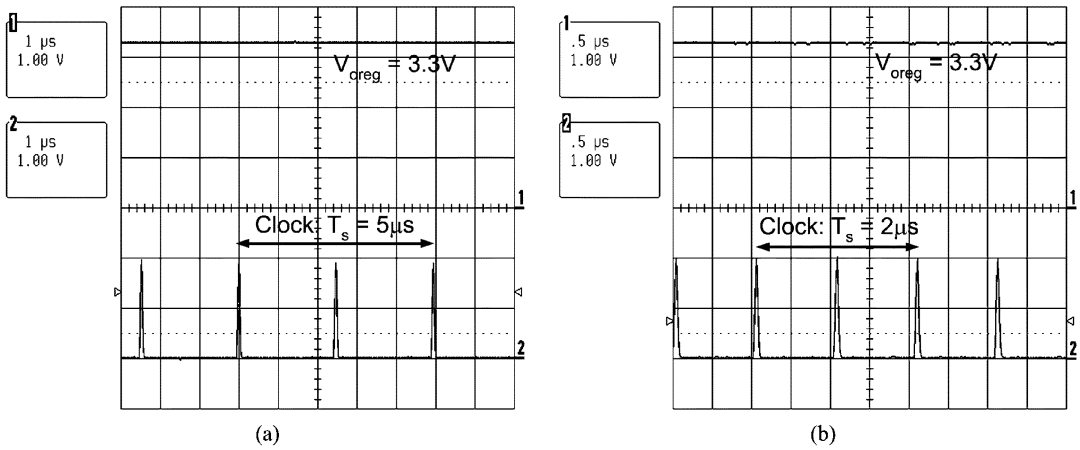


Fig. 12. Measured output voltages at (a) $V_{\rm in} = 1.8$ V and $f_s = 200$ kHz, and (b) $V_{\rm in} = 2$ V and $f_s = 500$ kHz under zero-load condition.

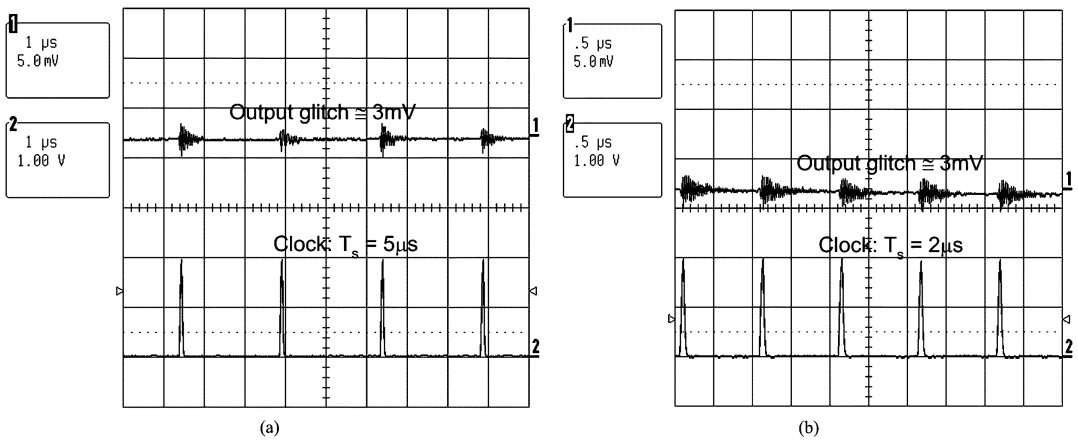


Fig. 13. Measured AC-coupled output glitch under no-load condition with (a) $f_s = 200$ kHz and (b) $f_s = 500$ kHz.

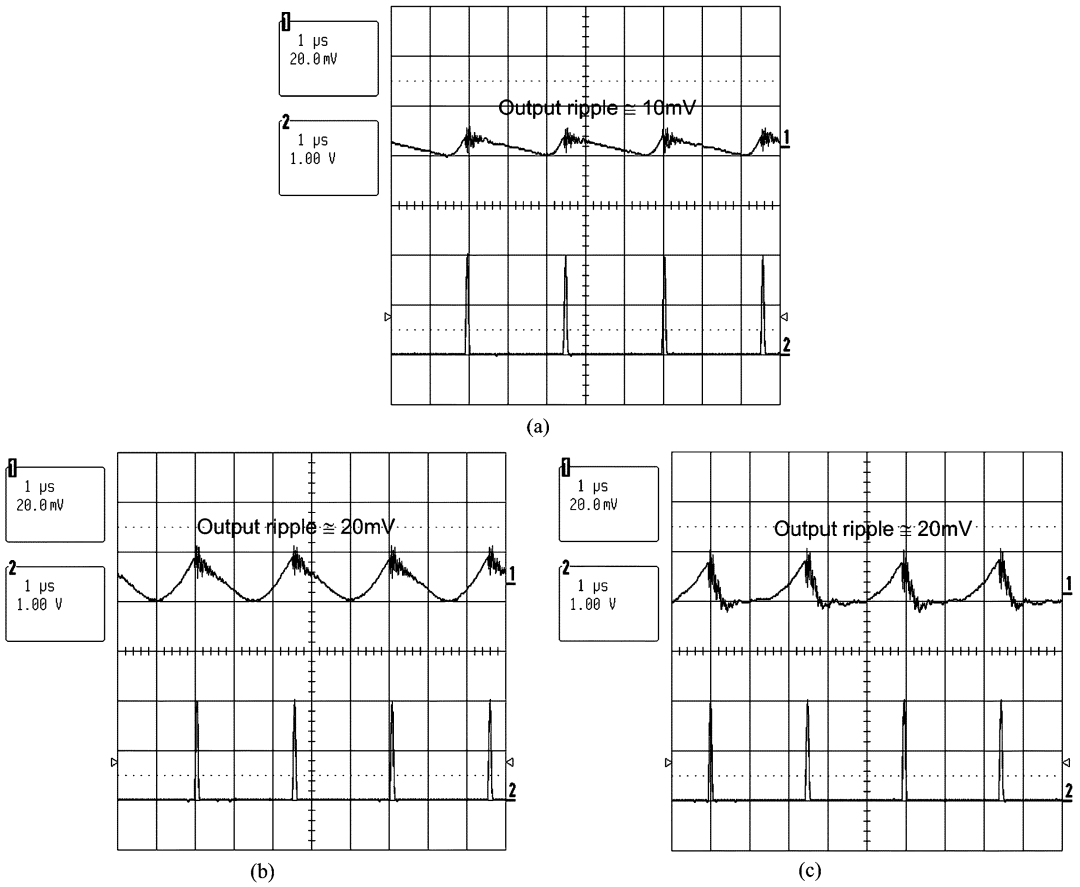


Fig. 14. Measured output ripples at $f_s = 200$ kHz with (a) $I_L = 10$ mA, (b) $I_L = 50$ mA, and (c) $I_L = 150$ mA.

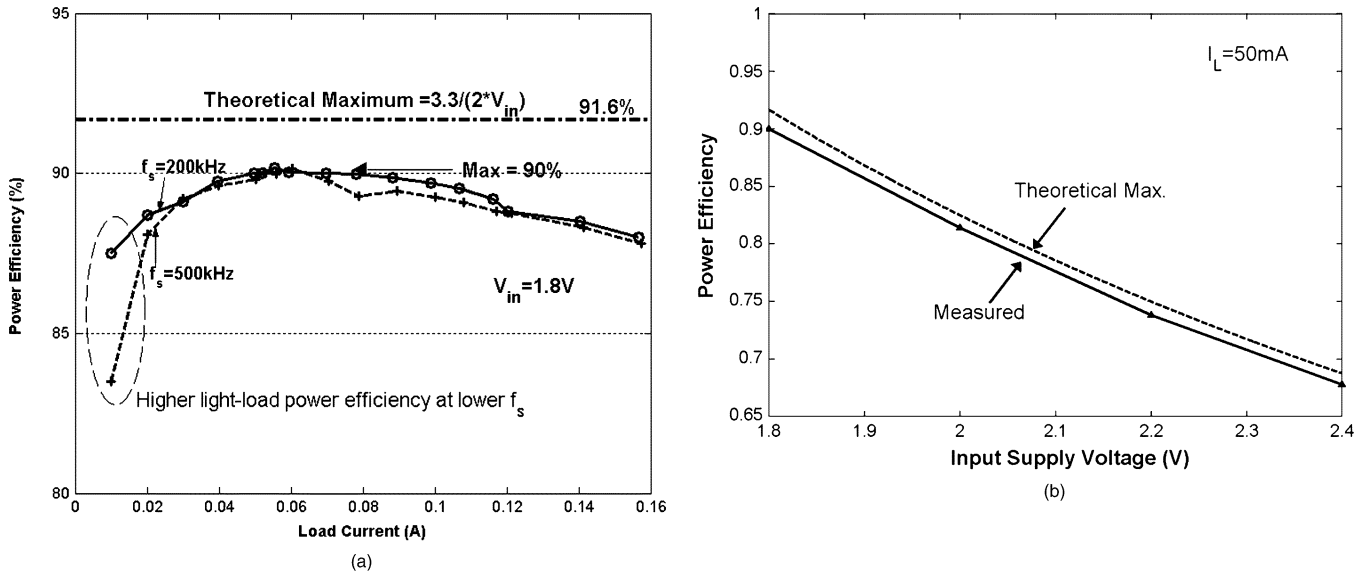


Fig. 15. Measured power efficiency of the proposed regulated voltage doubler under (a) different load currents and (b) different input supply voltages.

500 kHz with the theoretical maximum efficiency of 91.6%. Since the power efficiency of a regulated SC voltage doubler is related to the regulated output voltage and input voltage ($V_{\rm in}$) as $< V_{\rm oreg}/2V_{\rm in}$ [4], [17], the theoretical maximum efficiency is then associated with the minimum dropout voltage ($V_{\rm do,min}$) across the regulated power transistor and is defined as $V_{\rm oreg}/2V_{\rm in} = (2V_{\rm in} - V_{\rm do,min})/2V_{\rm in}$. Since $V_{\rm do,min}$ equals to 0.3 V in our design, the maximum achievable efficiency of the proposed regulated doubler is 91.6% when $V_{\rm in} = 1.8$ V. In addition, Fig. 15(a) shows that the power efficiency of the regulated doubler is 87% when $I_L = 5$ mA and $f_s = 200$ kHz, which has 3.5% increase as compared to the efficiency of the

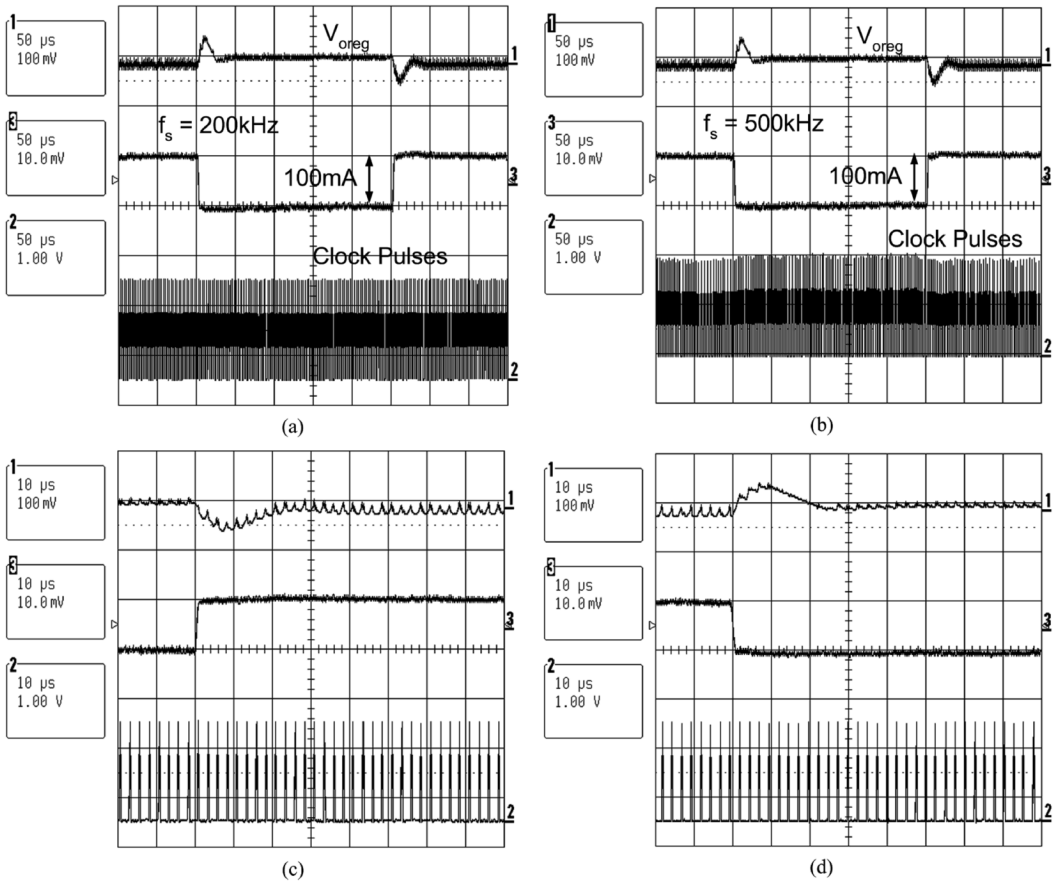


Fig. 16. Measured load transient for a 100 mA load step with rise and fall time of 1 $\mu$s at (a) $f_s = 200$ kHz, (b) $f_s = 500$ kHz, and close view of load transient response at $f_s = 200$ kHz when load changes, (c) from 10 mA to 110 mA and (d) from 110 mA to 10 mA.

doubler operating at a higher $f_s$ of 500 kHz. The improvement of the light-load power efficiency is mainly due to the reduction in the switching power loss by operating the regulated doubler at lower switching frequency. Moreover, the measured power efficiency is always about 1% less than the theoretical maximum efficiency under different input supply voltages as shown in Fig. 15(b).

Figs. 16(a)–(d) show the measured load transient response of the regulated voltage doubler. The transient recovery time is defined as the time required for the output voltage settles to the final value to within 5% of the step size. With the load-current step of 100 mA and the rise and fall time of 1 $\mu$s, the transient recovery time of the output voltage is within 25 $\mu$s with the overshoots and undershoots of 50 mV. Figs. 16(a) and (b) also show that the load transient response is the same for both $f_s = 200$ kHz and 500 kHz, which indicate that load transient response is independent of the switching frequency. These results further justify that the continuous output regulation is achieved by using the proposed PCC scheme. The proposed PCC with three-stage switchable opamp allows the regulated voltage doubler to obtain fast output transient recovery time even the regulated doubler operating at low switching frequency. Since lower switching frequencies correspond to lower switching power loss in the light-load condition, both load transient response and light-load power efficiency of the regulated doubler are optimized simultaneously by using the proposed pseudo-continuous control with three-stage switchable opamp and time-multiplexed enhanced AFFC.

## VI. Conclusion

This paper has presented a pseudo-continuous control (PCC) scheme using a three-stage switchable opamp for the cross-coupled voltage doubler capable of delivering 150 mA load current in portable applications. The PCC does not require use extra power transistor to continuously regulate the output voltage, thereby saving chip area. With continuous output regulation, the doubler not only can be operated at lower switching frequency for reducing its switching power loss, but also has smaller output ripple even when a small output capacitor is used. The three-stage switchable opamp improves the DC loop-gain magnitude for better line and load regulations, while time-multiplexed enhanced AFFC scheme ensures stability and enhances the speed of the loop response of the regulated doubler. Experimental results verify that the PCC scheme with its implementation using three-stage switchable opamp and time-multiplexed enhanced AFFC scheme allows the regulated doubler to simultaneously achieve high light-load power efficiency, low cost in terms of using small output capacitor and chip area, high output-voltage accuracy and fast load transient response.

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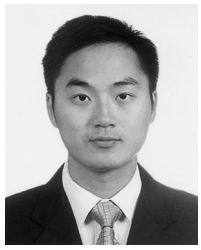

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