An Infinite Phase Shift Delay-Locked Loop With Voltage-Controlled Sawtooth Delay Line

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***Abstract*—A wide-range delay-locked loop (DLL) with infinite phase shift and digital-controlled duty cycle is presented. By changing the polarity of the input clock of the voltage-controlled sawtooth delay, this proposed DLL achieves infinite phase shift by only a single loop. The proposed DLL has been fabricated in a 0.18 μm CMOS process and the core area is 0.45 $\times$ 0.3 mm^2. The measurement results show the proposed DLL operates from 50 to 500 MHz. The duty cycle of the output clock can be adjusted from 30% to 60% in the step of 5%. At 500 MHz, the measured rms jitter and peak-to-peak jitter is 1.43 and 11.1 ps, respectively. Its power consumption is 6 mW for a supply of 1.5 V.**

***Index Terms*—Clock synchronization, delay-locked loop (DLL), dual-loop DLL, duty cycle, infinite phase shift, jitter.**

I. Introduction

FOR the high performance microprocessors and memory ICs, the phase-locked loops (PLLs) and delay-locked loops (DLLs) are usually adopted to reduce the skews and jitters of the clock signals. If the multiplied clock is not required, the DLL [1] is usually chosen for its unconditional stability and better jitter performance. To make the DLL immune to harmonic or false locking, the conventional voltage-controlled delay line (VCDL) must have the initial delay between $0.5T_{\rm REF}$ and $1.5T_{\rm REF}$ [2], where $T_{\rm REF}$ is the reference clock period. Therefore, there are several disadvantages in a conventional DLL. First, due to the process, voltage, and temperature (PVT) variations, the initial delay constraint of the VCDL may limit the operation range of a DLL. Second, it is difficult to guarantee the initial delay constrain if a wide operation frequency range is needed. Third, the VCDL may distort the duty cycle of the clock, owing to the unbalanced rising and falling times. It is unsuitable for the applications, which require the precise duty cycle of the clock.

To overcome the above problems, several solutions have been proposed, such as the replica delay line [2], a start-up control circuit [3], the dual-loop approach [4]–[8], and the phase mixing technique [9]. In [2], an additional replica delay line is needed. Once the mismatch exists between the replica and the main delay lines, the operation range will be limited. In [3], a start-up control circuit and a stage selector are used. However, many DFFs are needed in a stage selector, which occupy large chip area. The dual-loop DLL [4]–[8] can generate the fine phase shift by the phase interpolator [4]. However, the dual-loop DLL may have the large output jitter and active area. To extend the operation range, the quadrature phase mixing technique is adopted in [9]. The wide phase shift is achieved, but the phase discontinuity may occur at the quadrant boundaries. To correct the duty cycle distortion of the clock caused by the VCDL and PVT variations, the pulsewidth control loop (PWCL) [10], [11] or the duty-cycle corrector [2], [12], [13] are usually used in the DLL.

In this paper, a wide range DLL with infinite phase shift by using the voltage-controlled sawtooth delay line (VCSDL) is presented. Compared with the dual-loop DLLs [4]–[8], the proposed DLL achieves infinite phase shift by using only a single loop. Therefore, the output jitter and chip area are reduced. Meanwhile, the duty cycle of the output signal is controlled to overcome the distortion, which is affected by the VCDL and PVT variations.

This paper is organized as follows. In Section II, the circuit description is given. Section III shows the experimental results. Section IV gives the conclusions.

II. Circuit Description

A. Voltage-Controlled Sawtooth Delay Line (VCSDL)

The pulse-to-sawtooth converter is shown in Fig. 1(a). A digitally controlled current, I, will charge the capacitor C_L to generate a ramp signal. To realize a sawtooth signal, the internal clock $\rm CK_{int}$ is converted to a pulse $V_{\rm reset}$ by the pulse generator. $V_{\rm sawtooth}$ will be reset by $V_{\rm reset}$ if the rising edge of the internal clock $\rm CK_{int}$ arrives. Four output bits ($\rm S_3$, $\rm S_2$, $\rm S_1$, and $\rm S_0$) of the 4-bits counter determine the slope of this sawtooth signal.

Fig. 1(b) shows the proposed VCSDL. It is composed of three comparators, two pulse-to-sawtooth converters, a 3-bits digital-to-analog converter (DAC), a 4-bits counter, and a VCSDL output generator (VCSDL_OG). For simplicity, the latency for the pulse-to-sawtooth converter, the comparators, and the VCSDL output generator is neglected. The timing diagram of the VCSDL is shown in Fig. 1(c) and it is realized by two steps: sawtooth slope tuning and phase tracking. These two steps are also summarized by the flow chart as shown in Fig. 1(d). In the first step (i.e., sawtooth slope tuning), the output "Hit" of the third comparator (COMP_amp) is low and the slope of the sawtooth signals will be adjusted. In Fig. 1(b), $V_{\rm ctrl}$ is set to its initial value $V_{\rm init}$, and the 4-bits counter counts up. Therefore, the slope of the sawtooth signals at the outputs of the pulse-to-sawtooth converters will be increased. The output, $V_{\rm out,rise}$, of the first comparator (COMP_1) is realized by comparing $V_{\rm sawtooth,1}$ with $V_{\rm ctrl}$. This comparator's output, $V_{\rm out,rise}$, enters into the VCSDL output generator and the

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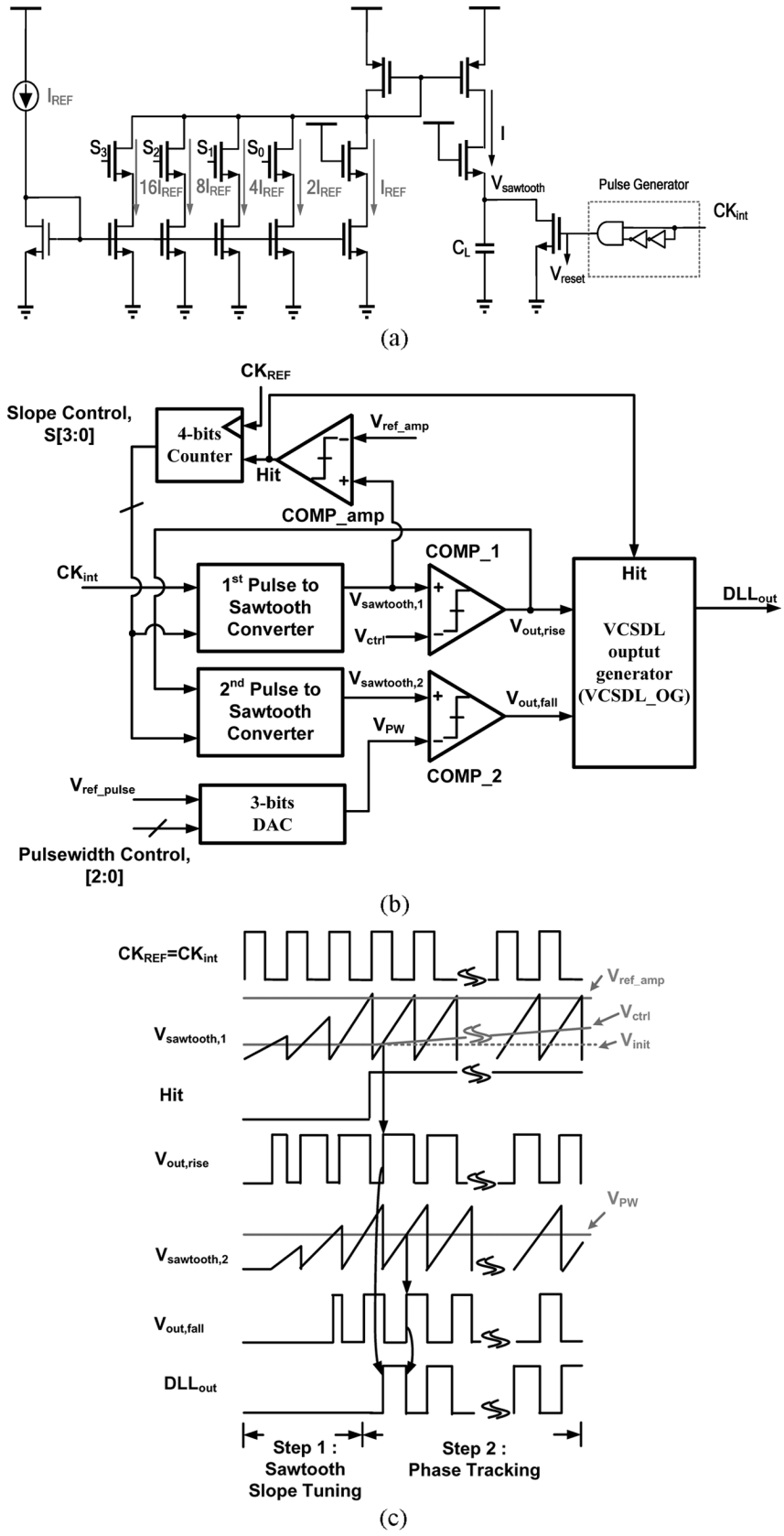


Fig. 1. (a) Pulse-to-sawtooth converter. (b) Proposed voltage-controlled sawtooth delay line (VCSDL). (c) Timing diagram of the proposed VCSDL.

second pulse-to-sawtooth converter. The second comparator (COMP_2) generates $V_{\mathrm{out,fall}}$ by comparing $V_{\mathrm{sawtooth},2}$ and the pulsewidth control voltage V_{pw}. When the amplitude of $V_{\mathrm{sawtooth},1}$ is larger than the reference voltage $V_{\mathrm{ref\_amp}}$, the output "Hit" of the third comparator (COMP_amp) goes high and it is latched in the 4-bits counter. Then, the 4-bits counter

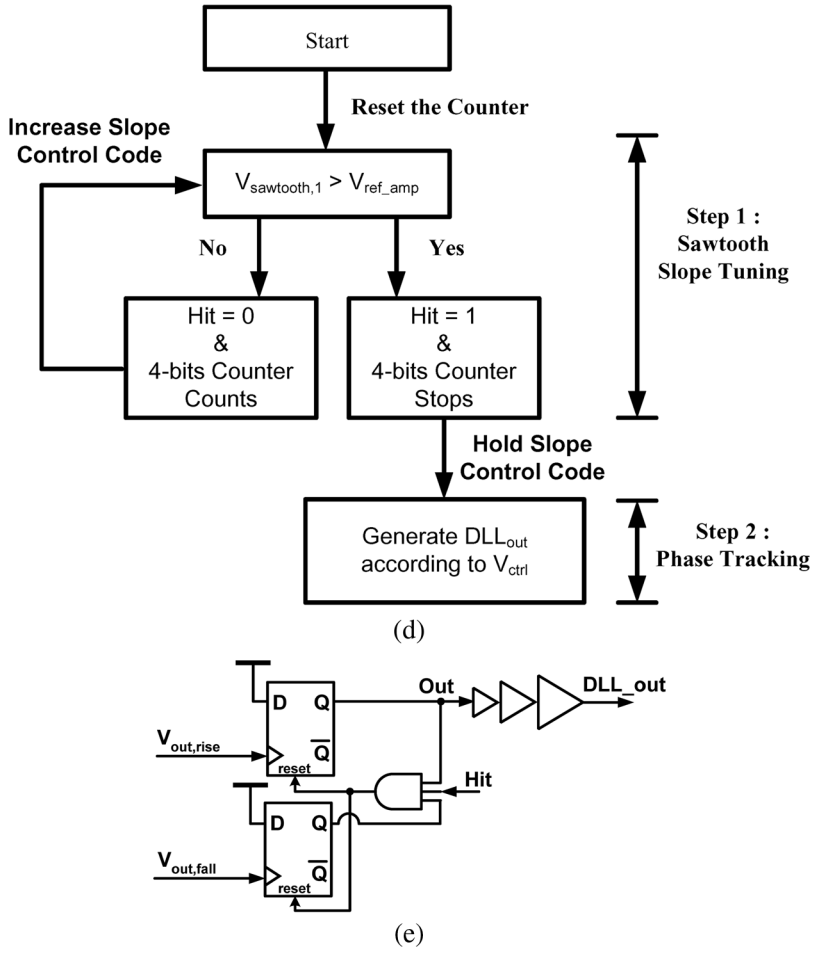


Fig. 1. *(continued)* (d) Flow chart of the VCSDL. (e) VCSDL output generator.

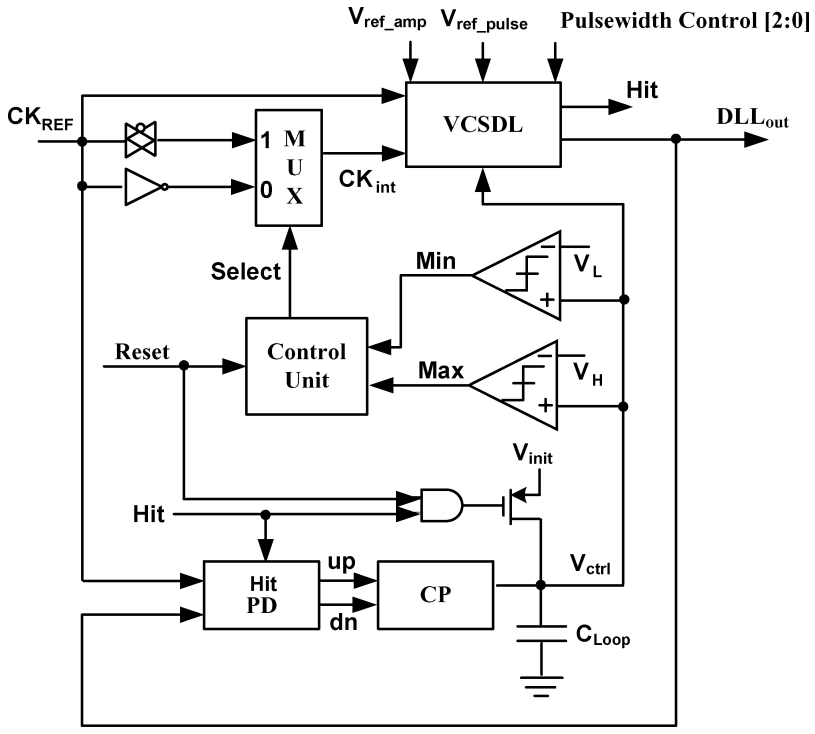
stops, and the slope of the sawtooth signals is fixed. The control voltage $V_{\rm crtl}$ is disconnected from $V_{\rm init}$ and the CG is enabled.

In the second step, the VCSDL output generator generates the output clock $\rm DLL_{out}$ of this DLL and the DLL is under phase tracking. The VCSDL output generator is shown in Fig. 1(e). The VCSDL output generator is composed of two D-flip-flops, an AND gate and a clock buffer. The rising edge of $V_{\rm out,rise}$ becomes the rising edge of $\rm DLL_{out}$, and the rising edge of $V_{\rm out,fall}$ becomes the falling edge of $\rm DLL_{out}$. To increase the control voltage, $V_{\rm ctrl}$, the rising edge of $V_{\rm out,rise}$ will be delayed and the delay of the VCSDL is increased. Thus, the output clock $\rm DLL_{out}$ of the DLL is also delayed. Supposed that $V_{\rm pw}$ is fixed and $V_{\rm ctrl}$ is increased, the delay of VCSDL is increased as shown in Fig. 1(c). In the steady state, the rising edges between reference clock and output of the DLL are in-phase and the corresponding phase difference is eliminated. Note that the delay range of the VCSDL is proportional to the low-level pulsewidth of $V_{\rm out,rise}$. So, it is proportional to the control voltage $V_{\rm ctrl}$ and the ratio of C_L/I in the pulse-to-sawtooth converter, respectively. It means a wide range delay is achieved if the low-level pulsewidth of $V_{\rm out,rise}$ is large. Theoretically, the delay range can be close to one period of the input clock.

The duty cycle of the output clock is controlled by $V_{\rm pw}$. When $V_{\rm pw}$ increases, the rising edge of $V_{\rm out,fall}$ is delayed and the duty cycle of the output clock, $\rm DLL_{out}$, will be increased. In fact, the 3-bits pulsewidth control code will determine $V_{\rm pw}$ by the 3-bit DAC [14]. Thus, the duty cycle of the output clock is adjustable.

B. Proposed DLL

Fig. 2 shows the proposed DLL. It consists of a phase detector (PD), a charge pump, a loop filter, a VCSDL, the comparators, the multiplexer, an AND gate, a PMOS transistor and a control unit. Depending on the "Select" of the control unit, $\rm CK_{init}$ changes its polarity. When the system starts, the signal "Reset" goes high and the signal "Hit" is low to turn on the PMOS transistor. Initially, $V_{\rm ctrl}$ is set to an initial voltage $V_{\rm init}$, which is lower than the high threshold voltage, $V_{\rm H}$, and higher than the low threshold voltage, V_L, and the output "Select" of the control unit is set to high. When the slope of the sawtooth signals is determined, the signal "Hit" in the VCSDL goes high to enable the PD and disconnect $V_{\rm ctrl}$ from its initial voltage. The PD converts the phase error between $\rm CK_{REF}$ and $\rm DLL_{out}$ to control the charge pump. The charge pump and the loop filter generate the control voltage $V_{\rm ctrl}$ to reduce this phase error. The control unit is shown in Fig. 3. When $V_{\rm ctrl}$ is lower than the high threshold voltage $V_{\rm H}$, "Select" is high and the input clock $\rm CK_{REF}$ is chosen as $\rm CK_{int}$. Once $V_{\rm ctrl}$ is larger than the high threshold voltage $V_{\rm H}$, the control signal, MAX, goes high and the inverse $\rm CK_{REF}$ is adopted. Due to the finite input offset voltage in a



Reset	Select	CK_{int}
0	1	CK_{REF}
1	0	$\overline{CK_{REF}}$
1	1	CK_{REF}

Fig. 2. Proposed DLL and the truth table of its control unit.

comparator, the reference voltage, V_L, is higher than the comparator's offset voltage. The reference voltage, $V_{\rm H}$, is lower than the supply voltage by the same amount. From simulations, the input offset voltage of the comparator is smaller than 80 mV in this work. Assume the propagation delays of the inverter and the transmission gate in Fig. 2 are matched. When the multiplexer switches from $\rm CK_{REF}$ to its inverse one for the VCSDL, it is equivalent to increase the delay by $0.5T_{\rm REF}$ where $T_{\rm REF}$ is the period of $\rm CK_{REF}$. The proposed DLL can have the infinite phase shift, since the DLL generates the phase shift from 0° to 360°. Note that the latency of the VCSDL is neglected and the input clock for the VCSDL is $\rm CK_{REF}$ in Fig. 1(c). Once the latency of the VCSDL is considered, the inverted $\rm CK_{REF}$ may be selected as the input clock of the VCSDL. Finally, the VCSDL is adjusted to align the input clock $\rm CK_{REF}$ and the output of the DLL, $\rm DLL_{out}$. By changing the polarity of the input clock of the VCSDL, it increases the delay by $0.5T_{\rm REF}$ where $T_{\rm REF}$ is the period of $\rm CK_{REF}$. The phase switching scheme yields larger transients in this DLL. The transients can be decreased by using a large charge pump current.

This proposed DLL has two advantages. First, the infinite phase shift capability is achieved in a single-loop DLL. Therefore, the chip area and power can be reduced. Second, the jitter performance of the proposed DLL is improved, compared to the dual-loop DLLs. It is because the delay line of the peripheral DLL contributes an extra jitter to the core DLL in the dual loop DLL. Although the proposed VCSDL achieves a very wide range, its highest operation frequency is limited and it can not be used for multi-phase clock generation.

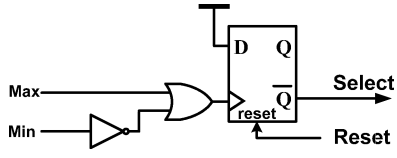


Fig. 3. Control unit.

C. 3-bit DAC

The pulsewidth of the output clock is controlled by $V_{\rm PW}$, which is the output voltage of the 3-bit DAC. This 3-bit DAC shown in Fig. 4 is similar to [14]. It consists of a resistor ladder, a binary-to-thermometer code decoder and an 8-to-1 multiplexer. This 8-to-1 multiplexer, which is realized by the CMOS transmission gates, selects $V_{\rm PW}$ from the resistor ladder. The variable output duty cycle of the DLL is given as

$$\Delta_{\rm duty\_cycle} = \frac{K_{\rm VCSDL}}{T_{\rm REF}} \cdot V_{\rm PW} = \frac{K_{\rm VCSDL}}{T_{\rm REF}} \cdot V_{\rm ref\_pulse} \cdot \frac{N}{2^3} \cdot 100\%, \quad 0 \le N \le 7 \qquad (1)$$

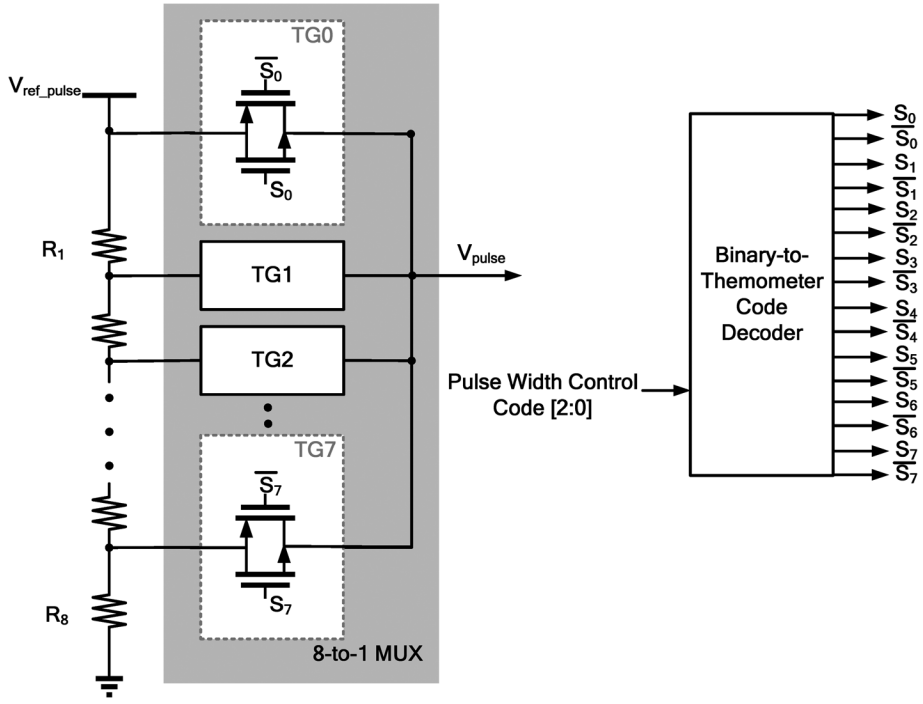


Fig. 4. The 3-bit DAC.

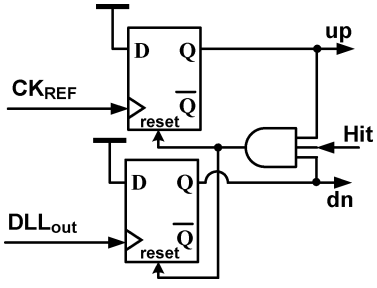


Fig. 5. Phase detector.

where K_{VCSDL} (sec/V) is the gain of the VCSDL, $V_{\mathrm{ref\_pulse}}$ is the reference voltage of this 3-bit DAC, and N is the equivalent pulsewidth control code of the 3-bit DAC [14].

D. Other Circuits

In this work, to mitigate the static phase error, when both the control signals, the charge pump in [12] is used here. A dynamic PD [15] is shown in Fig. 5 to achieve a higher operation frequency. The comparator in the DLL is realized by a differential amplifier with cascaded inverters.

III. The Analysis of the Proposed VCSDL

The pulse-to-sawtooth converter in Fig. 1(b) converts the internal clock to generate the sawtooth signal. The sawtooth signal and the control voltage V_{ctrl} are compared by the comparator to determine the delay range of the VCSDL. Thus, the delay range of the VCSDL is subject to the non-ideal effects, such as the offset voltage of the comparator, the propagation delay of the pulse generator, mismatch between current sources and mismatch between the capacitors in the pulse-to-sawtooth converter. Fig. 6(a) shows a simplified pulse-to-sawtooth converter where a constant current source I and a capacitor C_L are used. Since the comparator may have the finite offset voltage, the amplitude of the sawtooth signal is not exactly equal to $V_{\mathrm{ref\_amp}}$. Here the amplitude of the sawtooth signal is assumed to be V_{amp}. Fig. 6(b) shows the expanded sawtooth signal. The charging time T_{charge} is approximated as

$$T_{\mathrm{charge}} \approx V_{\mathrm{amp}} \cdot \frac{C_L}{I}. \tag{2}$$

Moreover, $T_{\mathrm{charge}} = T_{\mathrm{REF}} - T_{\mathrm{reset}}$ where T_{reset} is the reset time to discharge the capacitor in the pulse-to-sawtooth converter. When V_{ctrl} is equal to V_{amp}, the maximum delay range $T_{\mathrm{VCSDL,max}}$ of this VCSDL is given as

$$T_{\mathrm{VCSDL,max}} = \frac{C_L}{I}(V_{\mathrm{amp}} - V_{\mathrm{offset}}) \tag{3}$$

where V_{offset} is the equivalent offset voltage of the comparator. By changing the polarity of the input clock of the VCSDL, it increases the delay by $0.5T_{\mathrm{REF}}$ where T_{REF} is the period of $\mathrm{CK_{REF}}$. Therefore, to have the infinite phase shift for the proposed DLL, $T_{\mathrm{VCSDL,max}}$ should meet the following constraint

$$T_{\mathrm{VCSDL,max}} > 0.5T_{\mathrm{REF}}. \tag{4}$$

From (3) and (4), the maximum current in the pulse-to-sawtooth converter can be given as

$$I < \frac{(V_{\mathrm{amp}} - V_{\mathrm{offset}}) \cdot C_L}{0.5T_{\mathrm{REF}}}. \tag{5}$$

To generate the signals, $V_{\mathrm{out,rise}}$ and $V_{\mathrm{out,fall}}$, the amplitude of the sawtooth signal should be larger than the equivalent offset voltage, V_{offset}, of the comparator. Therefore, V_{amp} is expressed as

$$V_{\mathrm{amp}} = \frac{I}{C}(T_{\mathrm{REF}} - T_{\mathrm{reset}}) > V_{\mathrm{offset}}. \tag{6}$$

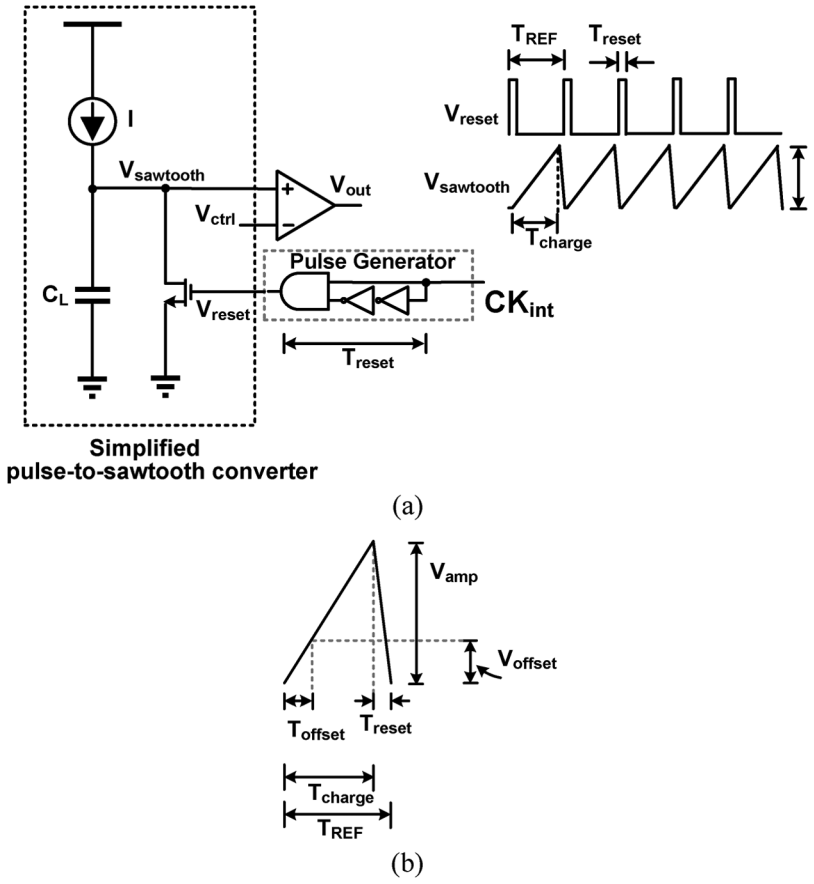


Fig. 6. (a) Simplified pulse-to-sawtooth converter and its timing diagram. (b) Expanded sawtooth signal.

The minimum current source in the pulse-to-sawtooth converter can be rewritten as

$$I > \frac{V_{\text{offset}} \cdot C_L}{(T_{\text{REF}} - T_{\text{reset}})}. \tag{7}$$

To achieve the infinite phase shift for the proposed DLL, the current source in the pulse-to-sawtooth converter should meet the constraints in (5) and (7). It can be expressed as

$$\frac{V_{\text{offset}} \cdot C_L}{(T_{\text{REF}} - T_{\text{reset}})} < I < \frac{(V_{\text{amp}} - V_{\text{offset}}) \cdot C_L}{0.5T_{\text{REF}}}. \tag{8}$$

In this work, T_{reset} is equal to the propagation delay of the pulse generator which is composed of two inverters and one AND gate. T_{reset} is around 170 ps in our process. The reference voltage, $V_{\text{ref\_amp}}$, is chosen as 0.6 V. In the pulse-to-sawtooth converter, the current source is adjustable within I_{REF} and $31I_{\text{REF}}$, which is controlled by 4 bits. The offset voltage, V_{offset}, of the comparator is sensitive to the PVT variations. To have the operation frequency range of this DLL from 50 to 500 MHz, I_{REF} and C_L in the pulse-to-sawtooth converter is chosen as 30 μA and 0.3 pF, respectively, to overcome the variation of V_{offset} and fulfill the constraint of (8).

IV. Experimental Results

The proposed DLL has been fabricated in a 0.18 μm CMOS process. Fig. 7 shows the die photo and its core area is 0.14 mm^2.

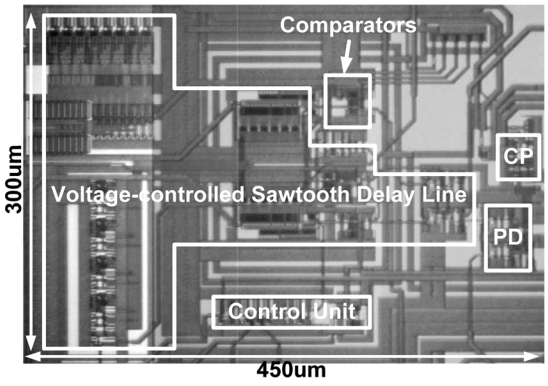


Fig. 7. Die photo.

The DLL operates from 50 to 500 MHz for a 1.5 V supply and it dissipates 6 mW at 500 MHz. The control signal of the multiplexer, "Select", in Fig. 2 can be externally controlled to demonstrate the variable phase range of the proposed DLL. Fig. 8 shows the measured transfer curve of the VCSDL at 500 MHz. The measured phase shift of the VCSDL is from 30° to 253°, when "Select" in the multiplexer in Fig. 2 is high. The variable phase range of 223° is around $0.62T_{\text{REF}}$. When "Select" is low, the variable phase shift of the VCSDL is from 210° to 436°. For (4), it demonstrates that $T_{\text{VCSDL,max}} > 0.5T_{\text{REF}}$. By changing the polarity of the reference clock, the proposed DLL can generate the phase shift from 0° to 360°. In Fig. 8, the overlapped

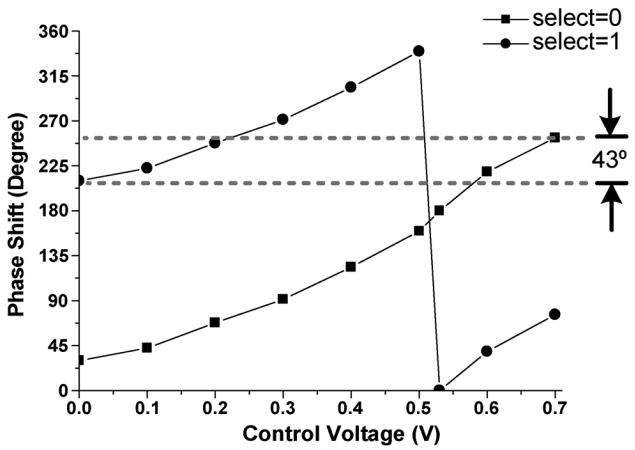


Fig. 8. Measured transfer curve of the voltage-controlled sawtooth delay line.

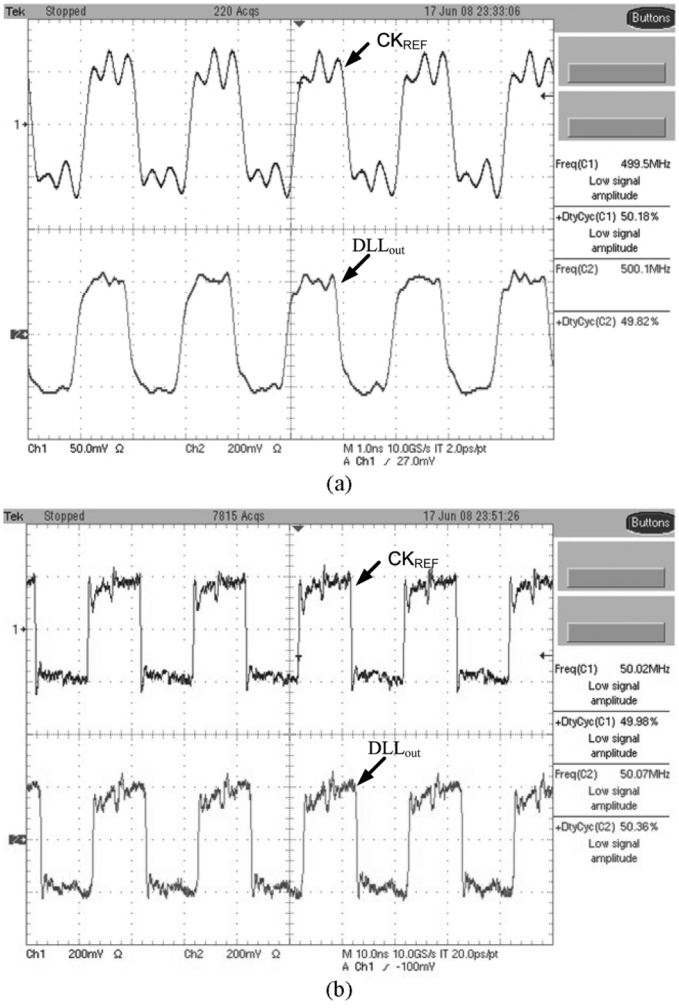


Fig. 9. (a) Output clock with 50% duty cycle at 500 MHz. (b) Output clock with 50% duty cycle at 50 MHz.

phase range is 43°. When the proposed DLL is used to eliminate the phase error between $\mathrm{CK_{REF}}$ and $\mathrm{DLL_{out}}$, the control signal of the multiplexer, "Select", is controlled internally by the control unit in Fig. 2. Fig. 9(a) and (b) show the output clocks with duty cycle of 50% when the proposed DLL is locked at

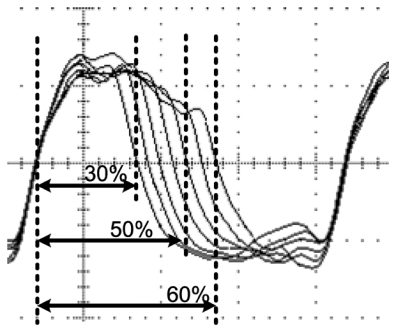


Fig. 10. Measured output clocks with different duty cycles at 500 MHz.

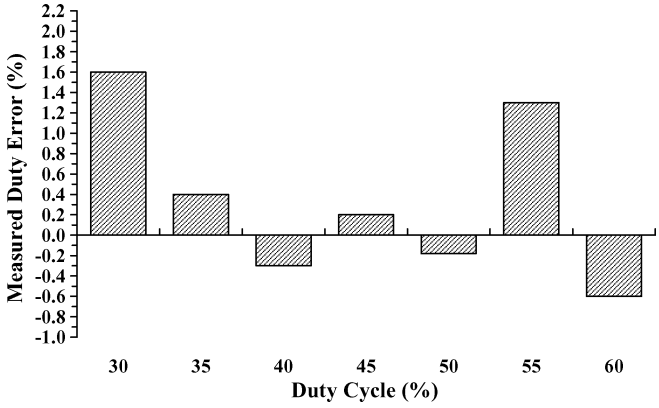


Fig. 11. Measured duty cycle errors for the output clock at 500 MHz.

500 MHz and 50 MHz, respectively. The excessive amount of reflections for the output clock waveforms in Fig. 9 and Fig. 10 are due to inadequate termination and cross coupling between signals. Fig. 10 shows the measured output clocks with different duty cycles at 500 MHz. The measured duty cycles of the output clocks at 500 MHz can range from 30% to 60% in a step of 5%. The measured duty cycle errors at 500 MHz are also shown in Fig. 11.

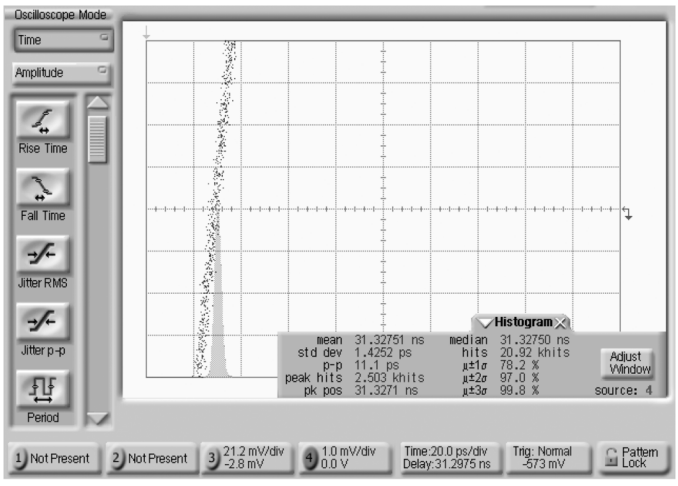
Fig. 12(a) and (b) show the measured period jitter histogram of the output clock at 500 MHz and 50 MHz, respectively. Fig. 13 shows the measured period jitters for different input frequencies. At 50 MHz, the measured rms and peak-to-peak period jitters are 2.62 ps and 16.9 ps, respectively. As the operation frequency goes up to 500 MHz, the measured rms and peak-to-peak period jitters go down to 1.43 ps and 11.1 ps, respectively.

The figures-of-merit (FOMs) for both power consumption and chip area are shown in Fig. 14(a). $\mathrm{FOM_{power}}$ [13] is defined as

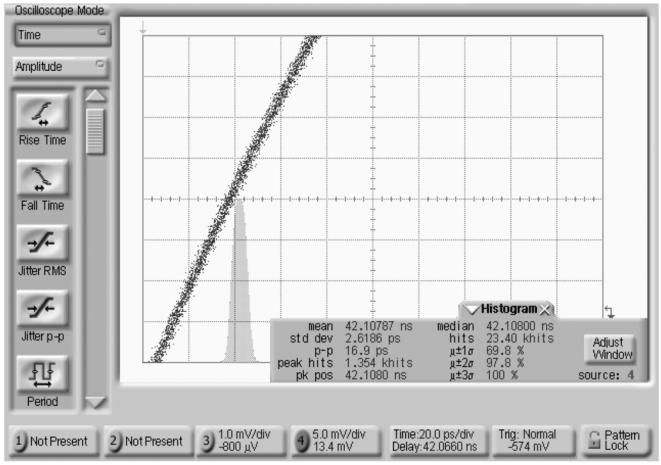
$$\mathrm{FOM_{POWER}} = \frac{\text{Power consumption(mW)}}{\text{Maximum operation frequency(MHz)}} \tag{9}$$

where the power consumption is represented in mW and the maximum operation frequency is represented in MHz. $\mathrm{FOM_{AREA}}$ [13] is defined as

$$\mathrm{FOM_{AREA}} = \frac{\text{Active area(mm}^2\text{)}}{\text{Channel length}^2 \cdot \text{Maximum delay}(\mu\text{m}^2 \cdot \text{ns})} \tag{10}$$



(a)



(b)

Fig. 12. Measured period jitter histogram for the output clock at (a) 500 MHz and (b) 50 MHz.

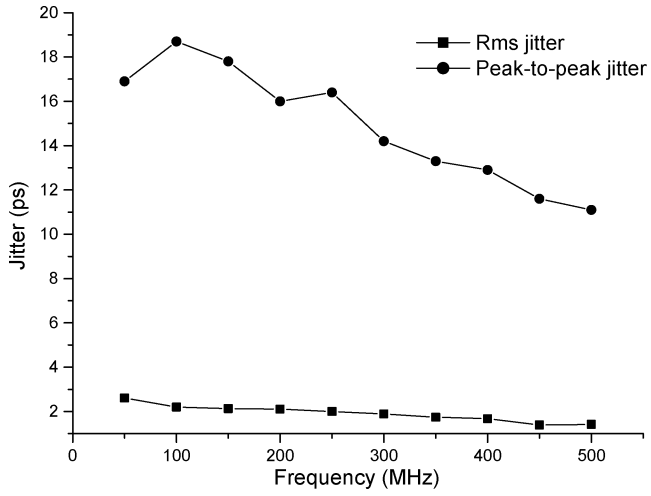
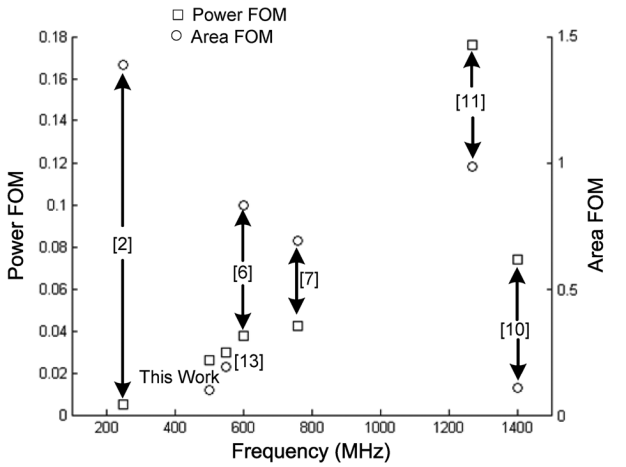
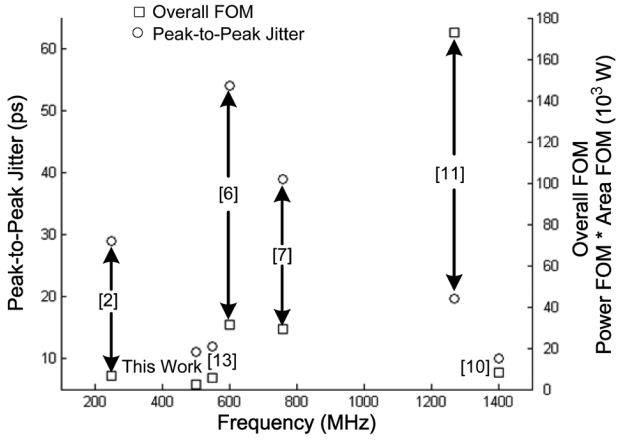


Fig. 13. Measured peak-to-peak and rms period jitters for different input frequencies.

where the occupied area is in square millimeters, the minimum channel length is in micrometers, and the maximum delay is the



(a)



(b)

Fig. 14. (a) Figures-of-merit for power and area. (b) Overall figures-of-merit for DLL and jitter performance.

delay time for the lowest operation frequency in nanoseconds. Fig. 14(b) shows the overall FOM and the jitter performance. The overall FOM is defined as the product of the $\mathrm{FOM_{POWER}}$ and the $\mathrm{FOM_{AREA}}$. The proposed DLL achieves the smallest FOM among the works in Fig. 14(b). Table I gives the performance summary and comparison with the previous works.

V. Conclusion

A wide range DLL with infinite phase shift and digital-controlled duty cycle is presented. By changing the polarity of the input clock of the voltage-controlled sawtooth delay line, this proposed DLL achieves infinite phase shift by only a single loop. Moreover, the analysis for the proposed VCSDL is also given. The experimental results show that the measured rms jitter and peak-to-peak jitter is 1.43 ps and 11.1 ps, respectively, at 500 MHz. Its power consumption is 6 mW for a supply of 1.5 V.

Acknowledgment

The authors would like to thank National Chip Implementation Center (CIC), Taiwan, for fabricating the chips.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[2]	[6]	[7]	[10]	[11]	[13]	This work
Process	0.35um	0.25um	0.18um	0.25um	0.35um	0.18um	0.18um
Supply Voltage	3.3V	2.5V	1.8V	2.5V	3.3V	1.8V	1.5V
Max. Operation Frequency	250MHz	600MHz	760MHz	1400MHz	1.27GHz	550MHz	500MHz
Min. Operation Frequency	62.5MHz	150MHz	60MHz	770MHz	1GHz	40MHz	50MHz
Output Duty Cycle Control Range	No	50%	No	25%~75%	35%~70%	50%	30%~60%
Synchronous	Yes	Yes	Yes	No	Yes	Yes	Yes
Infinite Phase Shift	No	Yes	Yes	No	No	No	Yes
Architecture	Single Loop	Dual Loop	Dual Loop	No	Single Loop	Single Loop	Single Loop
Peak-to-Peak Jitter	29ps @250MHz	54ps @400MHz	39ps @700MHz	10ps @1GHz	19.6ps @1.25GHz	12ps @550MHz	11.1ps @500MHz
Power	41.6mW	60mW	63mW	18mW	150mW	12.6mW	6mW
Core Area	0.08mm^2	0.13mm^2	0.19mm^2	0.05 mm^2	0.14mm^2	0.2mm^2	0.14mm^2

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