Equalization of Third-Order Intermodulation Products in Wideband Direct Conversion Receivers

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***Abstract*—This paper reports a SAW-less direct-conversion receiver which utilizes a mixed-signal feedforward path to regenerate and adaptively cancel IM3 products, thus accomplishing system-level linearization. The receiver system performance is dominated by a custom integrated RF front end implemented in 130-nm CMOS and achieves an uncorrected out-of-band IIP3 of −7.1 dBm under the worst-case UMTS FDD Region 1 blocking specifications. Under IM3 equalization, the receiver achieves an effective IIP3 of +5.3 dBm and meets the UMTS BER sensitivity requirement with 3.7 dB of margin.**

***Index Terms*—Adaptive equalization, adaptive signal processing, digital linearization, feedforward equalization, mixed-signal linearization, nonlinear circuits, postdistortion, RF receivers, system-level linearization, wireless communications.**

I. Introduction

SELF-GENERATED interference in RF receivers is the general result of signals interacting with circuit block nonidealities in such a way that error terms arise and corrupt the desired signal intended for reception. This interference is sometimes so severe that even increasing the circuit area and power dissipation arbitrarily to reduce the nonidealities is insufficient, and costly off-chip components are required for the receiver to meet specification. Often, this self-generated interference manifests itself as distortion products due to circuit block nonlinearities, but can also arise due to I-Q mismatch, interstage coupling, or various other mechanisms.

Unfortunately, it can also be said that these problems worsen in general as CMOS processes continue to scale. As supply voltages drop, less headroom is available to apply large overdrive bias voltages to devices, worsening their linearity and matching properties. Furthermore, as market pressures demand the further reduction in the number and size of off-chip components, auxiliary blocks that once facilitated receiver design, such as off-chip SAW filters, will become extinct. Therefore, there exists a great need to conceive and develop monolithic solutions to self-generated interference problems in RF receivers.

II. System-Level Solutions

A. General Solution Strategies

Although the prognosis for self-generated interference issues is bleak, the nature of the problem yields a plausible solution strategy. Most significantly, the error-producing signal is retained in the system at some point, while the error-generation mechanism is known, at least qualitatively. This knowledge was delineated in a general scheme described in [1] in which error producers within the RF receiver were applied to a rough model of the error generation mechanism to generate a reference signal consisting of solely the corruptive error. However, the actual model of the error is never known precisely. Hence, as shown in Fig. 1, an adaptive equalization algorithm is employed to subtract the reference signal from the corrupted main receiver path, as it can account for minor uncertainties in the effective alternate path baseband transfer function. Note that for simplicity in Fig. 1, only a dc gain uncertainty is shown.

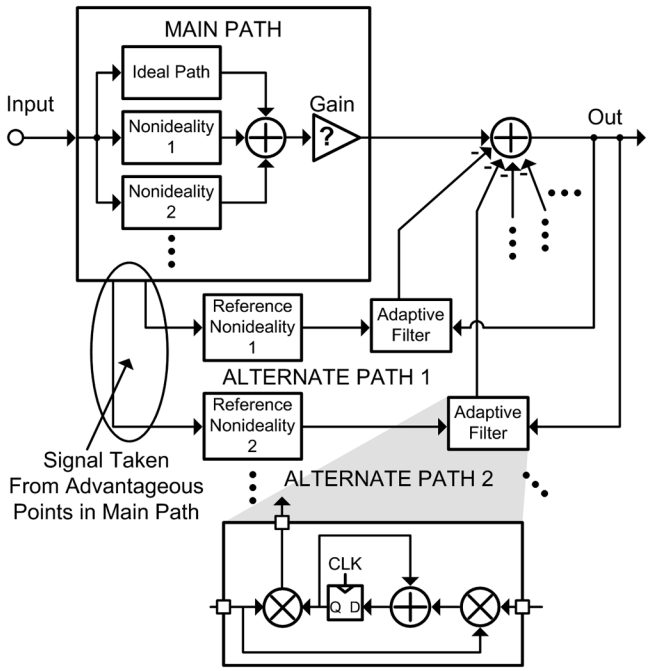

Fig. 1. General adaptive feedforward receiver concept.

Such a system-level solution methodology is advantageous for many reasons, not the least of which is its indifference towards the details of the original receiver. As this technique focuses only on cancellation of the error itself and not the error producers, it permits a relatively narrowband alternate path. That is, although large, undesired, error-producing signals may occur over a wide frequency range, the relevant error terms that they produce are only restricted to a much smaller bandwidth equal to that of the desired signal. The circuits processing the error operate with a lower dynamic range than their original receiver counterparts, as the corruptive error to noise ratio is in general much less than the error producer to noise ratio in the

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TABLE I
REPORTED IIP3 SPECIFICATION AND PERFORMANCE COMPARISON

Reference	IIP3 Specification	IIP3 Performance
[7]	+1.3dBm	+1.6dBm
[8][1]	-6.1dBm	-0.5dBm
[9]	-10dBm	-7.4dBm
[10]	-8dBm	-7dBm
[11]	-5dBm	-2dBm

1) Measurement at mixer transconductor input

main path. Also, if the LMS algorithm is used to perform the adaptive equalization, multiple LMS loops in parallel can be used to cancel different interference signals as shown in Fig. 1. [2] Finally, in the event that the self-generated interference of interest is due to large, undesired blocker signals, the power dissipation of an alternate path can be further reduced by only powering it on when needed, as most receivers only need to operate in the presence of strong interferers for a small fraction of the time.

B. Study Motivation and Application to Nonlinear RF Receivers

Due to the continued and rising popularity of FDD standards for 3G wireless communications, of notable current interest to the circuit design community is the task of improving the linearity of RF receiver front ends. It has been recognized in recent reports that adaptive feedforward error cancellation is useful in dealing with this problem [2]–[4]; however, the current literature only contains at most descriptions of high-level system studies implemented with discrete RF components. Hence, it is desirable to study the implications of applying this technique to a specification-compliant custom-designed RF front end to assess its suitability for commercial devices. This paper describes an experiment in which such a front end is implemented for the UMTS Region 1 standard in order to compensate for the exacting linearity requirements implicitly imposed by the FDD out-of-band blocker test [5]. In order to meet these requirements, several reported commercial receivers [6]–[8] have resorted to the use of interstage SAW filters to attenuate large blocker signals and hence to relax requirements on the integrated circuit blocks. Recently, several SAW-less UMTS receivers have also been reported, albeit with somewhat lower out of band IIP3 performance [9]–[11]. It should be noted that reported IIP3 specifications and achievements vary widely within the literature, as shown in Table I. This variation is, at least in part, due to the fact that the IIP3 specification depends on the receiver achieved noise figure, the peak TX power which must be handled, and the characteristics of the particular duplexer used, as discussed in Section III-B. Although the SAW-less receivers mentioned above meet their respective self-imposed out-of-band IIP3 specifications, it is worthwhile to consider the design of SAW-less receivers with still higher IIP3 in this context in order to permit the use of less stringent, and possibly also less expensive, duplexer blocks.

The general concept behind the adaptive feedforward IM3 cancellation scheme introduced in this work is shown in Fig. 2. In this figure, a nonlinear main receiver path is subject to two large blockers such that the desired signal is overwhelmed by the

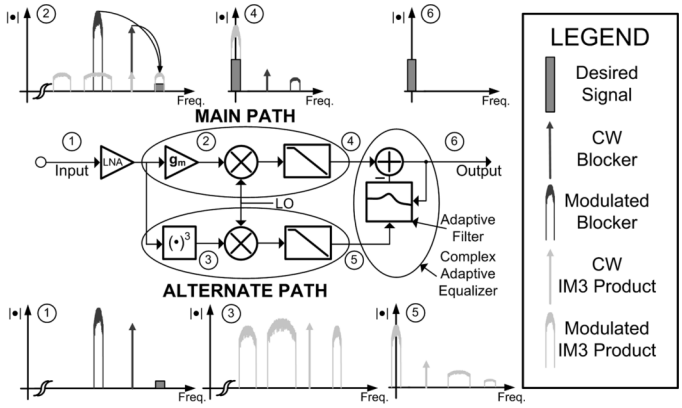

Fig. 2. Adaptive feedforward error cancellation concept applied to RF receiver third-order distortion in this work.

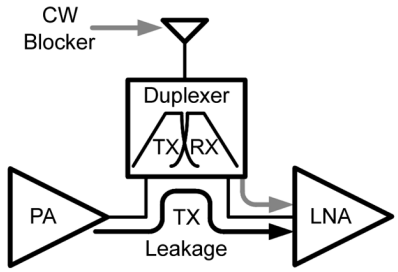

Fig. 3. FDD two-tone blocking problem.

self-generated IM3 interference products. The figure reflects the fact that the UMTS out-of-band blocking requirement [5] is an implicit two-tone test with one of the "tones" being the modulated TX output leakage through the antenna duplexer, as shown in Fig. 3. Reference IM3 products are generated at RF by a cubic term generator, while choosing the LO frequency of the alternate path mixer to be the same as that of the main path guarantees that the proper set of IM3 products are downconverted to baseband characteristics. Baseband postfiltering attenuates to negligible levels unwanted IM3 products in the alternate path such that the adaptive equalizer converges based only on the statistics of the IM3 products corrupting the desired signal at baseband. In this fashion, the equalized IM3 products of the alternate path can be directly subtracted from the main path, leaving only the desired RX signal. Note that this technique is not limited to a two-tone test but also removes IM3 products resulting from a three-tone test. Furthermore, this technique does not require prior knowledge of one or more of the blocker frequencies, as do techniques that rely on the cancellation of TX leakage to meet the UMTS linearity specifications [12], [13]. Although both IM2 and IM3 products can be concurrently cancelled by parallel LMS adaptive filters, it was decided in this project to leverage recent work [14], [15] to perform local IIP2 improvements in order to avoid adding additional ADCs to the system to pass reference IM2 products.

Most importantly, the technique described in this paper differs from those presented in [3] and [4] in that reference IM3 products are generated at analog RF rather than at digital baseband. It can be shown with trigonometric identities that the resultant downconverted IM3 products are the same as

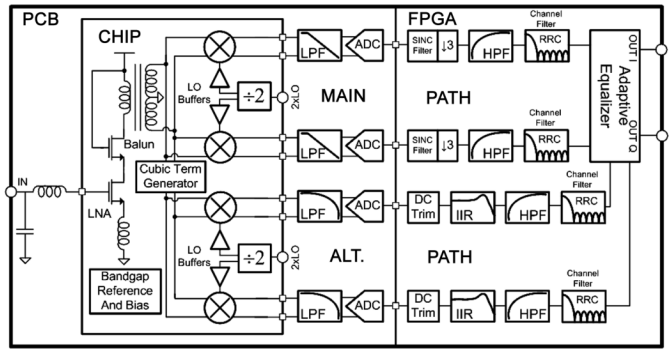

Fig. 4. Experimental UMTS receiver architecture.

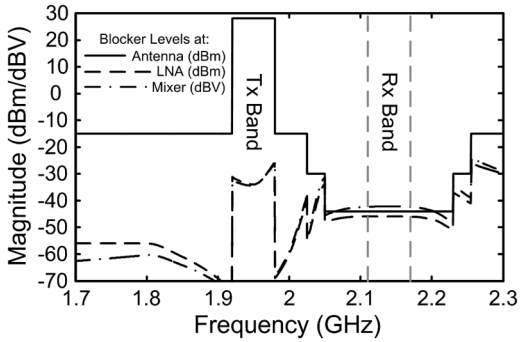

Fig. 5. Expected UMTS blocker profile at various points in the receiver.

those that would have been produced by I and Q baseband cubic term generators. IM3 generation in the continuous-time domain as performed in this work is the preferred method in an integrated downconversion receiver since it permits the use of relatively narrowband postfilters and ADCs, such as those based on $\Sigma\Delta$Ms. For the architectures in [3] and [4] to cancel IM3 products for UMTS, the ADCs must pass the full spectrum of potential problematic blockers (1670–1850 MHz, 1920–1980 MHz, 2015–2075 MHz) and would require at least 6 Nyquist ADCs and digital paths with sampling rates in excess of 60 MHz. Such requirements render this strategy unattractive in that this new circuitry would consume far more power than the original mixed-signal and digital portion of the receiver. Given that IM3 generation is therefore to be performed in the analog domain, it should additionally be performed at RF after the LNA, where the blocker magnitudes are at their largest point in the receiver.

III. Receiver Architecture

A. Receiver Architecture Description

The receiver architecture described in this paper is shown in Fig. 4. It centers around a custom-designed front end implemented in 130-nm RF CMOS. The chip is fully ESD protected and operates off of a 1.2 V supply, except for the bandgap circuitry that operates off of 2.7 V (drawing 2.5 mA). The chip is placed on a gold-plated dielectric substrate which is then mounted onto the PCB. Analog baseband circuitry is implemented on the PCB using low-power commercially available discrete components. Finally, a digital back end containing rate change, channel filtering, and equalization blocks is implemented on an FPGA platform.

Although it is possible to perform the equalization in analog circuitry, shifting as much of the signal processing to the digital domain affords several advantages. For example, the behavior of digital circuitry is relatively insensitive to process variations, the continued scaling of CMOS processes has rendered baseband digital blocks power-competitive compared to equivalent analog blocks [16], and digital circuits facilitate the implementation of reconfigurable multimode receivers [17].

Implementing the baseband components off-chip has negligible impact on this experiment, as the integrated front end typically dominates the performance of the RF receiver. In an actual implementation, the receiver main path would also include VGA functionality. The experimental receiver described herein is for proof-of-concept only and represents the case when the receiver is attempting to decode a signal near sensitivity. Were a VGA present in the main path, and were its gain to be changed during alternate path operation, the adaptive nature of the alternate path would allow the equalizer to quickly track the change and maintain IM3 cancellation.

B. Translation of Specification to System Requirements

In order to determine the worst-case blocking (alternatively denoted as peak blocking) scenario seen by the receiver circuitry, the UMTS blocker specification [5] must be used in conjunction with the frequency response of the duplexer shown in Fig. 3. From Fig. 5 it can be seen that for the duplexer described in [18], the largest IM3 products occur when $f_{\rm TX} = 1.98$ GHz, $f_{\rm CW} = 2.05$ GHz, and $f_{\rm RX} = 2.12$ GHz. In this case, the blocker powers are $P_{\rm TX} = +28$ dBm and $P_{\rm CW} = -30$ dBm at the antenna and $P_{\rm TX} = -26$ dBm and $P_{\rm CW} = -34$ dBm at the LNA input. Interestingly, in this case, the worst-case blocking scenario does not occur over the band in which the specified CW blocker is -15 dBm.

According to [19], the UMTS specifications impose an analog requirement of $\mathrm{NF}_{\rm ANT,MAX} = 9$ dB at the antenna. Adopting a more general definition of NF, which will be denoted as error figure (EF) to encompass other forms of error including distortion products, the UMTS specification allows $\mathrm{EF} = \mathrm{NF} + 3$ dB under blocking conditions. In other words, $\mathrm{EF}_{\rm ANT,MAX} = 12$ dB. Given the insertion loss of the duplexer [18] $L_{\rm DUP} = 1.8$ dB and that $\mathrm{NF}_{\rm ANT} = L_{\rm DUP} + \mathrm{NF}_{\rm RX}$, it is easily computed that $\mathrm{NF}_{\rm RX,MAX} = 7.2$ dB and $\mathrm{EF}_{\rm RX,MAX} = 10.2$ dB at the LNA input.

For UMTS, the noise due to the 50 Ω source resistance is $\mathrm{kTB} = -108\,\mathrm{dBm}/3.84\,\mathrm{MHz}$ at the LNA input. Denoting all quantities as LNA input-referred, this implies that after removing source noise, the maximum allowed receiver noise power is $N_{\rm RX,MAX} = -101.7\,\mathrm{dBm}/3.84\,\mathrm{MHz}$. Assuming that the error under worst-case blocking is dominated by thermal noise and IM3 distortion, the error figure limit implies that the rms sum of $I_{\rm RX,MAX}$ and $N_{\rm RX,MAX}$ is -98.2 dBm/3.84 MHz, where $I_{\rm RX,MAX}$ is the maximum allowed IM3 distortion product power. It follows

that $I_{\mathrm{RX,MAX}} = -100.8$ dBm/3.84 MHz. Using these values in expression (1) yields $\mathrm{IIP3_{RX,MIN}} = +3.4$ dBm.

$$\mathrm{IIP3_{RX,MIN}} = \frac{1}{2}[2P_{\mathrm{CW}} + P_{\mathrm{TX}} - I_{\mathrm{RX,MAX}}]. \quad (1)$$

The problem with this requirement is that it is inconsistent with typical attainable values for SAW-less receivers in the absence of special enhancements. For example, typical values for $\mathrm{IIP3_{MIXER}}$ range from +8 to +12 dBm [13]. For the initial design in this work, the simulated values for G_{LNA} and $\mathrm{IIP3_{LNA}}$ are 17 dB and +6 dBm, respectively. Recalling the IIP3 relation (2) from [20], as used in [13], such design values yield $\mathrm{IIP3_{RX}} = -9.1$ dBm for a mixer IIP3 of +8 dBm

$$\mathrm{IIP3_{RX}} = \left(\frac{1}{\mathrm{IIP3_{LNA}}} + \frac{G_{\mathrm{LNA}}}{\mathrm{IIP3_{MIXER}}}\right)^{-1}. \quad (2)$$

Clearly a significant discrepancy arises and some sort of additional IIP3 enhancement is required to meet the input-referred error specification.

To assist in the design of the feedforward linearity enhancement proposed in this paper, a quantity termed the IM3 product-to-error ratio (IER) is introduced. In this case, the "E" term represents all error except for IM3 products. The IER of the main path under peak blocking conditions ($\mathrm{IER_{MAIN,PK}}$) can be determined using the receiver IIP3 value in the previous paragraph. Using (1), the LNA input-referred main path IM3 product magnitude under peak blocker conditions $I_{\mathrm{MAIN,PK}}$ is equal to −75.8 dBm/3.84 MHz. Adding 2 dB of margin to the NF requirements and assuming that $\mathrm{EF_{RX,MAX}} = \mathrm{NF_{RX,MAX}} + 2$ dB (allowing 1-dB margin for error due to the alternate path), the maximum error, including 50 Ω source noise but not IM3 products, referred to the main path LNA input is $E_{\mathrm{MAIN,PK}} = -100.8$ dBm. Hence, $\mathrm{IER_{MAIN,PK}} = 25$ dB. The usefulness of this number is that it can be used to determine the required dynamic range of the alternate path in Section V.

IV. Main Path Block Design

A. LNA and Balun

Reflecting a typical choice for narrowband receivers, the integrated front end employs an inductively degenerated cascode LNA. As the duplexer [18] has a single ended output, the LNA must have a single ended input. However, as the SAW filter to be removed for this design previously handled the single-ended to differential conversion between the LNA and mixer, provisions for performing this task must now be made on chip. An area-efficient method of accomplishing this goal is to place a secondary inductor winding inside of the LNA load inductor, creating a transformer balun. The LNA and balun designs are depicted in Fig. 6.

B. Mixer and LO Buffer

As the system proposed in this paper only equalizes IM3 products, the mixer utilizes a folded high-IIP2 mixer in order to obviate any IM2 equalization [15]. The schematic of this mixer as implemented is shown in Fig. 7. In order to drive the large gate capacitances of the mixer switching pair, an actively

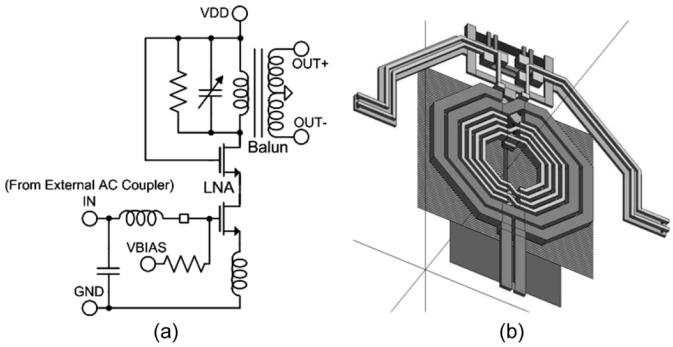

Fig. 6. Implementation of main path LNA and balun. (a) Schematic depiction. (b) Balun 3-D CAD representation.

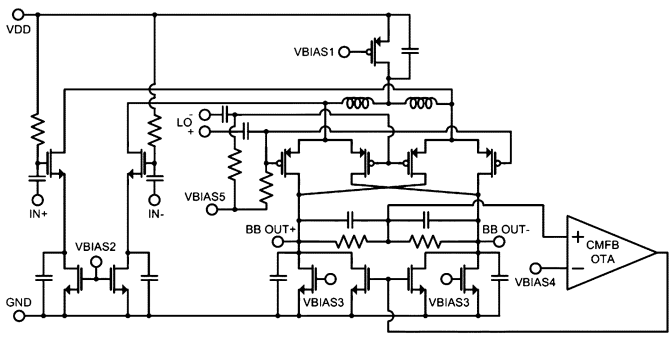

Fig. 7. Schematic of the main path mixer.

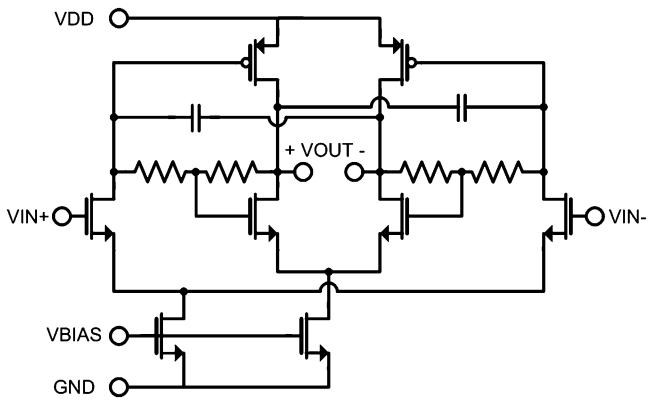

Fig. 8. Schematic of the main path LO buffer.

loaded Cherry-Hooper LO buffer is utilized. The schematic of this block shown in Fig. 8 reflects some biasing and neutralization modifications to the circuit shown in [6], permitting it to function under the low voltage supply headroom. Separate divide-by-two circuits are included immediately adjacent to the LO buffers in order to avoid problems associated with on-chip RF-LO coupling [21].

C. Analog and Digital Baseband Circuitry

The required order of the analog postfilter is obtained by considering the worst-case frequency translation to baseband of the blocker profile depicted in Fig. 5 after the LNA transfer function is added to the profile. It was found that for an ADC sampling rate of 50 MHz, a third-order Chebyshev filter in the analog domain was sufficient to attenuate downconverted out-of-band

blocker signals to levels negligible with respect to the thermal noise floor. This filter was implemented on PCB with a nominal passband edge frequency of 2.3 MHz with the real pole formed by the output stage of the mixer. The filter also includes an additional gain stage that drives the ADC, which utilizes an 8-bit pipelined architecture. The ADC sampling rates were chosen to be not equal to a multiple of the UMTS chip rate in order to facilitate testing with the particular FPGA platform used. However, as the baseband digital signal is oversampled, this choice does not compromise the integrity of the experiments presented herein. Coarse dc offset adjustments prior to the digital HPFs are also implemented to avoid saturating the baseband circuitry. Close-in adjacent channel filtering is provided in the digital domain by a 25-tap root-raised cosine FIR filter running at 16.66 MHz.

V. Alternate Path Block Design

As mentioned in Section III-B, a useful metric for the design of the alternate path is its IER under peak blocking conditions, denoted $\mathrm{IER}_{\mathrm{ALT,PK}} = I_{\mathrm{ALT,PK}}/E_{\mathrm{ALT,PK}}$. Denoting the gain of the main path as G_{MAIN} and the gain of the alternate path from the IM3 term generator to the output of the adaptive equalizer as G_{ALT}, it can be seen that the adaptive equalizer forces $G_{\mathrm{MAIN}}I_{\mathrm{MAIN,PK}} = G_{\mathrm{ALT}}I_{\mathrm{ALT,PK}}$, with any discrepancy in this equality counting towards $\mathrm{IER}_{\mathrm{ALT,PK}}$. To obtain $\mathrm{EF}_{\mathrm{RX,MAX}}$, all error is referred to the output of the equalizer in (3)

$$\mathrm{EF}_{\mathrm{RX,MAX}}(\mathrm{dB}) = 10\log_{10}\left(\frac{E^2_{\mathrm{MAIN,PK}}G^2_{\mathrm{MAIN}}+E^2_{\mathrm{ALT,PK}}G^2_{\mathrm{ALT}}}{G^2_{\mathrm{MAIN}}kTB}\right). \quad (3)$$

From the equality forced by the adaptive equalizer, substitution yields (4)

$$\mathrm{EF}_{\mathrm{RX,MAX}}(\mathrm{dB}) = 10\log_{10}\left(\frac{E^2_{\mathrm{MAIN,PK}}}{kTB}\right) + 10\log_{10}\left(1+\frac{\mathrm{IER}^2_{\mathrm{MAIN,PK}}}{\mathrm{IER}^2_{\mathrm{ALT,PK}}}\right). \quad (4)$$

The second term in (4) represents the excess error figure due to the operation of the alternate path. Given the design numbers in Section III, $\mathrm{IER}_{\mathrm{ALT,PK}} > 31$ dB. For simplicity, this error requirement is split equally between the cubic term generator and the remainder of the alternate path, yielding $\mathrm{IER}_{\mathrm{CUB,PK}} > 34$ dB.

A. Cubic Term Generator

1) Requirements of Cubic Term Generator: As the cubic term generator is an unconventional block in a receiver, it is important to first determine its particular requirements prior to its design. Aside from that of IER mentioned above, the circuit must heavily attenuate the incoming desired signal (i.e., linear term feedthrough) with respect to the IM3 products. This is visually depicted at point 3 of Fig. 2, where the desired signal around the LO frequency is absent from the spectrum. The reason for this is that any desired signal at the reference input of the equalizer will be treated as error by the adaptive algorithm. As the algorithm functions so as to minimize mean squared error, it will attempt to strike a balance between eliminating the IM3 products and desired signal, reducing small signal gain, IM3 cancellation, or both.

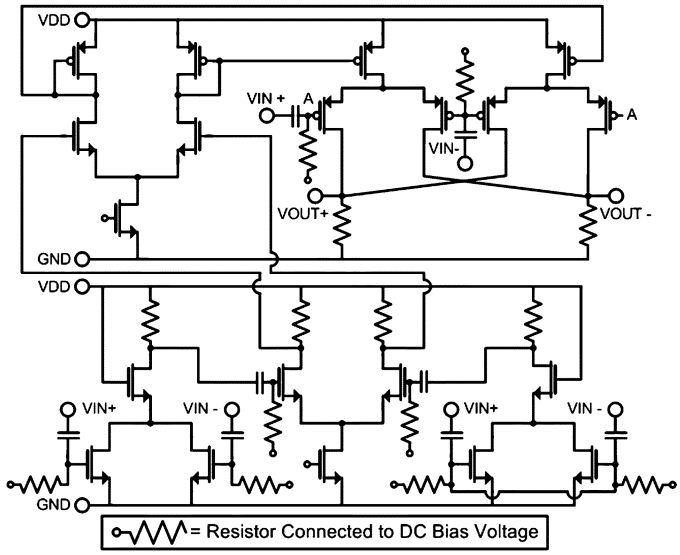

Fig. 9. Cubic term generator schematic.

The cubic term generator error that contributes to IER is composed of both thermal noise and other nonlinear terms. A reasonable design procedure is to ensure that the IER due to higher order harmonic products under peak blocking conditions is significantly larger than the IER requirement. This requirement can be verified in simulation with a harmonic balance simulation, varying the number of calculated harmonics in order to isolate the magnitude of higher-order terms that fall around the same frequency as the IM3 products.

2) Prior Art in Cubic Term Generators: Cubic term generators, or expansions thereof, have been used extensively in the literature for predistortion of nonlinear transmitter power amplifiers. Early circuits utilized the crossover distortion characteristic of back-to-back diodes [22], [23]. Subsequent developments in predistortion circuits often utilized networks of cascaded Gilbert cell mixers [24]–[26], while architectures explicitly utilizing the third-order Taylor series coefficient of the MOS transistor have been reported as well [27].

3) Implementation of Cubic Term Generator: The complete cubic term generator implemented for this work is shown in Fig. 9. As in [25], the cubing is broken up into two suboperations, a choice that potentially realizes an IM3-to-noise ratio (INR) benefit over architectures such as [27] in that the initial distortion products are only attenuated with respect to the noise of the distortion-producing devices as the square rather than the cube of the input signal. In this case, however, the initial operation is performed by a canonical MOS squaring circuit, located at the lower left of the schematic. This choice is made in order to avoid the generation of higher-order intermodulation products associated with the nonlinearity of the Gilbert cell current commutating devices. As the MOS squaring circuit produces a single ended output, it must be followed by an active balun to recast the signal differentially. One potential issue with

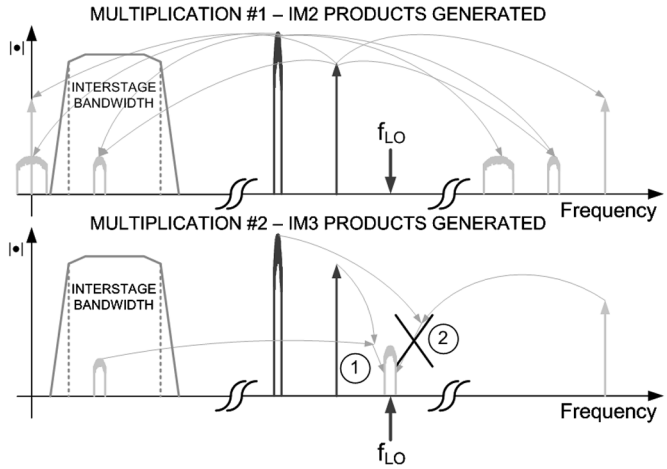

Fig. 10. Frequency domain depiction of proposed cubic term generator internal bandwidth limitation.

this scheme is that the squaring circuit directly passes common mode signal. If the balun negative terminal were grounded, the common mode signal would be recast differentially as well and would propagate through the remainder of the circuit. In order to provide some measure of common mode rejection, a dummy squaring circuit is added to the negative terminal of the balun. With the gate terminals of the dummy squaring circuit tied together, this circuit only passes common mode signal. Hence, the common mode signal is rejected by the CMRR of the balun and subsequent gain circuits.

The final multiplication of the cubic term generator is performed by a Gilbert cell multiplier. In this case, the nonlinearity of the current commutating devices can be improved at the expense of gain by increasing the multiplying device overdrive voltages. The lost gain can then be made up earlier in the circuit. The circuit as implemented is somewhat power-inefficient due to the voltage output at RF. This was done for testing purposes, but in a commercial implementation the IM3 reference signal would be passed to mixer switching pairs solely in the current mode.

Note that in this architecture, linear term rejection will be limited only by device mismatch and coupling. It is hence expected that this effect will be negligible. Furthermore, the circuit is verified in simulation to produce higher-order nonlinear terms at levels well below the required alternate path error floor for the two cases of when the nominally CW blocker from [5] is CW and amplitude-modulated with suppressed carrier.

4) Bandlimited Nature of Cubic Term Generator: The alternate path in this work needs to accurately reproduce only the subset of IM3 products that land around $f_{\rm LO}$ in the main path. It can be proven via trigonometric identities that in order to achieve this in the specified UMTS blocking condition, only the IM2 content around the two-tone beat frequency needs to be retained in the cubic term generator interstage circuitry, as depicted in Fig. 10. For UMTS, the beat frequency range is from 65–250 MHz, which is much less than the 4.15 GHz bandwidth required to retain all of the IM2 products generated by the initial squaring circuit. Similarly, in the more general case where IM3 products arise from three arbitrary bandpass blockers, only signal content from around one of two relevant beat frequencies needs to be retained in order to reproduce the required IM3 products.

In this case, the bandwidth of the interstage circuitry can be reduced dramatically, allowing the designer to obtain large amounts of gain for relatively little power by taking advantage of the gain-bandwidth principle. Successfully exploiting this relationship reduces the effective noise contribution of the final Gilbert cell multiplier and subsequent alternate path circuitry.

Unlike multistage predistortion circuits such as [24]–[26], the receiver cubic term generator does not need to retain IM2 products around dc for general blocker signals once high-frequency IM2 products are removed. Filtering out IM2 products near dc increases the maximum total blocker signal magnitude for which the receiver cubic term generator meets IER requirements. This is especially true for standards such as UMTS Region 1 in which the two IM3 producing signals of interest have significantly different amplitudes. In this case, the total IM2 energy around dc is considerably larger than the IM2 energy around the beat frequency, and if left unattenuated would dictate the compression point of the interstage circuitry without contributing to IM3 products around $f_{\rm LO}$.

B. Mixer and LO Buffer

The alternate path mixer and LO buffer are reduced versions of their counterparts in the main path. In this case, the "blockers" seen by the mixer are the undesired IM3 products as depicted at points 3 and 5 in Fig. 2. For the peak blocking condition, the power of these signals is on the same order of magnitude as that of the desired IM3 products. Hence, the linearity and noise requirements on these blocks are extremely trivial. Therefore, the IIP2-enhancing tuning inductor of the mixer is removed, while the gate capacitances of the switching devices are substantially reduced. A set of simple differential pair amplifiers is used for the LO buffering.

C. Analog Baseband Circuitry

The alternate path analog postfiltering consists of the first-order real pole at the output of the mixer and another first-order real pole embedded into an active-RC buffer, which drives an 8-bit pipelined ADC running at 16.66 MHz. As implemented on PCB, the analog portion of the alternate path baseband circuitry consumes less than 7.6 mA from a 2.7 V supply. This power could of course be reduced in a fully integrated design. The procedure used to set specifications on the alternate path baseband postfiltering is different from that of the main path in that the properties of the undesired "blocker" IM3 products in this case depend on those of the desired IM3 products. An algorithmic procedure that takes this relationship into account is thus required. Such a procedure shows that if the mixer output pole is at $\rm f_{-3\ dB} = 1.5$ MHz and the buffer pole is at $f_{-3\ \rm dB} < 8$ MHz, then the error due to unwanted aliased IM3 products is negligible with respect to the alternate path noise floor. More importantly, this procedure shows that if the system proposed in this paper were implemented monolithically with a sigma-delta ADC running at or around 50 MHz, then only the first-order pole at $f_{-3\ \rm dB} = 1.5$ MHz is required, greatly simplifying this portion of the receiver design.

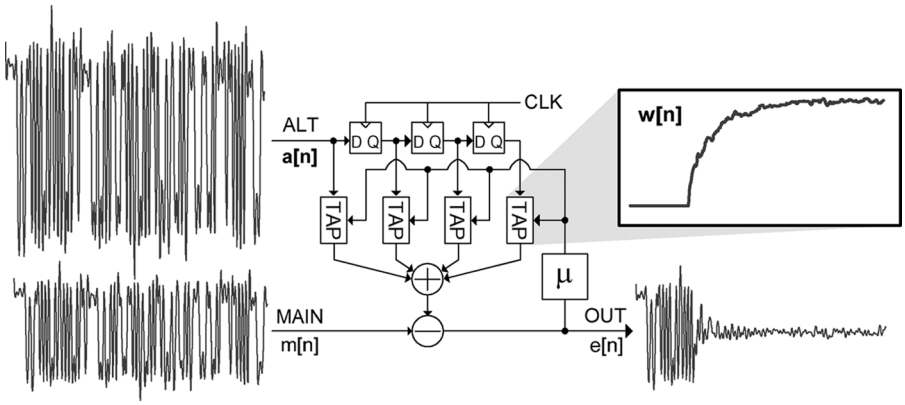

Fig. 11. LMS concept and simulation: real LMS filter.

VI. Digital Equalization

A. LMS-Based Adaptive Equalization

LMS-based adaptive equalizers are common choices for power-constrained applications due to their simplicity and robustness [28]. In this project, the NLMS algorithm is utilized, as its convergence speed is potentially superior to that of LMS [29]–[31]. The dynamics of the NLMS algorithm are also much less sensitive to the properties of the input signal than are those of LMS [28], [30], indicating more predictable behavior over a wide range of conditions. The concept behind LMS-based adaptive equalization is depicted in Fig. 11. Here, a time-varying FIR filter is utilized to modify a reference signal and to subtract it from an incoming signal corrupted by a version of the same reference signal. The taps of the FIR filter are adjusted based on the instantaneous correlation estimate between the equalizer output and the reference signal. That is, if there is any signal correlated with the reference signal in the equalizer output, each tap is adjusted on average in a direction so as to reduce the reference signal content in the output. If the equalizer is designed properly, the filter taps will converge close to a solution that yields the minimum mean squared output signal, but will exhibit a small excess error around that solution.

The operation of the two equalizers in their canonical complex form is described by (5), with bold symbols denoting column vector quantities and the italicized portions corresponding to the NLMS algorithm alone

$$\begin{aligned} e[n] &= \mathrm{m}[n] - \mathbf{w^H}[n]\mathbf{a}[n]; \\ \mathbf{w}[n+1] &= \mathbf{w}[n] + \tilde{\mu}\mathrm{e}[n]\mathbf{a}[n]; \\ \tilde{\mu} &= \frac{\mu}{\|a[n]\|^2}. \end{aligned} \tag{5}$$

When expanded into a physical hardware implementation, (5) takes the form of (6)–(8)

$$\tilde{\mu} = \frac{\mu}{\|a_I[n]\|^2 + \|a_Q[n]\|^2} \tag{6}$$

$$\begin{aligned} \mathrm{e_I}[n] &= \mathrm{m_I}[n] - \mathbf{w_I^T}[n]\mathbf{a_I}[n] + \mathbf{w_Q^T}[n]\mathbf{a_Q}[n] \\ \mathrm{e_Q}[n] &= \mathrm{m_Q}[n] - \mathbf{w_Q^T}[n]\mathbf{a_I}[n] - \mathbf{w_I^T}[n]\mathbf{a_Q}[n] \end{aligned} \tag{7}$$

$$\begin{aligned} \mathbf{w_I}[n+1] &= \mathbf{w_I}[n] + \tilde{\mu}\left[\mathrm{e_I}[n]\mathbf{a_I}[n] + \mathrm{e_Q}[n]\mathbf{a_Q}[n]\right] \\ \mathbf{w_Q}[n+1] &= \mathbf{w_Q}[n] + \tilde{\mu}\left[\mathrm{e_Q}[n]\mathbf{a_I}[n] - \mathrm{e_I}[n]\mathbf{a_Q}[n]\right]. \end{aligned} \tag{8}$$

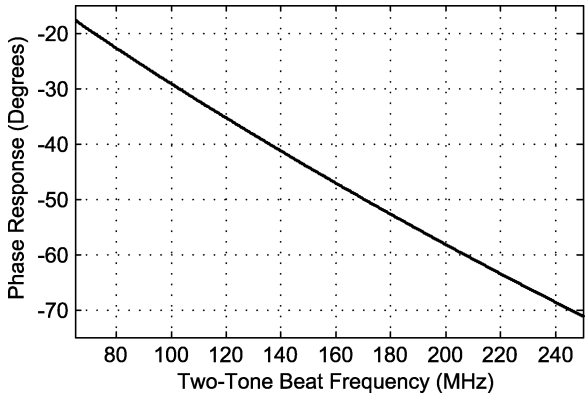

Fig. 12. Simulated phase response of cubic term generator with respect to two-tone beat frequency.

The complex form of this algorithm is required for alternate path distortion cancellation, as the phase relationship between the main and alternate path signals is not fixed. To see why, consider the phase of the IM3 term generator as a function of the blocker two-tone beat frequency as shown in Fig. 12. As the beat frequency changes, the adaptive filter must track the resultant rotational mismatch between the main and alternate paths. Note that for this reason the adaptive filter tap values can not be determined prior to the application of the IM3 producing blockers in such a way as to facilitate accelerated algorithm convergence.

B. Fixed Versus Adaptive Equalization

Adaptive equalization of a known path difference is computationally inefficient. The main reason for this is twofold. First, most analog path differences are IIR in nature, while adaptive equalization algorithms such as those in the LMS family are FIR in nature. Second, even if the path difference were FIR, the LMS adaptive equalizer requires two multipliers per filter tap, as opposed to just one for a fixed FIR filter. Hence, the known difference between the main and alternate path transfer functions is equalized by fixed real three-multiplier IIR filters, as shown in Fig. 4. The remaining path difference between the two paths is a complex dc gain and a small random mismatch in the baseband transfer function. This difference is broadband in the frequency domain and by the duality principle will correspond to a small number of taps required in the adaptive equalizer.

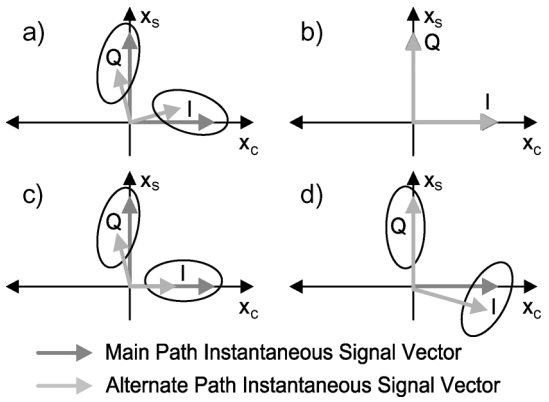

Fig. 13. Insufficiency of complex LMS/NLMS in presence of difference in alternate and main path I/Q phase mismatches.

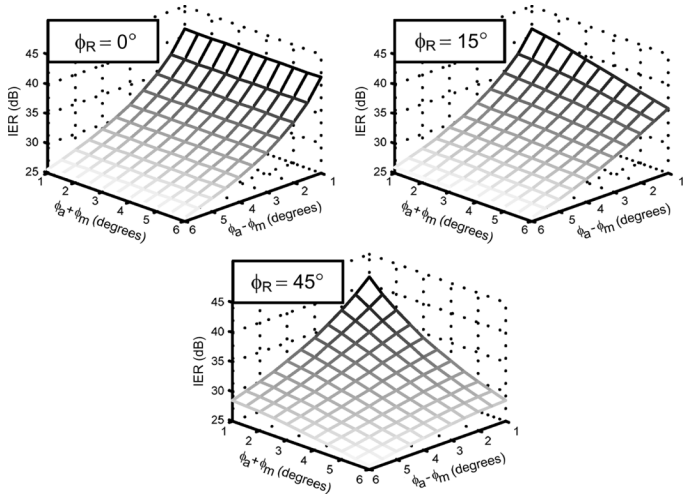

Fig. 14. Calculated IER versus rotational mismatch and I/Q phase mismatches.

C. Compensating for I-Q Mismatch in LMS-Based Adaptive Equalizers

As can be seen from a one-tap implementation of (6)–(8), for a solution to exist to the complex filter tap such that complete equalization is in theory achieved, the signals in the main and alternate paths must be related by a Givens rotation (9)

$$\begin{bmatrix} \mathrm{m_I}[n] \\ \mathrm{m_Q}[n] \end{bmatrix} = \begin{bmatrix} \mathrm{w_I}[n] & -\mathrm{w_Q}[n] \\ \mathrm{w_Q}[n] & \mathrm{w_I}[n] \end{bmatrix} \begin{bmatrix} \mathrm{a_I}[n] \\ \mathrm{a_Q}[n] \end{bmatrix}. \tag{9}$$

This is the case in Fig. 13(a) which shows a vector representation of IM3 products in the main and alternate paths. After the complex equalizer applies the proper Givens rotation to the alternate path signal, subtraction yields complete cancellation, as in Fig. 13(b). However, if as in Fig. 13(c) phase and rotational mismatch exist between the two paths, then clearly their respective signal vectors are not related by a Givens rotation. In this case, complete cancellation cannot be achieved, limiting the effective IER of the alternate path. Using minimum mean squared error analysis, it can be shown that the IER due to this effect depends on not only the phase mismatch within the main and alternate paths, denoted ϕ_{M} and ϕ_{A} respectively, but also on the effective rotational phase mismatch ϕ_{R} between the main and alternate paths. Note that the nonconstant phase response of the cubic term generator shown in Fig. 12 contributes to ϕ_{R} and hence this value experiences significant change not only over process and temperature variation, but also over different blocker conditions. The actual IER expression is given in (10) for phase mismatch only and in (11) when dc gain mismatch exists as well. In (11), $\mathrm{M_I}$, $\mathrm{M_Q}$, $\mathrm{A_I}$, and $\mathrm{A_Q}$ denote the baseband equivalent dc gains of the main and alternate I and Q channels. Expression (10) is plotted in Fig. 14 for some representative values of the phase mismatches.

It is evident that even in the absence of I-Q gain mismatch, small phase mismatches can severely limit the performance of the adaptive equalization. In order to overcome this constraint, an additional degree of freedom must be added to the adaptive algorithm. In the context of the Givens rotation, this means that the relationship (9) should change to (12)

$$\begin{bmatrix} \mathrm{m_I}[n] \\ \mathrm{m_Q}[n] \end{bmatrix} = \begin{bmatrix} \mathrm{w_I}[n] & \mathrm{x_I}[n] \\ \mathrm{w_Q}[n] & \mathrm{x_Q}[n] \end{bmatrix} \begin{bmatrix} \mathrm{a_I}[n] \\ \mathrm{a_Q}[n] \end{bmatrix}. \tag{12}$$

In this case, the new algorithm error subtraction equations become (13)

$$\begin{aligned} \mathrm{e_I}[n] &= \mathrm{m_I}[n] - \mathbf{w_I^T}[n]\mathbf{a_I}[n] - \mathbf{x_I^T}[n]\mathbf{a_Q}[n]; \\ \mathrm{e_Q}[n] &= \mathrm{m_Q}[n] - \mathbf{w_Q^T}[n]\mathbf{a_I}[n] - \mathbf{x_Q^T}[n]\mathbf{a_Q}[n]. \end{aligned} \tag{13}$$

$$\mathrm{IER_{ALT}(dB)} = -10\log_{10}\left[1 - \cos^2\left(\frac{1}{2}(\phi_A - \phi_M)\right)\cos^2(\phi_R) - \cos^2\left(\frac{1}{2}(\phi_A + \phi_M)\right)\sin^2(\phi_R)\right]. \tag{10}$$

$$\begin{aligned} &\mathrm{IER_{ALT}(dB)} \\ &= -10\log_{10}\left[1 - \frac{\left((M_I A_I + M_Q A_Q)\cos\left(\frac{1}{2}(\phi_A - \phi_M)\right)\cos(\phi_R) + (M_I A_I - M_Q A_Q)\sin\left(\frac{1}{2}(\phi_A - \phi_M)\right)\sin(\phi_R)\right)^2}{\left(A_I^2 + A_Q^2\right)\left(M_I^2 + M_Q^2\right)}\right. \\ &\qquad \left. - \frac{\left((M_I A_Q + M_Q A_I)\cos\left(\frac{1}{2}(\phi_A + \phi_M)\right)\sin(\phi_R) + (M_I A_Q - M_Q A_I)\sin\left(\frac{1}{2}(\phi_A + \phi_M)\right)\cos(\phi_R)\right)^2}{\left(A_I^2 + A_Q^2\right)\left(M_I^2 + M_Q^2\right)}\right] \end{aligned} \tag{11}$$

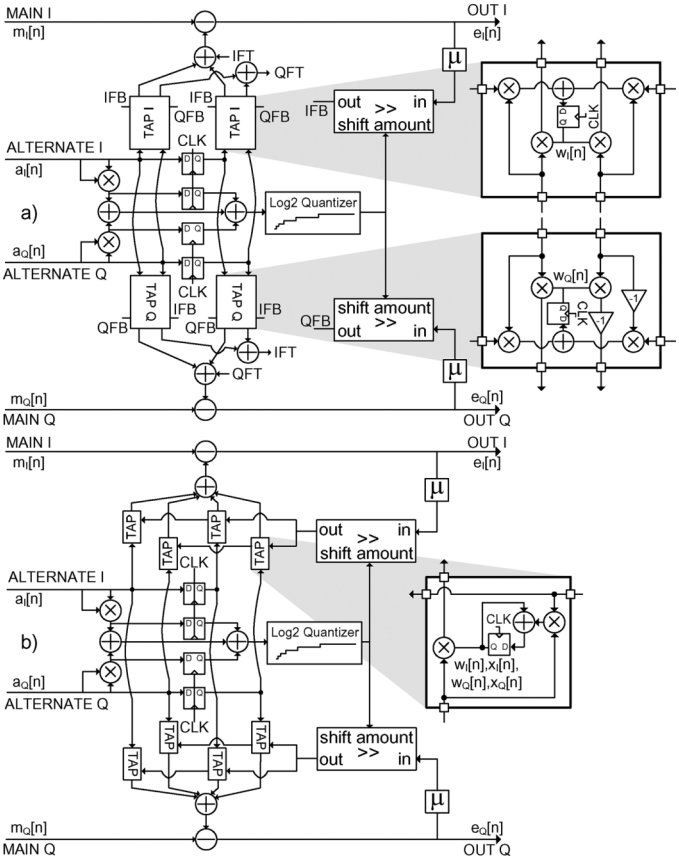

Fig. 15. Hardware implementation of complex NLMS algorithm. (a) Canonical. (b) Proposed architecture with enhanced degree of freedom.

Note that an equivalent solution to the I/Q mismatch problem in a complex adaptive equalizer was suggested in [32], [33]. Unlike [33], however, the equalizer tap update relations are developed in this work by viewing the complex LMS algorithm as a completely real implementation and by substituting the relations (14) into (5). It is then seen that (13) is satisfied and that (15)–(16) realize the tap update equations for the new algorithm

$$\mathrm{e}[n]=\begin{bmatrix}\mathrm{e_I}[n]\\ \mathrm{e_Q}[n]\end{bmatrix};\ \mathbf{a}[n]=\begin{bmatrix}\mathbf{a_I}[n]\\ \mathbf{a_Q}[n]\end{bmatrix};$$
$$\mathrm{m}[n]=\begin{bmatrix}\mathrm{m_I}[n]\\ \mathrm{m_Q}[n]\end{bmatrix};\ \mathbf{w}[n]=\begin{bmatrix}[\mathbf{w_I}[n] & \mathbf{w_Q}[n]]^{\mathbf{T}}\\ [\mathbf{x_I}[n] & \mathbf{x_Q}[n]]^{\mathbf{T}}\end{bmatrix} \quad (14)$$
$$\mathbf{w_I}[n+1]=\mathbf{w_I}[n]+\widetilde{\mu}\mathrm{e_I}[n]\mathbf{a_I}[n];$$
$$\mathbf{w_Q}[n+1]=\mathbf{w_Q}[n]+\widetilde{\mu}\mathrm{e_Q}[n]\mathbf{a_I}[n] \quad (15)$$
$$\mathbf{x_I}[n+1]=\mathbf{x_I}[n]+\widetilde{\mu}\mathrm{e_I}[n]\mathbf{a_Q}[n];$$
$$\mathbf{x_Q}[n+1]=\mathbf{x_Q}[n]+\widetilde{\mu}\mathrm{e_Q}[n]\mathbf{a_Q}[n]. \quad (16)$$

As the new algorithm was obtained from the original via a vector substitution process, it follows from the results in [34] that it is H^{∞} optimal. This change is also efficient from a hardware perspective, as shown in Fig. 15. Both the original NLMS and enhanced-degree-of-freedom NLMS equalizers have the same number of multipliers, which dominate the power and area consumption of the digital implementation.

D. Hardware Implementation of Enhanced NLMS Equalizer

The implemented version of the adaptive equalizer is shown in Fig. 15(b). Two doubly complex filter taps were used to adjust for a small path frequency response difference and for perturbations in the baseband group delay over variations in LO frequency. In practice these quantities will also vary with process and temperature. The division associated with the NLMS algorithm is log2-quantized here, allowing the use of a simple barrel shifter as a divider [35].

VII. Operation of Alternate Path in Non-Static Environment

A. Criteria for Enabling/Disabling Alternate Path

In order to use the alternate path most efficiently, it must be powered on only when IM3 products corrupt the main path signal. Detecting this condition cannot be done with the use of a simple power detector at RF, as such a circuit cannot discriminate between single and multiple blockers. Using a power detector at main path baseband is similarly ineffective, as it cannot discriminate between large IM3 products and large desired signal.

A superior method of detecting a problematic blocking condition is to use a portion of the alternate path itself, as its baseband output power is proportional to the IM3 products corrupting the main path signal. For example, the RF front end portion of the alternate path can be powered on in the event that a problematic blocking condition is possible and its baseband output monitored by a simple power detector circuit. Once a given IM3 power threshold is exceeded, the rest of the alternate path is then enabled to perform IM3 cancellation.

The alternate path front end enable condition can be flagged by an additional power detection circuit at RF when blocker magnitudes exceed a certain threshold or, as in UMTS, when the TX output power is known to exceed a certain threshold. Based on measured results in this receiver, IM3 products large enough to corrupt the desired signal may arise when the TX output power is greater than $+10$ dBm. According to [36], in UMTS this condition occurs 30% of the time in a cell with radius of 1 km and 20 users. Thus, the time-averaged power consumption of the RF front-end portion of the alternate path would be reduced by this amount under these conditions. The time-averaged power consumption of the rest of the alternate path would be negligible, as its operation depends on the rare event when another blocker appears with the proper amplitude and frequency so as to cause IM3 products.

In any detection procedure such as this, the possibility of a false alarm and its effects on the system must be considered. If this were to occur with the system described in this paper, both main and alternate path inputs to the adaptive equalizer would consist of uncorrelated noise-like signals. Since there is no significant correlated data in the main and alternate paths, the equalizer taps will not converge but will exhibit a small variation around the zero value. This noisy signal then multiplies the thermal noise in the alternate path. Since both signals are small, the resultant noise signal added to the main path is very small, resulting in a negligible increase in the receiver noise figure.

Powering off the alternate path can be done with a modified SNR detection procedure within the adaptive equalizer. The IM3 content of the main path can be easily estimated by considering the total summed signal power at the output of the

equalizer taps. Comparing this quantity to the total power of the equalizer output yields an estimate of the desired signal to IM3 product ratio. When this ratio is high enough, the baseband portion of the alternate path can be turned off. Because this SNR estimate can fluctuate under fading conditions, a minimum on-time can be instituted for the alternate path baseband circuitry such that it does not toggle on and off repeatedly within a single blocking incident.

B. DC Offset Issues During Alternate Path Enabling and Solution

As is well-known, direct conversion receivers are susceptible to large dc offsets at baseband [16], [20]. This presents an issue with regards to the adaptive filter in that if both dc offset and IM3 signal are present on both main and alternate paths, the adaptive equalizer will attempt to equalize both signals. However, because the dc offset is large and uncorrelated with the path mismatch at dc, the optimal transfer function of the adaptive equalizer will have a large impulse at dc in the frequency domain. In the time domain, this corresponds to a very large number of adaptive filter taps, which will consume inordinate amounts of power and degrade the performance of the equalizer [28].

A common solution to the dc offset issue in UMTS receivers is to use high-pass filtering at baseband [7], [8], [37], with a cutoff frequency no greater than 10 kHz [37]. In this work, high-pass filtering at 10 kHz is performed in the digital domain for both main and alternate paths to remove the dc offset of the complete analog portion of the receiver, including the ADC. The problem with doing this in either domain, however, is that when the alternate path powers on, the dc offset of the mixer appears as a step to the alternate path high pass filter. Because the cutoff frequency of the HPF is low, the resultant step response takes 3–4 time constants to settle below the error floor, thus preventing convergence of the adaptive filter during this time. Another option is to adaptively remove dc offset as part of the equalizer algorithm [2], [38]. However, it can be shown that this technique effectively implements a high-pass filter and would have the same settling time issue.

The solution utilized in this work to remove this startup transient is to retain the high-pass filters mentioned earlier, but to also power on the alternate path baseband circuitry and measure the dc offset in the digital domain in the absence of IM3 products being passed through the alternate path. This measurement is then immediately subtracted from the incoming signal to remove the dc offset. Since the only signals present at this time are dc offset and a small amount of noise, these operations can be performed relatively quickly (a few microseconds) by a simple averaging circuit, permitting periodic dc offset measurements while the alternate path front end is enabled for IM3 product detection. The complete scheme is depicted in Fig. 16. DC offset correction can be performed in the main path as well, but was forgone in order to simplify the experiment.

C. Behavior of System in a Fading Environment

The adaptive equalizer in the architecture presented herein exists mainly to compensate for unknown circuit mismatches and the effective rotational phase difference between the main and alternate paths. However, the adaptive equalizer may also need to track slightly to compensate for changing blocker characteristics as a result of fading. Considering that most IM3-producing blockers for UMTS are clustered around 2 GHz, and assuming that the maximum speed of the mobile terminal is 250 km/h, the minimum coherence time of the blockers is about 400 μs [39] (note: for this experiment $IL = 0$ dB, $G = 21.1$ dB). The adaptive equalizer needs to be able to converge faster than this amount in order to properly track the changing IM3 products, a requirement that is not difficult to meet.

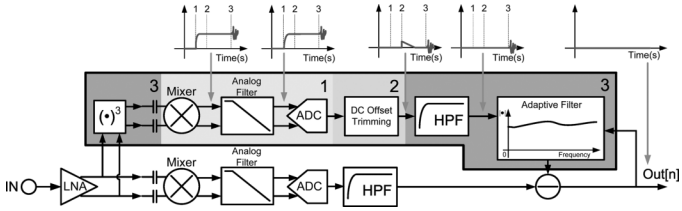

Fig. 16. Alternate path dc offset correction procedure.

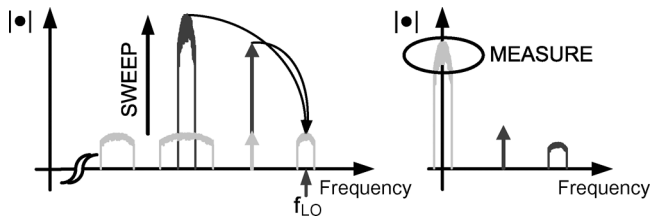

Fig. 17. Modified two tone test concept.

VIII. Experimental Results

A. Receiver IIP3 Measurement Results

Fig. 17 shows the concept behind the modified two-tone IIP3 test used to evaluate the IM3 equalization. The goal is to reproduce the TX leakage and CW blocker signals at the LNA input at several magnitudes (including the worst-case specified), at all 12 UMTS RX frequencies and to measure the output across the RX band in each instance. The TX signal model is a QPSK-modulated pseudorandom noise bit sequence (PN23) at 3.84 MSPS that is upsampled, passed through the UMTS-specified channel filter, and upconverted to 1.98 GHz. The CW magnitude is fixed at 8 dB less than that of the TX. The resultant steady-state error over swept TX leakage magnitude for $f_{\mathrm{LO}} = 2.1225$ GHz is shown in Fig. 18(a). Note that all plots shown and numbers reported depict the I/Q receiver channel with worst-case performance under worst-case specified blocking. The total input-referred error accounts for gain loss, thermal noise, and all IM products. Removing the effects of main path thermal noise and IM2 products yields a lumped input-referred error quantity consisting of all other error sources. From this quantity, which is treated as residual IM3 error, a slope-of-3 line is extrapolated from the worst-case input blocker magnitude to obtain an effective IIP3 metric. Other measurement results show that the corrected IIP3 performance is limited by higher-order distortion products in the main path. Note that 50 Ω kTB noise is removed from these plots and that the maximum total input-referred error in this regard, computed in Section III-B (-98.2 dB) under the

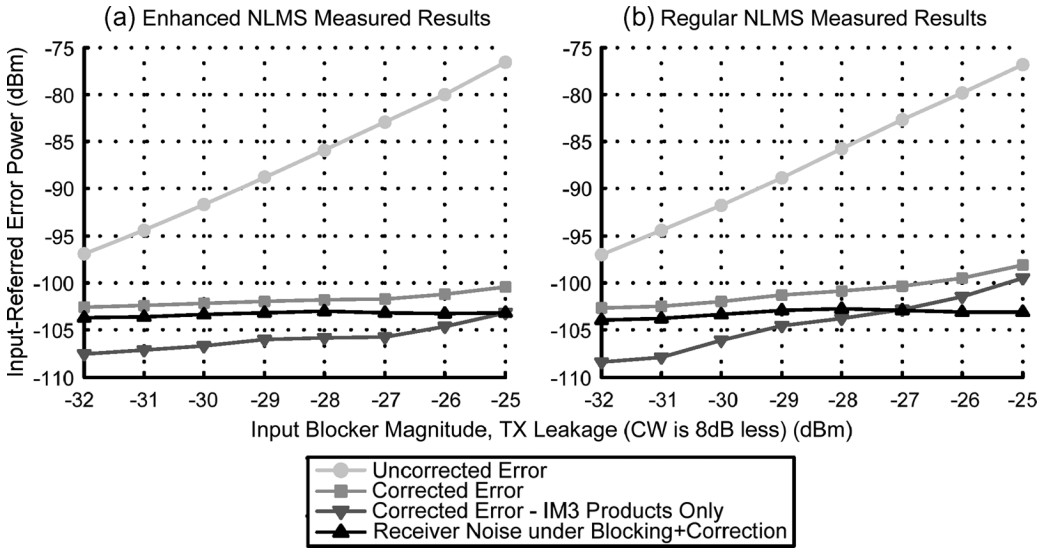

Fig. 18. Measured results of modified two tone test. (a) For proposed enhanced complex NLMS architecture. (b) For canonical complex NLMS architecture.

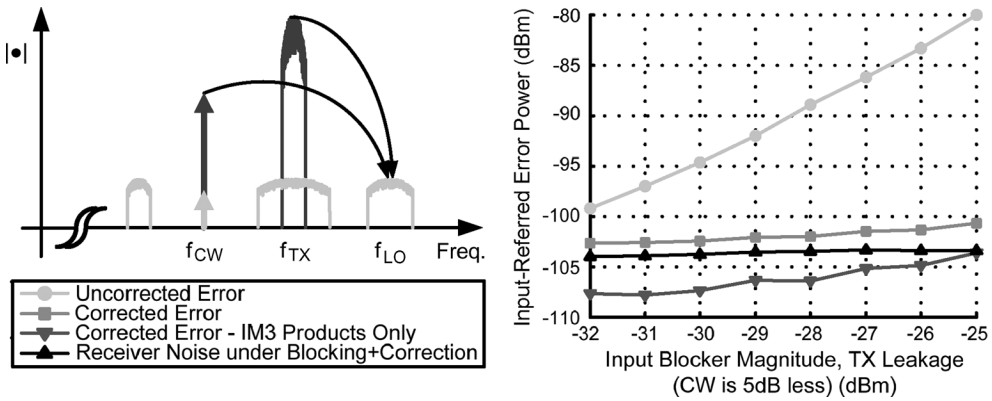

Fig. 19. Measured results of modified two tone testing which IM3 products contain squared TX leakage.

worst-case scenario of −26 dBm TX leakage, is met with 3 dB of margin when correction is applied. The contribution of the baseband circuitry to the uncorrected IIP3 has also been measured and found to be negligible.

In Fig. 18(b) are the results of this same test using the NLMS algorithm without the enhanced degree of freedom. A phase mismatch of about 3° in the main path along with mismatch in the baseband frequency responses are responsible for the higher input-referred IM3 products. This confirms experimentally that this design enhancement produces a noticeable performance improvement for this design.

Although the uncorrected IIP3 of the receiver happens to be sufficient to handle the scenario in which the CW blocker frequency is less than the TX frequency, the CW blocker amplitude was exaggerated far above specification in order to show that this case is covered by the proposed architecture as well. This case generates an IM3 product consisting of a frequency-translated version of the squared modulated TX signal in the main path. It is worthwhile to measure these results, as this condition is subject to an additional error term resulting from the bandlimited nature of the cubic term generator. Specifically, the alternate path output is not squared TX leakage but rather the modulated TX leakage multiplied by a delayed version of itself. The results of this test are shown in Fig. 19 for $f_{\mathrm{CW}} = 1.8375$ GHz and $f_{\mathrm{LO}} = 2.1225$ GHz and show similar correction ratios to those seen in Fig. 18(a).

The experiment performed for Fig. 18(a) is repeated across the UMTS RX band, with the results shown in Fig. 20. The TX frequency is kept at 1.98 GHz and the CW frequency adjusted so that the IM3 products land within the RX band. Convergence behavior of the adaptive equalizer is shown in Fig. 21 for the case where $f_{\mathrm{LO}} = 2.1225$ GHz. It is seen that if dc offset correction is not applied prior to the enabling of the alternate path digital back end, the convergence time is dramatically extended, as expected. The frequency-domain measurement of the digital receiver output in the presence of a moderately large tonal desired signal is shown in Fig. 22 both with and without correction.

B. Receiver Sensitivity Measurement Results

The actual specification that must be met for UMTS is that of the sensitivity test, whose results are often predicted from input-referred error tests by the relations described in [7], [17], [39]. With $L_{\mathrm{DUP}} = 1.8$ dB the receiver must achieve $\mathrm{BER} = 10^{-3}$ for $\mathrm{DPCH\_Ec} = -118.8$ dBm at the LNA input under typical conditions and $\mathrm{DPCH\_Ec} = -115.8$ dBm

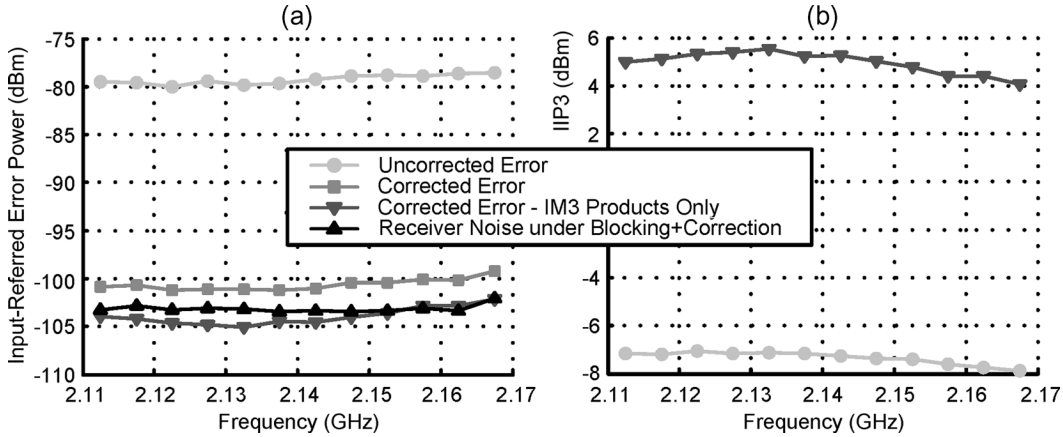

Fig. 20. Measured results of modified two tone test for −26 dBm TX leakage, −34 dBm CW blocker swept over LO frequency.

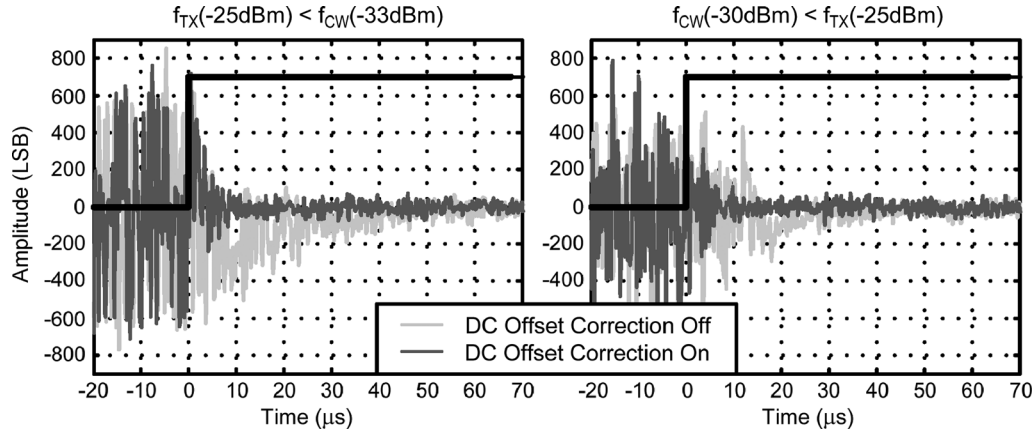

Fig. 21. Measured convergence behavior of adaptive equalization algorithm.

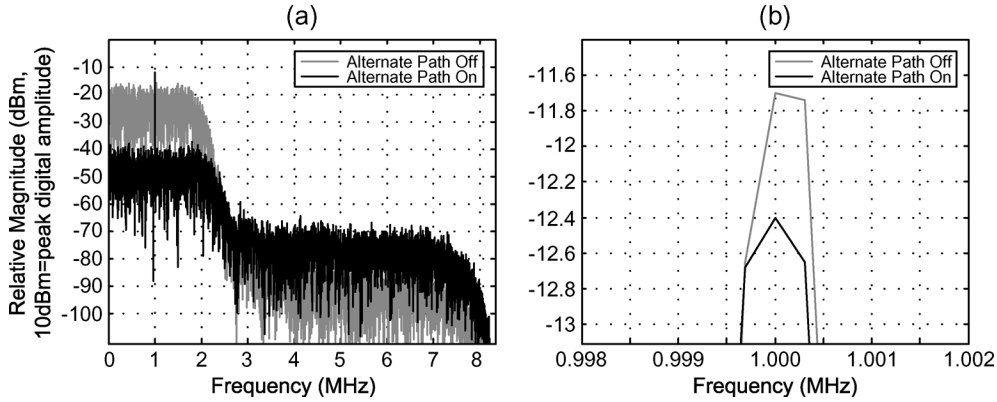

Fig. 22. Digital spectrum analyzer (Agilent 89601 VSA) measurements—Correction in presence of modulated IM3, tonal desired signal. (a) Full output spectrum. (b) Zoomed in.

under worst-case blocking. The results of such a test on the receiver described in this paper at $f_{\rm LO} = 2.1225$ GHz with both I and Q channels active are shown in Fig. 23. The input used is a specification-equivalent UMTS 12.2 kbps downlink reference measurement channel [5], and the measurement results obtained are comparable to those presented in [7]. Each point in Fig. 23 represents the average of 4.88×10^5 bits (2000 data frames), which is sufficient to accurately resolve BER down to 10^{-4} [40]. The baseline sensitivity is −121.9 dBm, 0.5 dB greater than predicted by the measured noise figure, with the discrepancy accounted for by unfiltered noise at frequencies greater than 1.92 MHz. The sensitivity of the receiver under worst-case blocking and correction is −119.5 dBm, 0.9 dB greater than predicted by total input-referred error, with 0.6 dB of this difference accounted for by noise at frequencies greater than 1.92 MHz. This shows that the total input-referred corrected error curve from Fig. 20 is an accurate predictor of the actual sensitivity performance. Without correction, sensitivity significantly exceeds specification at −98.8 dBm under blocking.

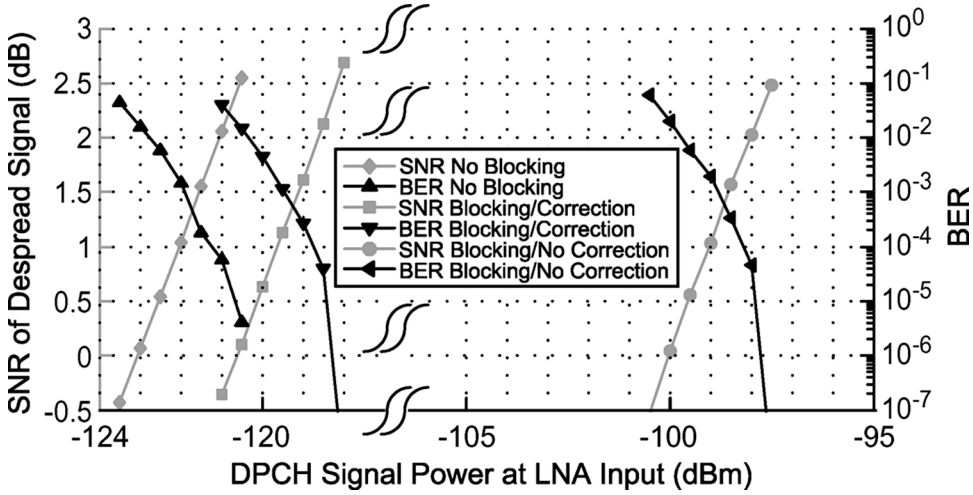

Fig. 23. Measured receiver DPCH SNR and BER under sensitivity, sensitivity/blocking/correction, and sensitivity/blocking/no correction, respectively.

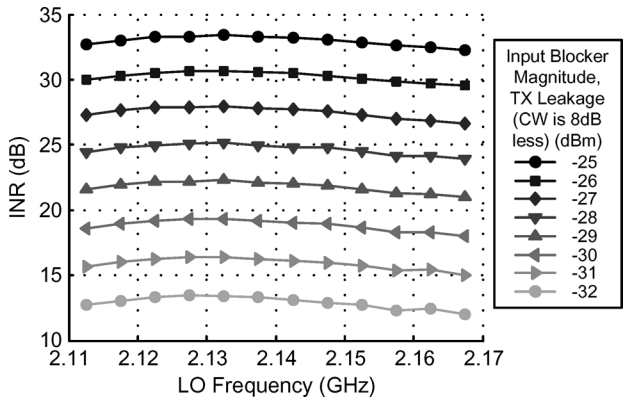

Fig. 24. Measured INR performance of alternate path.

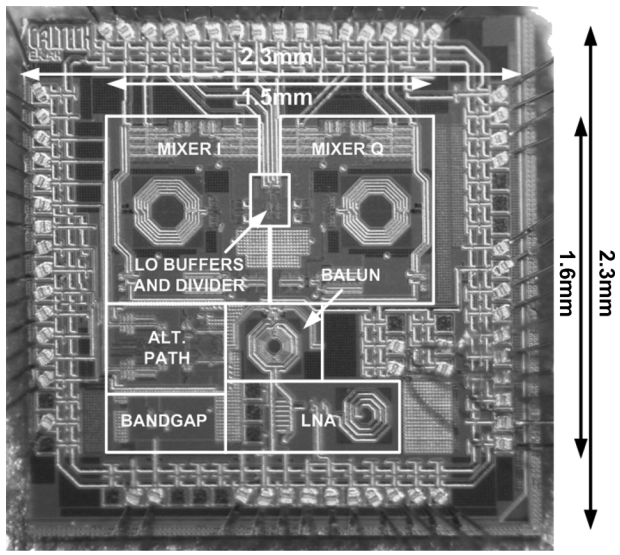

Fig. 25. RF front end die photo.

C. Alternate Path Measurement Results

The IM3-to-noise ratio (INR) performance of the alternate path for $f_{\rm TX} < f_{\rm CW}$ is measured up to the equalizer input and shown in Fig. 24. Performance under worst-case specified blocking conditions at $f_{\rm LO} = 2.1225$ GHz is 31 dB. Additional measurements suggest that higher order distortion products lower IER from INR by less than 1 dB. Alternate path linear term feedthrough is also measured and referred to the main path input. The attenuation referred to the main path input is found to be greater than 46 dB over all LO frequencies, indicating that the effect of these terms in the equalization process is negligible.

D. Additional Measurement Results

The RF front end die photo is shown in Fig. 25. The performance summary for the system and front end is shown in Table II. Note that these and all other quoted results differ from those reported in [41] due to improvements made to the system to permit acceptable operation across the entire RX band. The new power consumption estimate of the alternate path digital back end circuitry was obtained from switching statistics of a gate-level Verilog simulation referencing a 90-nm CMOS process standard cell library.

IX. Conclusion

This paper has presented a receiver architecture that utilizes a nonlinear mixed-signal alternate feedforward receiver path extending into the RF domain, and shows that it dramatically improves the IIP3 performance of an integrated SAW-less UMTS receiver front end. An internally bandlimited RF cubic term generator was described and successfully implemented in order to provide a suitable reference signal for equalization. Implications regarding the design of the other alternate path circuitry, including the digital adaptive equalization, were also examined. Furthermore, a technique to deal with the interaction of dc offset and adaptive equalization while maintaining a relatively small convergence time is described and demonstrated. The excess power consumption drawn by the alternate receiver path is small over time-averaging, as it needs only to be fully enabled in the rare event that an IM3-producing blocking condition exists.

TABLE II
MEASURED PERFORMANCE SUMMARY

Parameter Measured At f_{LO}=2.1225GHz	Result
Active Analog Die Area	1.6mm x 1.5mm
Active Analog Die Alternate Path Area	0.5 mm x 0.4 mm
Analog Die Technology Node	130nm RF CMOS
Analog Die Supply Voltage	1.2V / 2.7V
Estimated Alternate Path Digital Die Area	0.42mm x 0.42mm
Digital Die Technology Node	90nm Bulk CMOS
Digital Die Supply Voltage	1.0V
Analog Die LNA+Main Path Current	28mA (1.2V)
Analog Die Alternate Path Current	6.7mA (1.2V)
Estimated Digital Alternate Path Current	5.6mA (1.0V)
Analog Die LNA + Main Path DC Voltage Gain	30.5dB
Complete LNA + Main Path DC Voltage Gain to ADC Input	70.2dB
Input Return Loss (S11) 2.11GHz-2.17GHz	<-13dB
IIP2 @ 1.98GHz	+58dBm
Uncorrected IIP3 @ 1.98GHz/2.05125GHz	-7.1dBm
Effective IIP3 @ 1.98GHz/2.05125GHz	+5.3dBm
ICP1 @ 1.98GHz	-19dBm
Analog Die LNA + Main Path NF	5.1dB
Complete LNA + Main Path NF	5.5dB
Baseline DPCH Sensitivity	-121.9dBm
DPCH Sensitivity Under Blocking/Correction Off	-98.8dBm
DPCH Sensitivity Under Blocking/Correction On	-119.5dBm
Baseband Signal Measurement Bandwidth	10 kHz-1.92MHz

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